Digital IC Design
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Lecture -73
Flop Characterization

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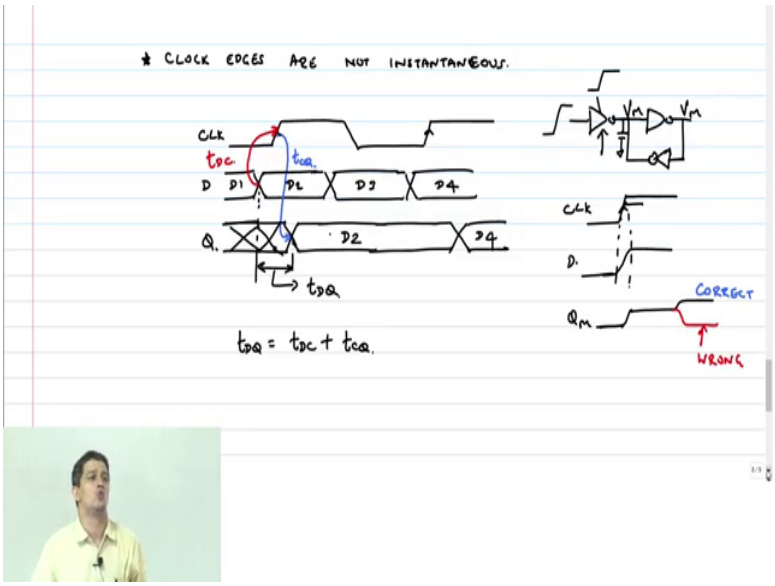

So, I need to discuss one more topic before we can wind up today ok. The last thing I want to discuss is I want to now remove one more constraint clock edges are not instantaneous. In that case I want to see how to analyze, setup, hold, clock to Q whatever it is ok. So, my clock edges are going to look like this.

And, my data let us say this is the positive flop, positive edge flop data is now going to change like this D 1 to D 2 and any further change should get ignored until the next D 3, D 4. Q basically should just right I do not know what the state is right and from the clock edge this

change should happen ok. So, this will be D 2 and after the thing it will become D 4 ok. So, you cannot analyze this in a theoretical way like we did for earlier examples, you have to go to simulations ok. So, I want to now tell you how you can figure out what the setup and hold time of your flop is through simulations right.

So, first we will look at what is the setup time ok, I want to see what the setup time. Actually you look at both of these together setup and clock to Q delay you will look at it together ok. So, what we will do is I am going to this delay is t CD clock to data, data to yeah t DC sorry data to clock delay ok. And what is this delay? t CQ right, then there is an other delay which is basically the time from data to Q t DQ ok.

So, what is t DQ equal to? t DC plus t CQ. So, now, my point is I want to make t DC smaller and smaller that is I am going to bring the data change closer and closer to the sampling edge and see when the clock when the flop fails. So, the thing is the flop failing is actually more an extreme condition that may you know it may tolerate more delay. The point is as I bring the data edge closer and closer to the clock, that feedback loop will start entering meta stability region ok.

So, if I have now look at this thing just for simplicity I will draw this without any you know without cutting out the feedback right, over powering the feedback. So, what is happening is my data change is happening, my clock is also changing and it so happens that clock is changing here, data is also changing here. So when the clock actually cuts off right, when the clock cuts off remember that this is my; this is my sampling edge. So, when its samples right and the clock goes from 0 to 1 my L 1 is going to go to what state?

Student: (Refer Time: 05:09).

Opaque, L 1 will go to opaque state, that means it is going to just hold the data in the feedback mode ok. Now, let us assume that D 1 D changed something like this almost in sync with the clock, at somewhere here the clock will cut off this tri state inverter path right. And, it is very much possible that this capacitor here will charge not all the way to V DD or ground or discharge all the way to ground, it may come and land up somewhere near V M right. And

I already told you that, that is also a reasonably you it is a meta stable state. If this comes to V M, this will also be V M and it can remain in that state for a long time until noise or something comes and switches it one way or the other ok.

So, what you see is if this happens the Q M right, let us assume there is no polarity changing Q M will actually charge to V M like this for some time and then go high. You can do this in your simulation and check, bring it closer and see what happens to Q M, Q M will go to this meta stable state for some time. And, the closer and closer you bring the data change to the clock this time will keep on increasing. It will remain in that thing and ultimately, because of some capacity coupling or something this Q M will switch to the actual value ok.

So, in this example the D and Q M are the same polarity, if I keep bringing this edge closer and closer at some point this will go to the wrong value also, it can switch to the wrong value you, Q M can switch. So, this is completely wrong right this is correct, but it will happen with some delay. That means, even though the setup time was correct, data was data could be sampled correctly by the flop; the clock to Q delay will go up significantly, because only if Q M settles to the correct value will Q then reflect the right value out right.

That is what we are going to know exploit in order to give a very formal definition to set up and tool time ok. So, what I am going to do is I am going to now plot.

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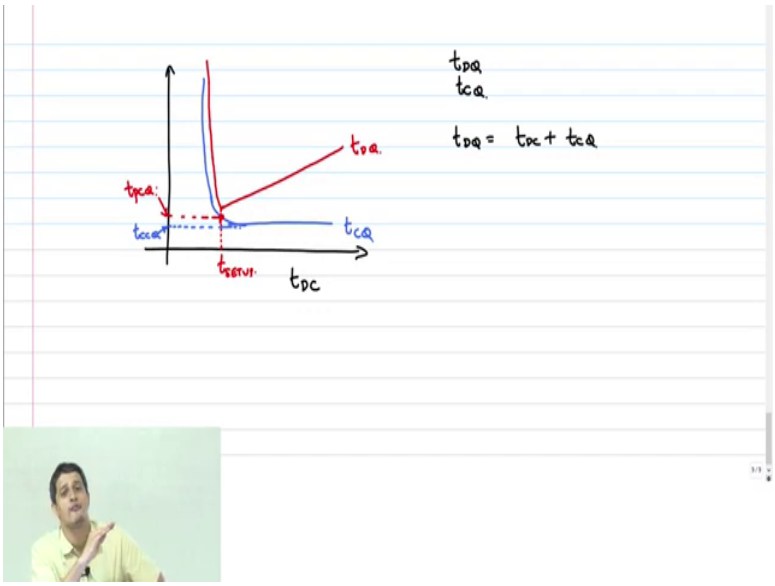

So, I am going to bring my clock edge closer and closer right. So, I am going to plot versus t DC ok. And, what am I what are the things that I am going to plot? I am going to plot t CQ and t DQ ok, I am going to plot two things t DQ, t CQ and remember that t DQ is nothing, but t CQ plus or rather t DC plus t CQ ok.

So, let us assume that t DC was a very large value, that means, the data change; the data change has happened far away from the clock edge. What should be the value of t CQ in that case? Will it be minimum or maximum? Yeah, it will be minimum because the data change has settled correctly, there is no meta stability problem, the feedback loop would have settled and the output also will appear very quickly.

Therefore, if you look at my t CQ for large t DC, it will be some minimum value ok, t DC right; as I bring the t DC closer and sorry this is t CQ. As I bring t CQ closer and closer I

mean t DC closer and closer what will happen to t CQ? It will start increasing right, the clock delay will start increasing like this and at some point it can go up significantly, because the meta stability time will be very large after that ok; you have to simulate this to see it.

How will the plot of t DQ look like now versus t DC? For the large value of t DC what is the equation like? Is it a constant is it a.

Student: t DC (Refer Time: 10:39).

It is a straight line because its t DC plus t CQ and t CQ is a fixed number now right. Therefore, it is going to be a thing like this correct. So, as I bring my t DC right my data change closer and closer to the clock edge my t DQ actually is coming down. Why is it coming down? Because, t DC itself is reducing, t CQ is a constant number, t DC is reducing.

Therefore, the delay keeps reducing as I bring it closer and closer to the edge, but at some point because t CQ is now going to go up t DQ also starts going up right. And therefore, you will see that this takes a turn like this and goes up of course, remember for any value of t DC t DQ should be greater than t CQ. So, it will always be above that thing ok, this is my t DQ. So, what you do is you pick this time when it is minimum ok. Let me redraw this slightly; so, that I can make it more exaggerated ok.

You pick the time when t DQ is minimum, you get a particular value of t CQ right, that t DC for which t DQ is minimum is defined as the set up time. Setup time is formally defined as the time when data to Q change, data to Q delay is minimum that t DC when this delay is minimum. Now you get two different t CQ's right yeah. If t DC were large then the t CQ is very small, but if t DC were at setup time then you see a larger t CQ. This is the origin of contamination and propagation delay for clock to Q.

So, this I will call as t CCQ right this point and this point I will call as t PCQ ok. So, when you make a flop you have to do this exercise take t DC closer and closer and now again you have to do it for both 1 and 0 transition; it is a different it will be different delays ok. You have to because PMOS and NMOS are not identical in reality. So, you have to do it for both

transitions plot your t DQ and t CQ versus t DC, see where my t DQ becomes minimum that point is defined as your setup time right that is t C that t CQ right, is defined as the propagation clock to Q delay.

And, the when t DC is far enough, that delay is called the contamination clock to Q. So, remember like I told you the origin of contamination and propagation delay are very different for flops and combination circuits and this is the origin for sequential circuits ok.