Digital IC Design
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Lecture – 72
C2MOS Flop

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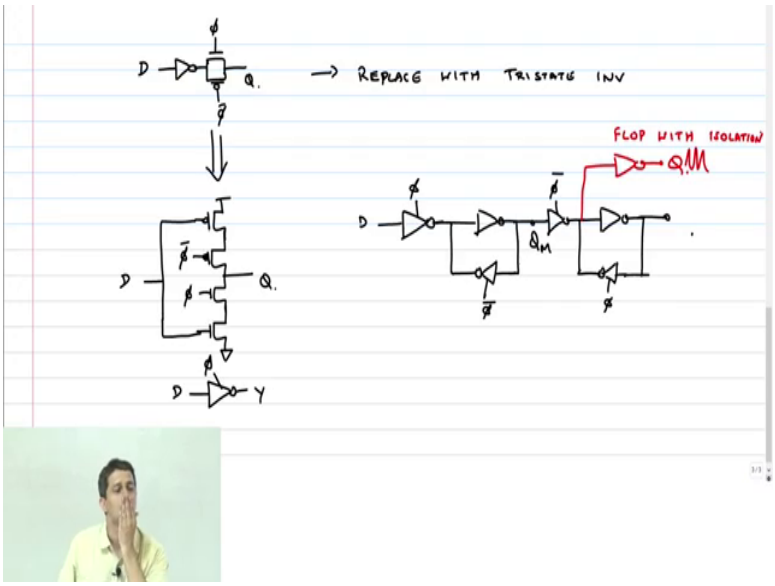

So, now I can you know I can change this concept of an inverter followed by a fast transistor right. This was D; phi let us say phi bar you got something here. What was the alternate circuit I said that can be used instead of this cascading and inverter by a transmission gate?

Student: (Refer Time: 00:46).

Yeah?

Student: (Refer Time: 00:49).

I told you one more circuit which has similar functionality, but slightly different configuration.

Student: (Refer Time: 01:01).

Yeah, buffer with a clock or an enable it is called a tri-state inverter, I can replace with inverter, right. Therefore, I can simply replace this structure with this kind of a thing. So, here I said this is phi bar and this will be my D and this will be my Q, right. So, I will represent this with a symbol like this inverter and an enabled phi D Y. It means phi is connected to the NMOS transistor phi bar is connected to the PMOS that is what the symbol means.

So, now, I can replace that flop that I had earlier with such a structure ok. D then, I will in the feedback path I could put another tri-state inverter right or I could consider that like a let us put another tri-state inverter there not a big deal. So, let us say this is phi, then this has to be phi bar right; then I can put another tri-state inverter here with this is phi bar feedback inverter Q and this is Q M, right.

So, in general if you look at this Q is what is going to be available to the outside world. In the sense the next gates input will be connected to this Q right which means that that node is going to be available as a wire somewhere right and any noise on the output suppose there is a noise on the output, let us say there is a large noise. Then, this feedback path can potentially get affected because remember this is now trying to hold some data right, in a feedback mode and let us say the noise is large enough that it could flip it. Then the state of that flop can potentially flip, right.

In order to avoid that what you do is you isolate this output in the following way. You add another inverter and make Q available here instead of here which means now Q is what is going to connect to the next gate and any noise will affect only this guy. This internal node is not going to be available to the next circuit; I can shield that appropriately right. Therefore,

now any noise on Q M is at the output of an inverter as opposed to input of this inverter here and therefore, the noise will not percolate backwards and affect my functionality. So, this is a latch or a flop right with isolation.

So, let me just show you one more interesting circuit here, yeah.

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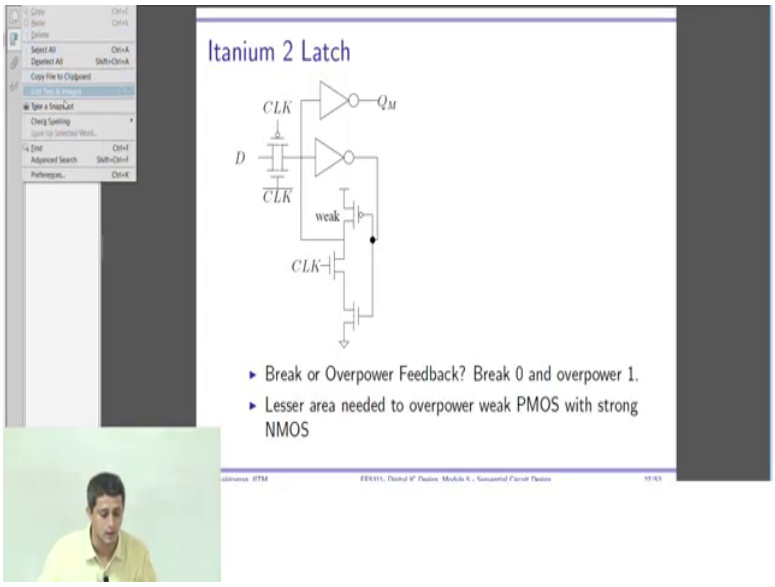

What is this look at this latch here, ok? I will basically copy paste this here.

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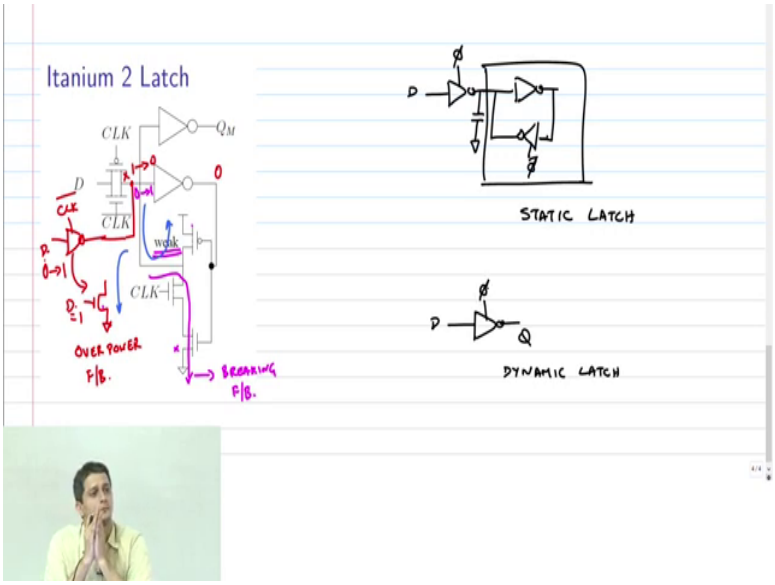

So, this latch of course, it is been drawn with the bus transmission gate in the beginning you can always replace that with the tri-state inverter, it does not matter. Is this a latch with breaking the feedback or overpowering the feedback configuration?

Student: (Refer Time: 07:15).

Yeah.

Student: (Refer Time: 07:17).

Is it true for both logic states?

Student: We cannot say that.

Ah?

Student: We cannot say anything.

No. So, that is what I am saying. So, you have to tell me this analysis now. For if D was 0 and if D was 1, what would happen? So, let me replace this with the tri-state inverter and maybe easier to analyze this is clock bar. So, if this node happened to be let us say 1 ok; that means, the feedback path is holding a 1 therefore, this is a 0 in that condition if I want to now flip the flop right, if I wanted to flip the state D has to be I want to make this 1 go to 0; that means, D has to be what?

Student: (Refer Time: 08:56).

Nodding, initially this node X has a 1, I want to make it 0. Therefore, D has to go where?

Student: 1.

1. So, D has to go from 0 to 1 and clock also has to be enabled only then it can happen. Now, when that happens what will happen to this path this is basically NMOS transistor here right which is basically not this guy has one NMOS transistor to ground right which is connected to D and this is now becoming 1. So, there is a pull down path like this. Earlier when the intermediate node was storing a 1, it was being pulled up through which transistor, through the weak transistor that is shown here this was the pull up path.

So, there is going to be a fight between the PMOS of the feedback inverter which is labeled as a weak transistor here and the pull down of this tri-state inverter which means it is what kind of is it breaking feedback or overpowering feedback?

Student: Overpowering.

Yeah, right. So, you have to overpower feedback in this case, right. So, therefore, this is overpower feedback. Other way, suppose the node X had a 0 and I wanted to make it 1, then node X had a 0 means it was being pulled down through which guy? It was being pulled down through this path right when clock was 1. Now, clock goes to 0, I want to sample the data I want to bring it in. So, when clock goes to 0 what happens to the feedback path?

Student: Break.

It breaks and therefore, now my tri-state inverters free to write it is data unconditionally. So, here this is breaking feedback. Why did not they do it the other way round, where they said that let us do breaking feedback for the 1 case and overpowering feedback for the 0 case?

Students: (Refer Time: 11:52).

Exactly, here note that when there is a fight between this PMOS and this NMOS. It is always easier to make the NMOS stronger with smaller area than the PMOS. If I had done the reverse case what would have happened is there would have been a fight between the NMOS here and the PMOS of that inverter. Now, the tri-state inverter has to win. Therefore, the PMOS has to be sized up significantly.

So, in order to reduce area you have to do this only on the by sizing the PMOS down right. So, you allow the fight to happen between an NMOS pull down and a weak PMOS pull up. That is why you will see this weak PMOS pull up in many many places because it is very easy to make a PMOS weak with small area, ok. Any questions here?

So, now, as I told you, I had this tri-state inverter D with a feedback, right. This was phi, this was phi bar. Question is do I really need this. With the element that is storing my data or that is going to hold my data is this feedback inverter, right. If this is 0 at the input here, the output

will be one that output will drive the 0 and this feedback will hold it steadily as long as the power supply is on, right.

Therefore, this is known as a static latch just like we did static CMOS and dynamic logic in combination circuits you also have the corresponding static latches and dynamic latches in sequenced circuits, ok. It turns out that there is a capacitance here and therefore, technically that capacitance can store the value for a short period. Ultimately if you look at what should happen each latch needs to hold the data for half a period the holding needs to happen for half a period the other half it is transparent. So, there is something driving it.

So, if you look at very high clock speeds or the order of gigahertz then the clock the data has to be held only for 1 nanosecond right and technically it is possible to do this with a reasonable capacitance on chip right. And, therefore, you can simply use a tri-state inverter as a dynamic latch fine, ok.

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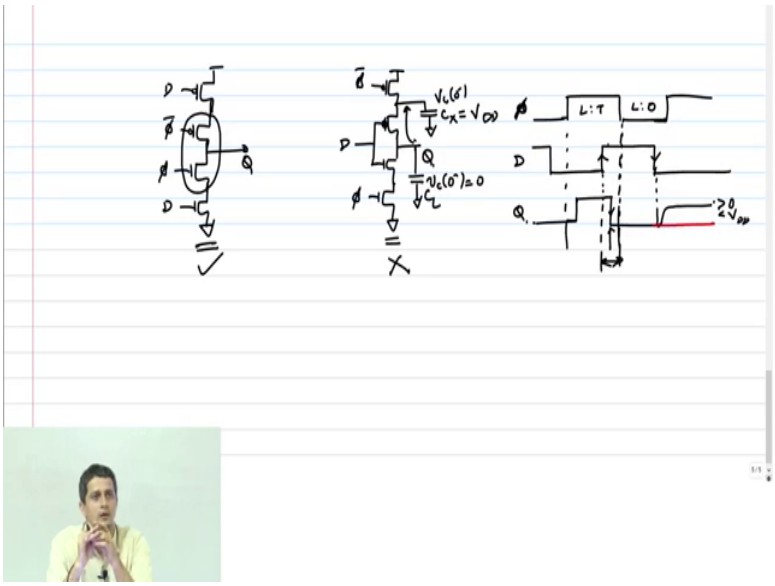

So, now let us look at this connection right I said a tri-state inverter had to be like this. This is D, D, phi, phi bar. Can I swap D and phi? Logically, this is also a valid flop right, phi bar, phi and then this I will call as D. Logically, these two are the same right when phi becomes 1 both of them act like in an inverter when phi is 0 both of them do not provide a path to either V DD or ground thereby tri-stating the output Q. Q will be in high impending state, but are these two equivalent otherwise.

So, let us look at what we want from a flop. This is my clock, data is so, now I will talk. So, this is phi, this is my D. So, let us say that my D is changing like this. What should happen to Q after the data has been sampled and is going to be held? So, in this case when phi equal to 1 data is going to the latches in what state, it is in transparent state right. So, D will any change in D will just go through right there is no problem there. So, if you look at the output here this

is a positive latch. So, therefore, Q will simply follow D with an inversion of course, and some delay; now, let us say D changes here, right.

So, this is latch is transparent, latch is opaque. When the latch becomes opaque any change in D should not reflect in the change in Q, correct. But, now in this configuration let us say that the skew was basically what? 1, Q was 1 and my D now went to 0, ok. I am looking at this transition here. So, if D was 1, then my no; so, what should oh sorry, this is what should happen right because D as change here and Q should get inverted in the transparence phase, right.

So, D was 1 and Q became 0. So, this capacitor was discharged to equal to 0, right out here. Now, when Q becomes when D becomes 1, this Q is now going to get connected where?

Student: (Refer Time: 19:00).

It is going to get connected to this capacitance, right. There is an intermediate capacitance C X here and this is C L, which means that this node will now charge share with C X, you agree with me? What was the state of C X when at D where the clock went low?

Student: (Refer Time: 19:35).

Q has fallen, right; Q has fallen, right. Now, at this phase right in this period here my clock PMOS is on right and my D has what has happened to D? It has gone high, thereby turning off this guy. So, what is the state of C X?

Student: V DD.

V DD, right; V C of 0 minus is V DD. So, this Q now because of this when my data falls right in the opaque state will now charge share and come to some in between value. In this configuration any change in D after the clock has shut off will not reflect in the change in the output Q, because the clock is actually getting the change right in between. So, therefore, this

is the only correct configuration for a tri-state inverter and this is not a correct configuration for the tri-state inverter.

So, in this configuration 1, Q will continue to be at 0. Of course, now it depends on what this charge shared value is right. Whatever this value is, it will go to something between 0 and V DD right. This will be greater than 0, less than V DD depending on how where it goes and lands the following states may trip or not trip, but that is not a good thing.

Any questions here, ok?

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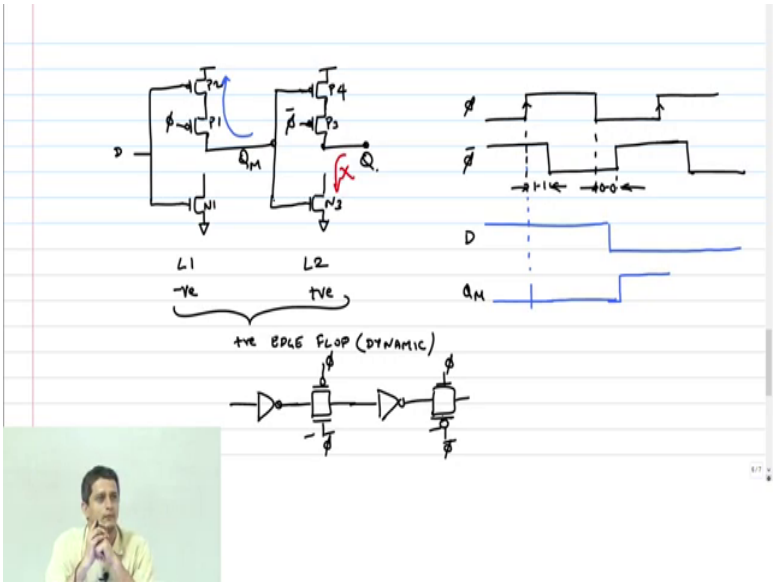

So, now we will look at a configuration which is a very interesting configuration from the perspective of clock overlap, ok. This is going to be my D, this is phi bar, phi, this is phi and this is phi bar Q M, Q, ok.

So, this is just a dynamic flop, two dynamic latches have been cascaded that is all we have done, ok. This is latch L 1, this is latch L 2. What kind of a flop is it? Positive edge triggered or negative triggered?

Student: Positive edge triggered.

Yeah, because when clock equal to 0 the data will go through and therefore, this is a negative latch, this is a positive latch together you get a positive edge flop and it is a dynamic flop, ok. Now, I am going to analyze this thing for the clock overlap condition that we discussed earlier. This is my sampling edge now, correct; the rising edge is my sampling edge. So, this is phi, phi bar; I am going to delay phi bar a little bit now as usual. So, this is my overlap, ok. This is what 1 – 1 overlap and this is 0 – 0 overlap, ok.

So, first let us analyze the 0 – 0 overlap case, ok. So, what will happen can you tell me what transistors will be turned on, ok? Let me label them N 1, N 2, N sorry, P 1, P 2, N 3, N 4, P 3 and P 4. In my 0 – 0 overlap condition which transistors are off? Both phi and phi bar are 0.

Students: (Refer Time: 25:00).

Yeah, all the BMOS; so, N 2 and N 4 are going to be off. These transistors are basically off, ok. So, maybe let me because I need the other condition also. So, let me make a copy of this, yeah.

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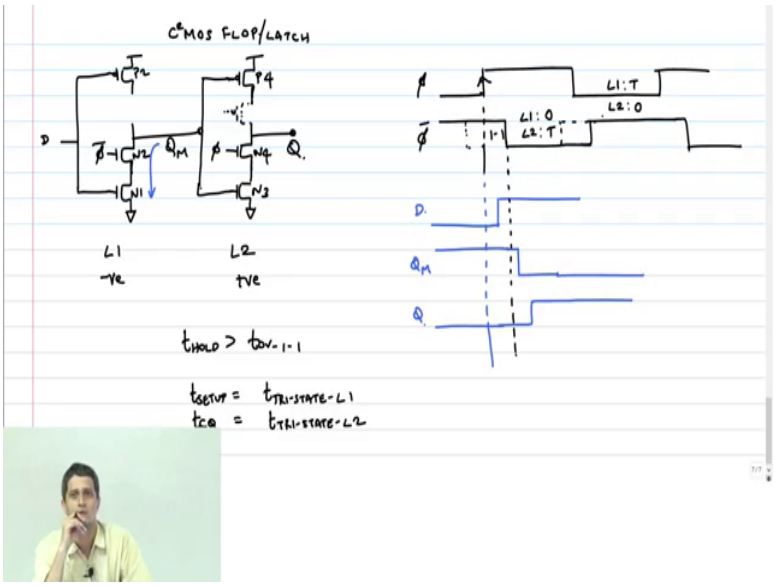

So, therefore, I am going to now remove this transistor's from the path for the 0 – 0 overlap condition, fine. So, now, I want to see if a change in D can percolate all the way to Q or not, right. So, should I even analyze this particular condition I mean which of the two transitions should I analyze is my question. Should I analyze D going from 1 to 0 or should I analyze the other case? Let us say D went from 1 to 0 in my 0 – 0 overlap period or D goes from let us say 0 to 1 sorry, let us look at the red case first. D goes from 0 to 1 in my 0 – 0 overlap case.

Can the change in D go to Q M first of all? No, why because that NMOS has already cut off. So, there is no discharge path available. Therefore, the only condition I have to analyze is this condition where the data goes from 1 down to 0 thereby there is a pull up path right. So, Q M can therefore, now right; so, let me draw this in blue. So, that it is there is a pull up path, right.

So, therefore, what happens to Q M, let us plot that. Q M was initially what, 0 right, at this edge it is going to sample 0 because D is 1, Q M is an inverted value of D. Therefore it will be 0 here, but now D has switched right and there is it is going to pull Q M all the way up, right with some delay, correct. I am not go all the way till the edge let me draw it here. So, the change has now percolated to Q M.

Question now is can it go further from there? No, why because I need to discharge through the NMOS transistor and there is no pull down path here, right. So, on the non sampling edge nothing goes through. What is it that did the trick compared to the previous case?

So, we analyzed in earlier case where the there was an on the non-sampling edge the overlap was a problem and we said you have to make sure that the delay through these gates you know take care of the overlap. What is it that is doing the trick here or if put it other way if I were to go back to that static latch or flop and apply the same thing and ensure that the non-sampling edge overlap is not an issue, what should I do?

Student: (Refer Time: 29:37).

Yeah?

Student: (Refer Time: 29:38).

Remove the?

Student: Transmission.

So, what is; so, there is a very critical thing. You see that the in both cases only the pull up path is available both latches, but in order for data to go through one has to pull up other has to pull down, only then data can go through. So, there is a logic inversion that is doing the trick here. Earlier when I used a transmission gate; the transmission gate was conducting for

both 0 and 1 logic. What we are done here is for 0 you are going through the PMOS, for 1 you are going through the NMOS, right.

If I we if for example, if I replace this guy with a circuit like this, right this is also a dynamic latch right and I put another inverter here and make a flop like this, right. Let me call this as phi, phi bar right or so, this is phi bar and phi. I cannot do that here. The same thing will not hold because now for both 0 and 1, these two transmission gates will conduct and therefore, I have a race path available. What is doing the trick is making the 0 conduct only through the NMOS making the 1 go only through the PMOS and then there is a logic inversion in between which is ensuring that these two are complimentary to each other, clear, ok.

So, now let us look at the other condition which is basically my on the sampling edge I want to see what happens, right. This is phi, phi bar. So, 0 – 0 overlap there was no problem, this is my 1 - 1 overlap. What are transistors that are going to conduct or what are transistors that are going to be off in this overlap period?

Student: P 1 and.

P 1 and?

Student: P 3.

P 3. So, I can remove this transistors off, correct? Now, what is the condition that I have to analyze first of all? Ok, before that tell me after the overlap period which latch is in which mode L 1, L 2 right this is L 1 and L 2. After the overlap is done, it is a positive latch I mean it is a positive flop positive edge triggered flop. Therefore, L 1 has to be in opaque mode and this will be in transparent mode and this will be in transparent, this will be in opaque, right.

So, now again tell me if I should analyze the case where D goes from 1 to 0 after the overlap I mean after the clock falls or the other way; which conditions should I analyze?

Student: 0 to 1.

0 to 1; why because when if D goes from 1 to 0, there is no pull up path therefore, that is that is not even going to go through that change cannot even go through to Q M. So, forget about Q. Therefore, I can ignore this condition completely I am going to look at only this particular condition D going from 0 to 1 in that overlap.

Now, this is the difference that you want to be careful about from the previous analysis that we did on the non-sampling edge and the sampling edge remember. If D happens to go through right because there is a pull down path; there is a pull down path available therefore, if D goes to 1, Q M will fall to 0, what happens after the overlap is done?

Student: (Refer Time: 34:31).

Yeah?

Student: (Refer Time: 34:34).

What is happening in L 2 after that?

Student: It is (Refer Time: 34:40).

It is transparent; that means, any change that has gone through to Q M will go straight to Q after that and therefore, you will have a serious violation. Therefore, Q M if you look at this will basically happen to be like this, right and Q which was actually supposed to sample the edge 0 right, will actually get inverted like this somewhere in between my sampling edge is this and there is a problem. How do I solve this problem?

Student: (Refer Time: 35:28).

Yeah?

Student: (Refer Time: 35:29).

Someone just said it. Hold, again hold time condition. Anytime there is a problem on the sampling edge you have a rescue it is called the hold time. Impose a condition that my whole time should be greater than the overlap period and I am done, the flop will work. It is a violation on the non sampling edge that is going to ruin your circuit and you should never have a violation on the non-sampling edge; sampling edge you can impose this condition. Worst case let us say you designed it wrong something happened, you just say my hold time is larger it does not mean that the circuit is unusable.

But, if there is a violation on the non sampling edge then that is a race condition and it is not even fixable later. You have a big problem; you cannot impose a whole time constraint or a setup time constraint, ok. So, in this case you just impose the condition of t hold should be greater than t overlap of 0 – 0, I mean of 1 – 1, I am sorry, yeah.

Student: Why Q M becomes (Refer Time: 36:46)?

Why Q 1 becomes; why Q M?

Students: Q.

Why Q, because Q M is become 0 and after the then what I am saying look at what has happened after this overlap period, what has happened to L 2 my PMOS transistor is back and both are conducting it is like an inverter now, it is transparent. That is why you have to very carefully sorry, analyze what happens after the overlap period; during the overlap it is sometimes to allow data to go through little bit, but it depends on what happens after the overlap. If L 2 becomes transparent then you have a problem, ok. Any questions here?

So, what is the setup time of this flop? It is basically just a delay of L 1 right, t not inverter I will call it tri-state of L 1, right whatever delay as long as you are able to charge that capacitor on Q M correctly your setup is done, right. If you cut it off before that then you have a problem what about t CQ?

Yeah?

Student: (Refer Time: 38:28).

Exactly, this is t tri-state L 2, ok. This by the way is called C squared MOS flop, right and each state is basically a latch, C squared MOS latch. Essentially this is insensitive to clock overlaps, what do you I mean? It does not mean that any both overlaps is not an issue, 1 overlap is still an issue, but I can alleviate that by imposing a hold time constraint. It is always the other overlap period that is a problem and this flop is insensitive to that overlap; in non-sampling edge overlap is not an issue, ok.

By the way, I leave it to you to analyze what happens if phi bar comes early. That could also happen right, clock and clock bar it does not mean the clock bar is generated from clock always. Clock and clock bar maybe generated separately and then distributed to the entire chip which means clock bar could come early also, you never know. So, you can analyze that condition on your own and so, you have to see how that is going to change your analysis.

Student: Then it is (Refer Time: 40:06)?

Clock to Q now, right; what is clock to Q? Basically, my clock has gone high which means that L 2 has become transparent. It is how long it is going to take to charge Q. Q M has already been set up now, Q M has already been charged because of the setup time. It is only a question of how long Q M takes to go to Q that is clock to Q because when my clock goes high; that means it is sample the data and L 2 has become transparent, Q has to charge. So, that is just a delay of L 2 under ideal conditions, ok; any questions here.

General analysis of this you know clock overlap it may take some time for you to digested go back, look at the other circuits also, analyze what happened and see and then come back to me later if you have any questions, ok.