Digital IC Design
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Lecture – 70
Alternate Circuit Implementations

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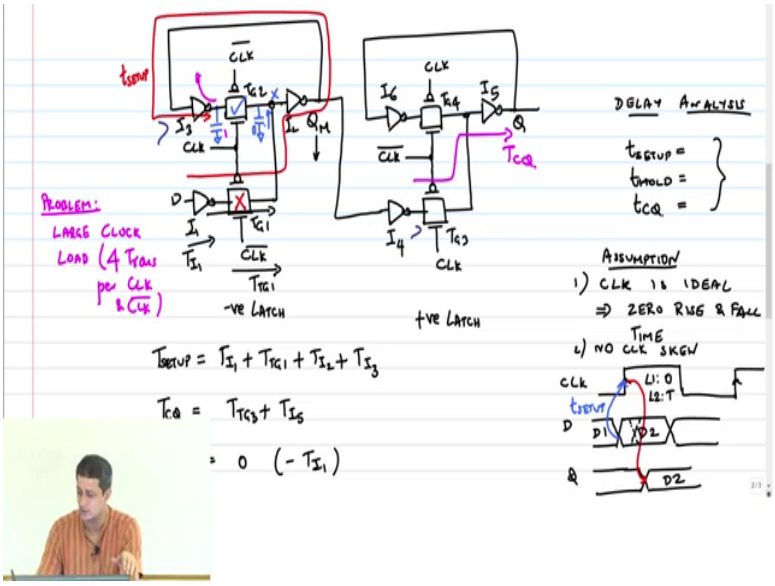

Now, what is the problem with this kind of a implement Circuit Implementation, right. So, you look at the clock, how many transistors is in driving clock and clock bar separately.

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4 each right and so, you look at the right problem large clock load, right. At least 4 transistors, right. 1 2 3 4, 4 transistors per clock and clock bar. Now you how many flops will you have in

your chip? They would have a huge number of them, right. In a million gates, you could have we have a billion transistors, you could have something like you know half a million clocks because ultimately in order to probe a digital systems for digital testability, you will put what is known as scan flop, right.

So, I do not have time to talk about that, but these scan flops are going to be large in number. That is the only way you can test the internals of your circuit because of that the load is very high and therefore, this is not a great architecture.

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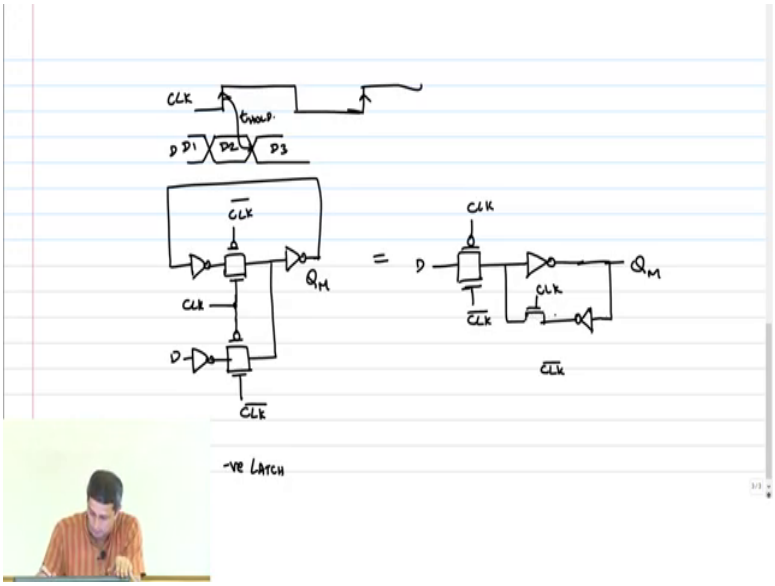

So, we want to get rid of transistors on the clock, ok. So, how do we do that? Now let me just draw only a latch, ok here. Let me see the great this is the latch. So, this I can first of all redraw little bit for some you know this to get a better understanding. This is my D. I am

going to call this as clock clock bar, right and the output here is going to go through an inverter, right and clock clock bar and no wait.

So, this is makes sense topological the same thing, right. This is my QM, ok. Now in order to get rid of this you know load what do I do technically I can remove this I know it has some problem, but we will come to that ok.

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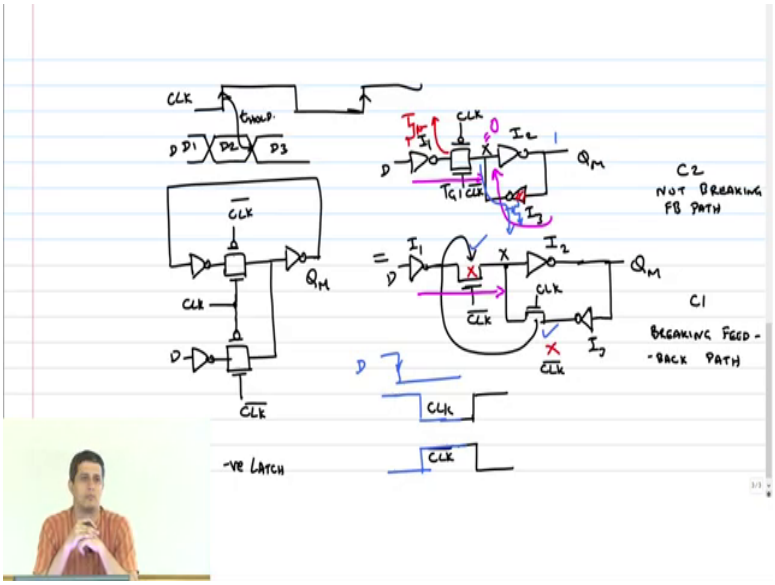

Obviously I will get rid of the PMOS transistor because that is going to be larger. In general I will only use transmission gate, I will use an NMOS pass transistor in order to make this latch. Clearly this has obvious problems in the sense I cannot pass a one right, but passing a one is not that bad because now remember this the feedback path right. So, as long as the capacitor can be charged above the trip point of this inverters ok.

What are the inverters by the way? We had I had one more inverter here, right. Sorry D, this is I 1, this is I 2 and this is I 3, ok. As long as this node here node x can be charged about the trip point of I 2, there is no problem right because then the feedback path will take care of keeping that value, right. Charging discharging to 0 is never a problem. NMOS can discharge all the way to 0.

So, there is no issue here right, but of course remember that when you are trying to charge using an NMOS transistor on this charge to a capacitor to VDD it is not just the fact that it can go only up to V DD minus V T. It starts charging slower and slower as the capacitor charges. Why? Because the V gs is the source is actually a capacitor node which is charging up there for V gs keeps dropping with time which means it is an asymptotic process. It will take forever. It is a very slow process, right.

Therefore, you can do one more thing right namely get rid of this transistor and put it as a PMOS transistor back here. Only you can do that fine. So, let me draw that separately here D QM I 1 I 2 I 3 and now there is only one transcription gate T g 1, ok. So, the difference between these two topologies or configurations is that in the feedback path right, I have removed that multiplexer select line right. So, now I can ask you a question. Do the sizes of these transistors matter?

Let say I 2 and I 3 matter in order for the flop to function correctly. Sizes of I 2 and I 3 transistors do they matter in order for my transistor, I mean flop the function correctly. Forget about timing set up. Time can be large bad. I do not care functionality wise in the sense if I want to sample data, I should be able to flip a node, I should be able to flip QM, right. That is what writing means you are flipping the data. Can I do that unconditionally irrespective of the sizes in both cases, ok?.

So, let us look at what happens. Suppose I want to write data into this configure. I will call this configuration C 1, this is C 2, ok. I want to write data into C 1. My assumption is what my assumption is very simple. I am going to assume the clock and clock bar are

instantaneous. Clock clock bar instantaneous knows Q. So, the moment I want to write data into x, my clock goes high, clock bar goes low thereby turning off this path, right.

It is cutting off that path and it is going to turn on this gap, correct. So, where am I what is happening when the clock goes 0 here and clock bar was 1 exactly the opposite happened, right. This is on and this is off. So, node x is being driven by how many gates? I 1 and through that transmission pass transistor NMOS transistor right, this is the; this is the only path which is driving mode x.

Therefore, sizes of I 2 and I 3 do not matter. I can make them unit size inverters and still it will function correctly delay maybe, ok. Now consider case the configuration C 2 when my clock is low, clock bar is high, right. So, where is this? I need to label it correctly right. So, this is clock bar clock and this is my node x. Now when the latch is transparent that is clock is 0, clock bar is 1, how many gates are driving node?

X 1 and I 3 clearly this guy is driving node x and so is this right. So, let us say that this node x is equal to 0 and I am trying to write a how is that node being going down to 0? So, what I am saying is consider this case where my clock is 0 before I. So, what I am saying is consider this case latch is now opaque data has stabilized to some value. I want to write a 1 D has become 1, right.

So, therefore my D has become 1 like this. What was the initial value inside for QM to be I mean if D was if the internal node was x, x was 0, right. That means, this guy earlier was 1, correct. 0 1 and I am trying to flip that data ok. So, therefore sorry my data has to fall that is what I was a bit confused about.

Internal node is 0 when the clock was high, when the latch was opaque. Now the latch is going to become transparent and I want to flip that data right. That means, my data has to fall, so that node x has to go high correct. So, when the latch was opaque, node x was being driven by which grade I 3. So, in order for that x to be 0 there was a pull down transistor of I 3 which was bringing it down to 0, correct.

Now at when the clock now goes low right and the latch becomes transparent, how many gates are driving node x, I 3 and I 1 but I 1 is now driving it high because data is gone low correct. So, therefore this guy is going to drive it through PMOS transistor like this high which amongst these two should win. Now I 1 should win because I want the data to flip.

That means the PMOS transistor should be stronger than might cool down NMOS transistor very lightly, but that is why if you see I will deliberately drawn this filter a little smaller in size, ok. So, you need this in order to get the functionality right and as the as it is very evident, this style of latch is basically classified as breaking feedback path and this is not breaking it, not breaking feedback path.

They issue with the latches not breaking feedback path is you might design it, you might see the width subset, the PMOS transistor right and by the way this holds even for the other polarity. If node x has a 1 and I want to flip it to 0, then the NMOS of I 1 should be stronger than the PMOS of I 3 has to hold both ways. So, in general I 1 should be much stronger than I 3.

So, you design it with some wits and make sure that it is stronger right, but you can ensure this only under some process conditions. Now when you manufacture it and across a million dyes that you manufacture it may so happen that in one of the chips it just so happens that let us say the V T of I 3 drops significantly and the VT of I 1 goes up significantly random due to random variations.

In that case it could happen that this flop may fail because you will not be able to flip the data that stronger assumption break stock. So, if you want to be absolutely sure, then you have to do this breaking feedback configuration, but of course that has a problem of you need more transistors, ok.

But otherwise if you can if you are sure that I have you know you can size it up, you can throw in more transistors leave enough area and all that, then there is no problem. You can even use the not by not breaking the feedback path, you can manage your flop defect ok.

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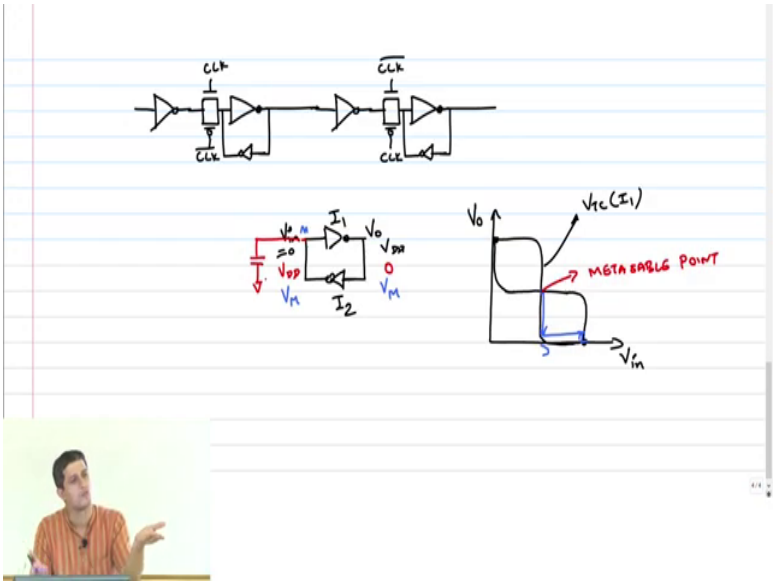

Just a quick thing to wind up this. So, if you look at this feedback path here let us say this is V in, this is V out ok. So, if I plot V out versus V in right, then you get the voltage transfer characteristics are I 1 I 2, right. This is V Ts of I 1. Now on the same thing I have to plot the VTC of I 2. What I want to now find out this what are the stable points on this in such a configuration where is it that I am guaranteed that the output will be stable always, ok.

So, now which means that there is a relationship between V in and V out because of I 1 and V out and me in because of I 2 and all of these constraints have to be satisfied. I will do only then it will be stable right. So, like for example if I put three of them in a feedback path like this, if you keep oscillating that is the ring oscillator. So, therefore I do not have a stable point at all.

Here I am trying to see because there are two of them, it seems like there is a stable point I am trying to see what the stable points are, ok. So, to analyze that you plot V out versus V in for I 1 which is of course obvious for us V out is now becoming the input of the other gate and V in is becoming the output of I 2. Therefore, you have to now plot this in this particular way right, ok.

So, what are the stable points? I have to ensure that the combination of V in V out is consistent across all of them. So, clearly V equal to 0, then this will be V DD. If that is V DD, then this will be 0 for I 2. So, therefore that is one stable point right. Similarly this guy if V in equal to V DD right, this is V DD then this will be 0. No problem, the feedback path is perfectly consistent, right.

What about this point in between that also seems to be correcting. So, for example if this is VM let us say that trip point is VM right, then the output can also be VM. V in equal to V out equal to VM, that is what that we defined it. So, if this is VM output is VM, if that is VM, this is also VM. So, is this another stable point why?.

Exactly, if even a small noise comes on this node right, then what will happen V in is now shifting by some positive value ok. That means, what will happen to V out, it will switch to a large what will V out reduce or increase radius because the gain at VM, V in equal to V out is equal to VM is a large negative value. That means, V out will come and sort of settle somewhere where here it was if B in increases a little bit, then V out will come somewhere here right. V out has to drop.

So, this will fall like this. Now further look at the other inverter V out has draw, right. So, therefore what will happen to the V in there the output of that inverter it will increase. So, that means this will go somewhere here right. So, within like 2-3 steps if you go and settle like V DD, similarly on the other side of noise is negative within 2-3 steps and go and settle at 0.

Therefore, that point is not a stable point of operation. It is known as a point of metastability, ok. This is a point of metastable point. Basically the only way to come out of metastability is

for noise to come and help you out right and that time is actually random, it can take arbitrary amount of time for a flop to come out in metastability.

So, you have to ensure that the flop also does not go in there, ok. That can be a problem because this time is now random, ok. So, to one in one over too much beyond this in this course that is a separate topic of study, but you need to know that this can be a problem in flop designs, ok, point of metastability and how to come out come out of it, what case will it go to VM.

Let us say that I have I have a node here and I have a tri state inverter on driving this node 2, tri state inverters and both I tri state invertors happened to be switched off for a short while, then this capacitor value will be somewhere in between that can come and settle at VM, right or you have a floating node. Basically floating nodes are very dangerous because some capacitive coupling can bump it up and then it will just remain there, then this guy will go in the metastability. That is all then the feedback should take of so.