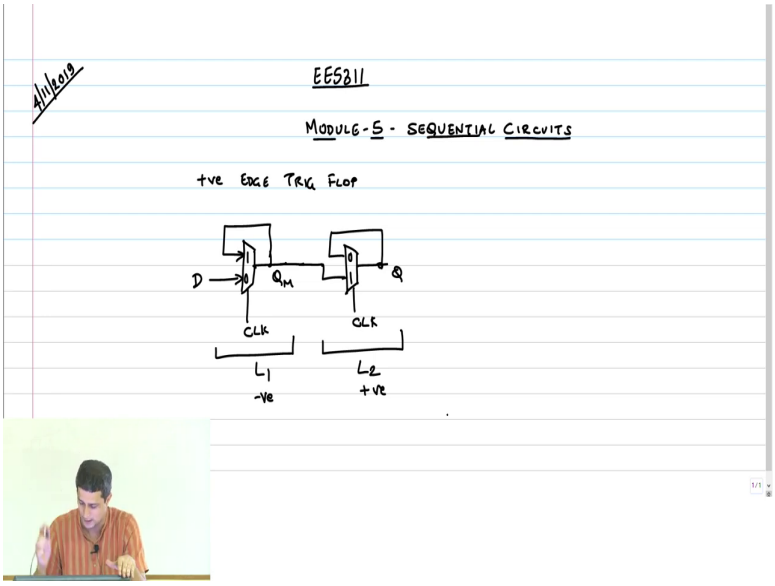
Digital IC Design
Prof. Janakiraman Viraraghavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 69
Flop Timing Parameters

(Refer Slide Time: 00:27)

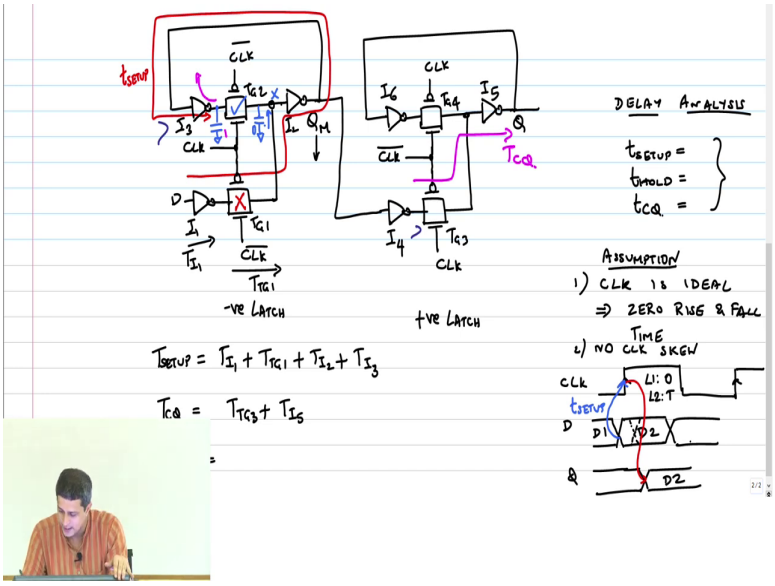


So, let us move on with our discussion and in the last class we discussed the construction of a master slave flip flop, right. Using two latches in order to get a positive edge triggered flop we said you need it to, right. So, clock we needed a negative latch first which means that this has to be 0, this has to be 1, D can go out to QM, right.

This is my latch L 1 and then we have another mux here and Q and this is what again this is clock and then, I am going to call this 0 1 right. So, this is L 2, this is a negative latch, this is a positive latch ok. So, the key idea was data that you sample on the positive edge should be

held for the entire period of the clock. So, it is being held in two stack in two steps. The first half data is being held by the L 1 where L 2 is transparent, second half L 2 is opaque and it is holding the data and L 1 becomes transparent, ok.

(Refer Slide Time: 02:30)



This is how we analyze this. We look at the timing diagram of how a change in the data you know even after the rising edge after the sampling edge data can go through till QM the first output, but cannot go beyond that because L 2 is then opaque right. So, you have to get used to these timing diagrams and also analyzing which latch is opaque or transparent ok.

That is very key to analyzing all the other timing constraints also which we will discuss going forward, right. Then we started looking at a particular circuit implementation of this flop, and we said that let me call this. So, the this is D and clock equal to 1, it has to go through right.

So, no clock equal to 0, it has to go to right that basically a negative latch clock equal to 0 clock and we constructed another to get like this clock bar, and then we said that you cannot just have transmission gates because in order if I ask you the question saying suppose I had a let me just explain that once more because there was a question last time right, do you connect this like this QM and D.

Suppose I ask you the question what is the; what is the delay of this flop set up time or what is the C to 1 delay right, then you will ask me other question saying what is driving this flop because right now there is no path to V DD or ground for this flop on both sides right, on the D side as well as the feedback side. So, there is no way that I can tell you the delay or characterize this flop.

What does characterization mean? It means that as a standard cell designer I design a gate or a flop and then, I in your assignment. Now you are characterizing the delay of a adder against the loads against the skew. What are you doing? You are basically saying you can load is this much and the delay is this number. I should be able to give you that number that is what is known as characterization, right.

Here when I try to characterize I need to know where this flop has been placed. Without that I cannot tell you and therefore, I cannot design a standard cell element like this. Some special places you are free to go and place this you know circuit as it is and you get it to work, but in order to characterize it, I need to drive it through inverters right, so that I can tell you exactly what the delays are.

Any questions? This is clock and why? No we need a negative latch here because I am going to construct the positive edge triggered clock now, ok. This is a negative latch. So, I am going to now put inverters here and what do I do? I said put one more inverter here, right.

And this was my QM, ok. So, then I just copy this again ok. I will place it here and I am going to now make the connection, so that I can construct my flop. This has to now become a positive latch. So, what are the changes I had to make here? Clock and clock bar, this will

become clock bar, this will become clock right. And where should QM go? It should basically go to the D connection here, right.

Remember that you can do this wire or only at the output of a transmission gate, ok. So, clear? Now let us try to analyze what we set up the whole time and the clock ticking delays are of this flop, ok. So, let us do the delay analysis. I want to calculate T set up T hold right and TCQ we will come to contamination in propagation delay later, ok. Let us not worry about that part now, ok. I want to calculate these numbers ok.

Now in order to do this we have to first make some assumptions on the clock edge ok. The first assumption we are going to make is function one clock is ideal. What does this mean? It implies 0 rise and fall time which means as opposed to what I drew earlier, the clock will now appear like this ok. So, of course if the clock edge is very fast, then because of capacitive coupling across this that node can you know flip and all. Do not worry about that. We are assuming that those non-idealities do not exist at this point T ok.

Now capacitive coupling this way sorry, ok. So, we are assuming that the clock is ideal and then we are going to do our analysis, ok. How to do the characterization of setup whole time and clock if you delay for a realistic scenario? I will discuss later the simulation part. I will discuss later.

So, this is my sampling edge ok. So, let us now look at T setup. What is setup time? It is basically the time before the clock edge right when data should have stabilized in order to be sampled correctly ok. This is my clock, this is my D. The data switches from D 1 to D 2 and you want D 2 to be captured right. My Q should look like this, this should be D 2, ok.

So, what are we trying to do? We are trying to move this particular edge T set up closer and closer and closer and then we are going to see when that data will not get captured at what point will D2 not get captured. That is what we are going to theoretically first analyze, ok. So, for that let me label these inverters. I 1 TG 1 TG 2 transmission gate 2 I 2 and I 3, ok.

This is you know let me call it I 4 TG 3 TG 4 I 5 and I 6. I am going to evaluate all these three quantities in terms of the delay of these gates inverters and trans meter gates,. So, now what happens first of all when the clock goes from 0 to 1, tell me what is the state of L 1 in terms of whether it is transparent or opaque?.

Clock is going high, sorry L 1 is opaque and L 2 is transparent, right. So, in order for the change of D 1 to D 2 to be captured some signals have to settle to the right value, so that when I cut this guy off, when I cut the guy off right and make it opaque when I cut the path to the and make N 1 opaque, my latch should have captured the right value and then it should hold it for the half-side. That is the idea, ok.

So, what do you think should happen like for example, is the set up time just a delay of this inverter, ok. This is the delay of the inverter plus, this transmission gate TI 1 TTG 1. So, what should happen eventually what is it that what is the node that should settle to the right value QM, right. This QM suit sample D 2 and should have settled the settle to the correct value.

When my clock edge instantaneously rises and shuts off this path thereby turning on this guy, what are the gates that are going to drive QM. I 3 TG to I 1 I 2 sorry I 2, right. So, now when my clock turns off and it turns on this feedback path what you want to ensure is that the feedback path is holding the light value right which means that if I can ensure that this capacitor here and this capacitor here are holding the same value, remember this is a theoretical called experiment, ok. Practically it looks slightly different. We will come to that.

If these two capacitors are holding the same value, then when my transmission gate TG 2 turns on those two capacitors will charge share right and you will come to some value where we both of them are the same value, then it is going to remain at that logic value. For example, if this stored 0 theoretically and this stored off 1, then when my transmission gate TG 2 turns on at the positive edge just after the positive edge, this 1 and 0 will charge share right and now there is going to be a fighting between this 1 and 0, right.

So, if this guy is 1 how is he being held at 1 which gate is doing it I 3? So, there is a PMOS transistor driving this to 1, there is a NMOS transistor driving this to 0, right. Driving this to 0 these two will fight and come to some in between value which I do not know right. It depends on the stripe strength, it depends on noise, it depends on so many things. So, to be safe if I can guarantee that both these capacitors have the same voltage, then I am sure that even after the transmission gate TG 2 turns all the voltage will not change because there is no fighting.

Now, both of them are part of the same thing right. By the way sorry this guy is not being driven down that is wrong. This is a capacitor on the gate. So, that is sort of floating. I was wrong there. That is not being driven to the ground because that is an input of an inverter, it is a capacitor that is floating and ground. That means, when this transmission gate TG 2 turns on and that has a logic 1 up there, that is going to charge this capacitor up now right. It is going to charge this capacitor.

So, this capacitor will start rising slowly and instead of storing 0 or 1, it may come to some in between value depending on where this voltage even to the settle. This node voltage x if x is below the trip of trip point of I 2, then it will end up being 0. If its above the trip point, it will end up being 1.

So, there is a sense of random necessary which we do not want ok. What we want is both these capacitors to store the same value. How do I ensure that? What is what are the delays that are incurred in this process I 1 TG 1? It has to go through I 2 and also I 3, right. Are you with me here?.

So, what will happen that set up time basically has to go through this path, this has to be my setup, this is an upper bound. If you ensure that by this time it settles, you are guaranteed that the correct datas point will be sampled. Now in reality the clock the clocks may be non-ideal. You know this it is not necessary that these two capacitors should always you know land up at a voltage which is wrong, it may land up at the right voltage also because it depends on the trip point of I 2, right.

So, it may be fine, it depends on that feedback path and all that. So, therefore in reality I will tell you how to do this characterization, but what we are doing now is a theoretical experiment, hot experiment and if you ensure that the data settles by this time you are 100 percent guaranteed that the data will be captured correctly, ok. So, therefore T set up I am going to now call it I am going to write it out as T of I 1 plus T of TG 1 plus TI 2 plus TI 3, right. Now I will ask you the next question. What is clock took you delay?.

First of all what is the clock took you delay defined as after the clock goes high, how long does the data take to appear at the output cube right. So, remember by imposing a set up time constraint we have ensured that the data has settled even the intermediate node somewhere to some value to the right value. So, all we have to see is how long does it take for data to propagate from the intermediate node to the output correctly after the clock goes high. Remember now the clock has gone high which means L 1 is opaque, L 2 is transparent, right.

So, what do you think will be the I 4 plus TG 3, ok. So, you are saying that this is that right now we do not have to worry about feedback path because this is l L 2 is transparent, they are nothing to worry about there. I asked you once more are you sure this is correct? TG 2 no, but see so what we have done is this guy had a voltage input voltage across to those another voltage both are same.

Now the feedback is switching which means that the feedback loop had some value. Nothing is changing there. Sorry that is a point you do not need I 4 because my signal has already propagated through I 2 remember right. You see how the signal is coming? It is basically coming in like when it traces this path and comes here by the time, the signal goes all around like this. The signal would have also gone here, therefore I 4 is not needed right.

So, let me take this off I 4 is not needed. So, therefore the clock to Q delay is only this much. So, what is TCQ? It is TTG 3 plus I 5. You need to be consistent about this. If you have said that the set up time is come all the way to I 3, then obviously I 4 will be out of the picture, ok. You have to ensure this because sometimes in some configurations I am even if you say that the set up time is does not include I 3.

Let us say then in that case your TCQ should be include I 4. You understand ultimately the setup plus TCQ should take your data from input to output fully that you have to ensure you are doing correctly because the reality is both TCQ and T setup are actually some numbers which are in between this total delay.

If you add these two numbers, there is some sort of a constant that comes in. We look at it later ok. So, this is just a thought experiment, but please be consistent ok. Any questions here? Correct that is the other thing. That is the assumption that I will write here. No clocks cube absolutely which means the moment clock is going high, clock bar will go low.

That is the assumption and reality is not true. There will be a slight delay because some there will either you are generating clock and clock bar separately and then doing the distribution or you locally generate clock bar which means again there is going to be a delay, right. So, this is also an assumption clear right. What about Whole Time?.

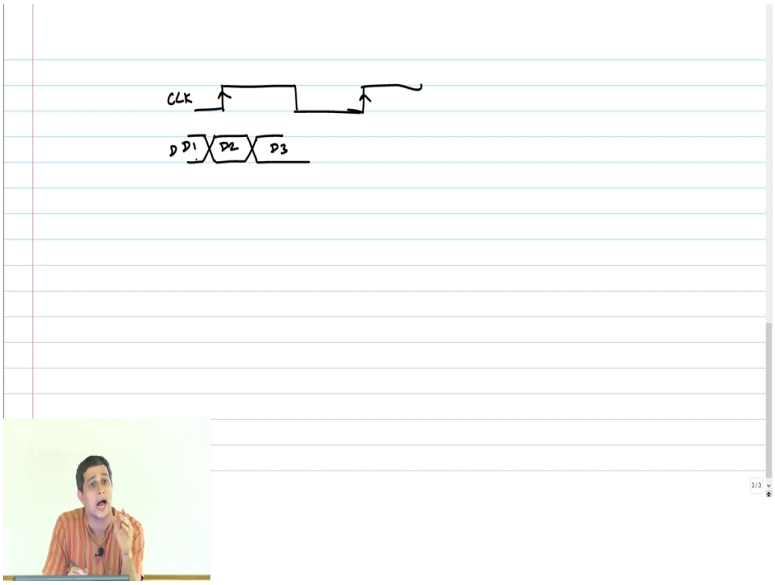
Now, what is whole time right? Let us say my D 2 chains here ok. I want D 2 to be captured that is my aim right. D 2 change before the clock edge and it changed after the clock edge as well the sampling edge, but I want B 2 to be captured and retained that the output to the entire time period in orders of that to happen. I should ensure that even if B 2 changes after the clock edge, it is still captured appropriately if it changes after some time right.

So, for example if I bring this edge very very close here, then I cannot guarantee the D 2 will be captured in reality. Theoretically we will see. So, now again tell me what is going to happen when my clock goes high and how do you think a change in D 2 cannot you know just slip inside and get into Q L because if your chain goes into Q M, then I cannot be guaranteed that the feedback you will not capture that value. There is some randomness because remember after that L 2 is becoming transparent.

So, whatever is at QM will just go through depending on the feedback loop. Of course, there is that constraint, but I cannot guarantee anything once because that is the there is some

randomness there. So, clock is shutting off my TG 1 turning on TG 2, what do you think the whole time is how long? Should I hold my data.

(Refer Slide Time: 25:59)



So, what is Whole time? Whole time is definition is data is clock right B I caused a change in data before and after the edge D1 D2 D3. The point now is before the edge when the change happens, I want that change to be captured that is setup time, the change that is happening after the sampling edge. I do not want the edge to be captured, I want that to miss. I wanted to retain D2 all three all through right.

So, the point is this change is T hold in the sense if it changes far away from the edge, then D2 will be captured. There is no problem. The change to D2 will be ignored if you bring it very close that minimum time after the clock edge where a change in D will not go through this we find that the whole time, ok.

So, that is what I am trying to analyze here again under these theoretical conditions under the assumptions we have made. So, if my clock edge first of all changes let us say and the changes after that what is the minimum time that leads to even arrive at the transmission gate I 1 right. So, if my clock shuts off at 0, then actually there is one inverter to further delay the change in B, right.

So, actually the whole time is negative D can change immediately after the clock edge under these theoretical assumptions that you have made. Clock is in instantaneous no skew and all that the moment you introduce Q, you will see there is a problem. We will look at that later, but right now there is negative whole time or safely you can define this as 0's.