Digital IC Design
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Lecture – 68

Master Slave Flip Flop

So, let us get going here with the discussion on sequential circuits.

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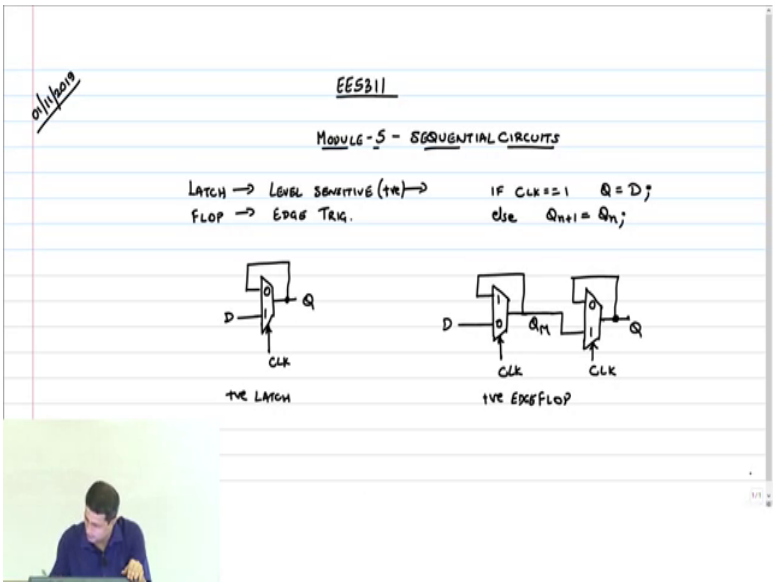

So, last class we were discussing the idea of a latch and a flop; a flip flop is also called a flop right. So, this is level sensitive and this is edge triggered ok. So, the we also discussed one very simple implementation of a latch which is using a multiplexer, right. So, if you look at the latch if right and by default its a positive its sensitive to the positive cycle of the clock.

So, if clock equal to equal to 1 then Q equal to D; else Q n plus 1 equals Q n hold the state, right. So, we said that we can implement this very easily with a multiplexer. And if you want a positive latch, then what you have to do is you have to allow D to go through when clock is 1 and this is 0 ok. So, using this we now want to construct a flop which is going to be edge triggered ok. So, we will see how we can do that.

So, if this is a latch and its a positive latch then the basic idea is you cascade two latches ok, let me call this Q M clock clock ok, I am going to call this clock also (Refer Time: 02:44) still the 1 and 0 here correctly for the mux, this is Q ok, this is a flop. And I want it to be positive edge triggered flop ok.

So, now, the question is what kind of a latch should I put in the first stage, what kind of latch should I put in the second stage. Negative in the first stage and positive; so 0 1 1 0 correct. So, what we will do is we will draw a; so we (Refer Time: 05:49), select this.

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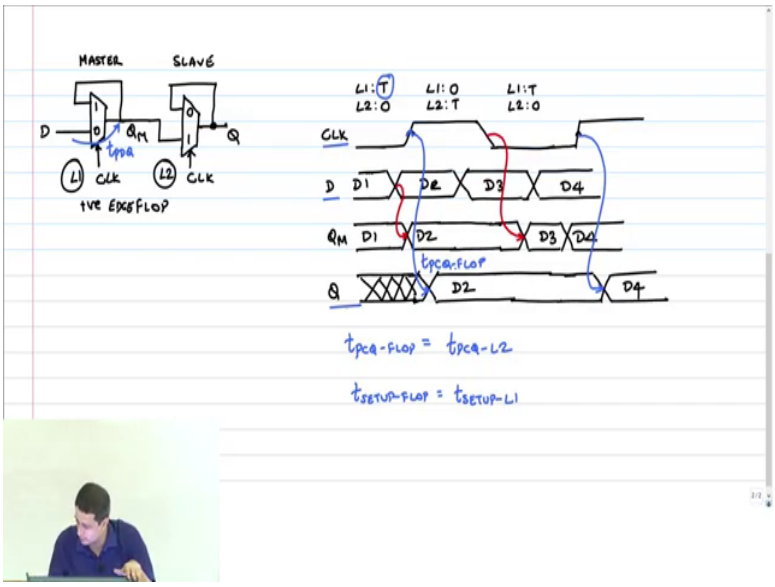

So we will sketch a timing diagram to understand how this actually works ok. Why we should put a negative latch in the first stage and a positive latch in the second stage right. So, by the way this is called the master stage and this is called a slave stage ok. So, let us assume my clock is like this ok. And my B as usual makes some transitions before the clock after the clock and so on ok. I will make some transitions here. So, this is D 1, D 2, D 3, D 4.

So now, what happens when the clock is 0 here, ok. This is let me call this latch L 1 L 2 ok; latch L 1 and latch L 2. So, first of all in each phase of the clock when clock is 0 tell me if L 1 is transparent or opaque; L 1 is, when clock is 0 it is a negative latch. So, clock data has to go through. So, therefore, it is going to be transparent. L 2 will be opaque, its a positive latch right. So, positive latch means in the negative cycle is opaque data cannot go through.

Similarly here L 1 L 2; what is happening here? Its reverse opaque and transparent; transparent L 2 is opaque and this continues. So, what we want to now see is how is it that we are able to put two level sensitive latches and still make it an edge triggered flop ok. So, let us see what happens to D 1? D 1 is you know changing in the 0 cycle, during which L 1 is transparent. That means, any change in D will go through a percolate to Q M right, to the output of this.

So, Q M we can safely say is this is D and this clock is D 1. It may have happened at some delay, but given that D 1 has settled already, this is going to be D 1 ok. Now, the D D makes a change to D 2 before the clock edge ok. So, what is the sampling edge for L 1? If its a negative latch then its the positive edge that going to be the. So therefore, if D 1 switches to D 2 at least a set of time before the clock edge then this sampling will happen properly, right.

So, which means that I am not going to worry about the contamination delay right now, I am just going to make it like this D 2. Q M will now change to D 2. What happens to the change of D 2 to D 3 for L 1? It will remain because now L 1 has become opaque right. And therefore, it is going to keep D 2 all the way until L 1 becomes transparent again in the 0 cycle.

So therefore, here you will see a change to D 3 right. And you know there are obvious things where if D 1 changes here this is the edge this is the transition that is triggering the changing Q M, right. Because L 1 is transparent, change in D goes out to Q M. On the other hand when the clock goes low that is when the clock the L 1 becomes transparent and therefore this is the thing that will trigger a transition to D 3, right. They are consistent to here. Now, we have to see what happens to Q M ok.

So, in the 0 cycle what was the state of L 2? It was opaque right. So that means, is holding some state so we do not know what it is. So, that is why we said remember that this thing we do not know what it is ok; we do not know what the state is; its an unknown state. Now the clock is going high and therefore L 2 is becoming transparent and L 1 has become opaque, right.

But Q M has already sampled D 2. The latch L 1 has already sampled the data that you wanted and it is holding it through the positive cycle at which point L 2 is now becoming transparent. And therefore, the change in D 2 this thing D 2 will go out ok.

Which amongst the change in Q M or D or clock which one is triggering this switch to D 2? Its a clock, because the clock is now switching and making L 2 transparent it goes opaque till now. That is why this is happening. The delay is basically whatever t pc Q or whatever right we will come to that. Now what happens to the chains that in of Q M from D 2 to D 3? L 1 is transparent but L 2 is opaque, the moment the clock goes low L 2 becomes opaque and therefore it is going to retain the state.

What is that state? D 2. So, its going to simply retain D 2 all the way to clear. And eventually you will see the same thing because now D 3 has changed, of course L 1 is transparent. So, therefore, you will find a change no. So, Q M it changes to D 3, but then it will also switch to D 4, right. That is right; D 4 ok, From very I can use the (Refer Time: 12:23).

So, assuming that happens then at this edge again you will find that it switches to D 4 successfully, right. And so, what you see for a flop is basically only clock D and Q M sorry, Q you do not see Q M. And that is why all the changes are happening with respect to the clock edge right.

So, now let me just ask you a question what is t PCQ of the latch, I mean of the flop. Assume that the latch has some parameters: this is t CCQ t PCQ and all that. What is t PCQ of the flop? You agree that this this delay is nothing but t PCQ of the flop right let me call it flop. What is that delay? Q of the; in terms of the latch delay component. Exactly, it is t PCQ of L 2; is just how long it takes for data to go from input off from the clock going high and making L 2 transparent to the data being available at the output of L 2, right.

What is t setup of the flop: t setup of the flops on similar lines? Setup of L 1 ok. So, basically what is happening is L 1 and L 2 are operating alternately in this transparent and opaque mode and achieving this edge trigger business for you, right. Because L 1 is transparent;

basically if you have a sample on the positive edge then the first latch should be transparent in that previous cycle, that is when the clock is 0 only then you can sample and then hold that data, right.

So, clearly the slave stage does nothing, it basically just takes the sampled output at Q M and just take holds it for the remaining part, ok. So, if you look at what is happening in this D 2 right, L 1 is actually transparent correct L 1 no L 1s opaque L 2 is transparent. So, what is happening is your Q M is being held for half the cycle, in the other half it is Q that is being held.

Ultimately you want a flop to hold the data to the entire clock cycle. How is that achieved? That achieved by holding the data on L 1 for half the cycle and holding the data on L 2 for the other half. When the data is being held on L 1 the slave is transparent right. And therefore, data just goes through, correct. When L 1 is opaque it will hold mode L 2 is transparent or allowing the data to go through.

So, L 1 is holding the data for the positive half cycle, L 2 is holding the data for the negative half cycle. And that is how you achieved edge triggering with two level sensitive latches, ok. Any questions here? So, now you this look at it what is the set up time of the flop?.

Basically, the data has to change before that sampling edge right. What is the sampling edge? It is basically this positive edge here which flop is sampling the data there or which latch is sampling the data it is L 1. See L 1 is transparent here, then L 1 becoming opaque. Now L 1 is sampling the data and holding it.

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Y t PD; y t PDQ.

Student: (Refer Time: 18:04).

So, PDQ is of the first latch; t PDQ is basically this delay right this t PDQ; is not it ok.

Student: (Refer Time: 18:36).

So we will come to this. We will see where the origin of this set up time itself is; now that is nothing but some delay of the first latch ok. So, we will come back to it I will answer this question in maybe in the next class, where we look at an implementation. And then we see what needs to happen right and the origin of the set of ten first of all.

Why should I even have a non 0 (Refer Time: 19:07), once we look at that it I can answer that question more clearly. Right now I am just saying if I give you a latch with a set of time value you can express the flop set up time in terms of the set up time of the latch, and the t PCQ of the slave latch. That is all I am tend to convey here. So anyway.

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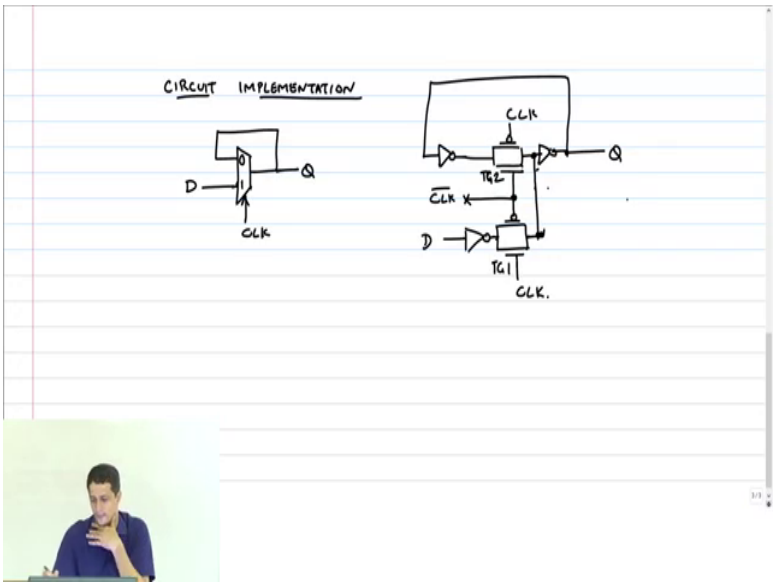

So, let us now look at some circuit implementation right. We do a very very simple picture here. We said we put a mux like this, we are going to hold the data through a feedback and the clock will be the select line ok. So, this is what let us say I want the positive latch 0 and 1.

So, how do I now implement this in circuit level? The best thing to do for a multiplexer is: what is the best circuit implementation for a multiplexer: transmission gates right, first transistor is just one NMOS on PMOS, transmission gate is a combination of that put in parallel right. So obviously, we will do this Q ok. So, this is my D. So, can you tell me what this signal here should be?.

So, will be clock or clock bar; corresponding to this latch positive latch. Clock, clock bar? When clock is 1 right we want the D 2 go through right. So, when clock is 1 this has to be 1. Therefore, that has to be clock bar and this also has to be clock, right. Clearly, we have a its a

very simple implementation. But, like I told you a transmission gate without or driving gate is meaningless, because I cannot tell you what the delay is, I need to know which guy is driving, I cannot even characterize this stuff.

If I want to say that this guy has a set up time of so much and this has a pc Q of so much then I need to know which gate is driving this in order to tell you this delay. So, that is meaningless. I need to have a standalone flop that I can just characterize, and say that these are your set up whole time and you know clock to delays go ahead and use it in circuit. For that I need to now put in inverters. So, that we can use them appropriately right.

So, what do we do? We are simply go in to break the circuit and put inverters in the path. First I put one inverter here, then. So, what do I do? I can you will does work I do not think it. So, we do this produces the output.

Student: (Refer Time: 23:54).

Loop to inverter should be there right. So, this is not a correct implementation that is right. So therefore, this is will satisfy my two inverter requirement here right and of course I can do this. No, but again this cannot be driving here it has to appear here. Because, you can wire or only the outputs of a transmission gate. So, I cannot connect this to the output to an inverter, because that will always be driving something and I cannot wire or something there.

So, the wired or connection should always happen and the output of the transmission gates. So, this is TG 1 TG 2. So, only those outputs I can wire or and the remaining (Refer Time: 25:02) So, what you can do; is if you want you can really avoid this guy and take your output here right; r q as I would call it back ok. This is a very simple circuit implementation of a positive latch with inverters and transmission gates ok. So, you are out of time.

So, in the next class on Monday we will exactly determine what the set up time and clock to two delays are for this kind of an implementation, ok. And hopefully his question also should be answered at that point ok. So, just be very careful sometimes you can get confused if you do not practice this hard enough, where like I did now you might put the connection here that

cannot happen. Remember wired or connection has to happen at the output of the transmission gate always, nowhere else.