Digital IC Design
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Lecture - 67
Time Borrowing

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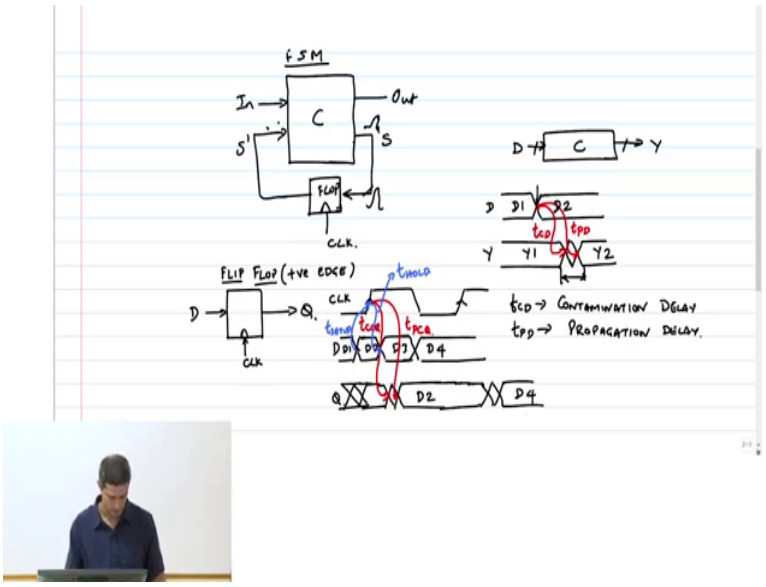

So, let us see what happens. You know we need to now very carefully define certain terms right, certain definitions for delay of various blocks right, and what we want out of these blocks. So, if I have a combinational block, I have an input D and an output Y ok. Let us assume that my input D changed at this point ok. So, this is a timing diagram that we forget used to this switch here right, this transition means data is switching from one state to another state, but both are deterministic we know what they are.

So, this will be data D 1 this will be data D 2. And the reason I am not drawing it as a binary function is this would be a bus. This also could be a bus, right. So, any change in any of the inputs is what we are capturing through this transition here, here this transition.

So, what happens is after the input changes the output will start changing at some point first. Now, this means, this region its data is going to some random transitions we do not want to pin down what the values ok. Why does this happen?

For example, when one input changes I could have some short path through my combinational block which causes one of the output to change, right. But now, another input changes and it may come and overwrite this right. There is a possibility that you will have a glitch at one of the outputs and that glitch is what we are capturing here. The issue is the glitch can affect the circuit going forward.

So, we have to make sure that the earliest change of data also we should be very careful about it. So, the earliest time at which data can change is basically called contamination delay. This we did earlier, even for land and all that we said there is a contamination delay which means the earliest smallest delay largest delay is called propagate to delay. So, this is maybe I call it to arrive t CD. This arrow mark going from here to here says that its the transition between D 1 and D 2 that caused my output Y to start changing, ok. the issue.

The reason we need to do this is later you will see in a flop based system there will be a clock that changes there also data were changes, but the output may react only to the clock not to the data. So, by putting this arrow we are actually saying it is a change in this edge or data here that caused the change in the output Y. This change here is called a propagation delay t CD. That is the latest change after which the output is guarantee to be stable. Contamination delay is the earliest time at which the output starts changing, but the data is not guarantee to be stable after that. Output stable after propagation delay ok. So, t CD is contamination delay t PD is upper case and delay ok.

This is a combinational block now we have to see what happens to a, this is called a flip flop. The word flip flop or latch or register can vary from book to book. Rabbi has a different definition, we are following what western had its is using ok. A flip flop is a sequential element as defined by what I am going to show you now ok.

Now, I have a clock that controls this D Q ok. So, what am I going to do? I have this clock that is essentially changing like this ok; D sorry this is clock D and Q. So, let us assume by default a flip flop is always a positive its trigger to flop ok, this is positive edge. That means, data will be captured on that rising edge of the clock and data will now then be stable after that ok. So, let us assume that this data changed like this.

So, it went from D 1 went to D 2 and yeah. So, by the way this one I will be call this output here as Y 2 means D 2 output has now come to Y 2 right, this will be Y 1 ok. So, let us say that the data changed from D 1 to D 2. And then it again switched to D 3 somewhere in between ok, and or I will make it more interesting. This thing makes a very quick transition D 2 D 3 and then D 4 ok.

So, what should happen? What is the expected behavior of a flop is what we are looking at? I do not know what this output is before, because I do not know what the previous state was that is what this arrow mark here means ok. So, now, at the positive edge data that it is going to sample is which one: D 2 right. So now, again the output can start switching a little early and it can settle finally to some other value, ok; the.

So, therefore, there is a contamination delay for the flops as well and a propagation delay. But the origin of these two delays are not the same as that of combinational circuits. I will come to this at a later point, its not like because if you look at a problem only one part there is one you know part of inverters or whatever like. So, there is no alternate path to actually call this contamination delay. I will tell you where this comes from ok. The question is we are trying to capture the earliest change and the latest change, fine.

So, this will settle to D 2, Q will now capture D 2 right. On what edge is D 2 reacting to? On the yeah; but what I am asking is it the change out here or is it the change here; its with respect to the clock. Therefore, my arrow mark has to start in the clock and come here, ok.

So, this is clearly called a clock to Q delay for obvious reasons ok. Therefore, I am going to call this t CCQ, t PCQ ok. C to Q the last C Q is basically clock to Q. The first letter C or P is saying its contamination or propagation delay again ok. So, what is the behavior now? Now, what happens to this change to D 3 in between? What will happen? Nothing, it should ignore right. So, this is a very important point the change even at the negative edge there should be nothing that goes through, right. So, D 2 should be captured all through ok. Now, in order for?

So, what will happen in the next edge now? It will capture D 4 yeah again you will have the similar change this and this will be D 4. Now, in order like I already told you that there is a sequential over it. And I said that you cannot have a guy placing the brick like this and other guy taking a break away. So, it has to be placed a little before. How much before? That is called set up time. So, in order for D 2 to be captured at the positive weights correctly you have to set this data up, t set up before the clock edge arrives. So, this is set up ok.

Now, after the edge, after the clock edge is done sampling edge is done D 2 should be stable for some time in order for this to go through right. This is you know this is what we call t hold. The data has to be held after the clock edge so that the data can be captured correctly. Again the origin of setup and whole time is very different and we will look at all of that later, ok. So, this is basically I will just show you that what these definitions are, right.

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Learning Objectives

- Build elementary sequential circuits like latches and flip flops - Static and Dynamic
- Identify devices that affect set up and hold time
- Derive max and min delay constraints for latch/ flip flop based pipeline systems
- Account for clock skew in a pipelined system
- Analyse time borrowing across half cycles and across cycles
- Calculate the maximum clock frequency of operation of a pipelined system

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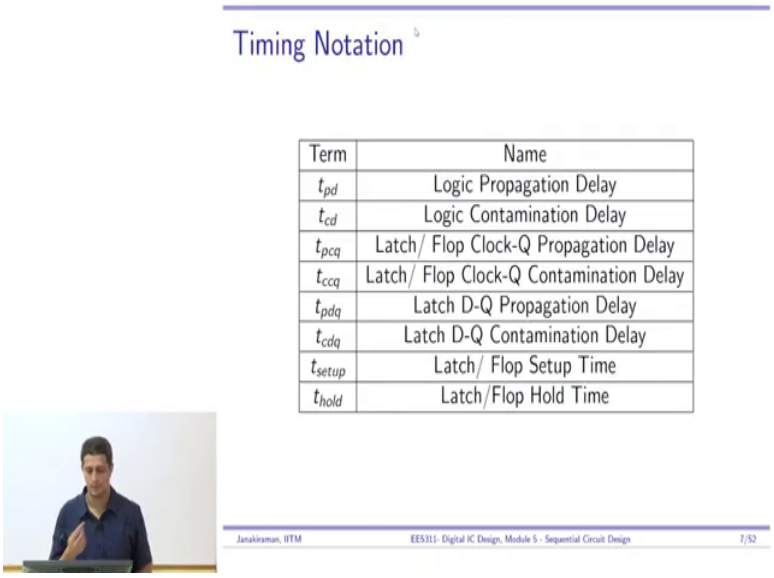

I can just I have that here, right: t pd is logic propagation delay, t cd is logic contamination delay, t pcq is for a latch or a flop I will show you what are latches clock to q propagation delay. The first p is for propagation, c to q is the clock to q t ccq again first c is contamination clock to q delay ok. And setup and hold time I just explained to you ok.

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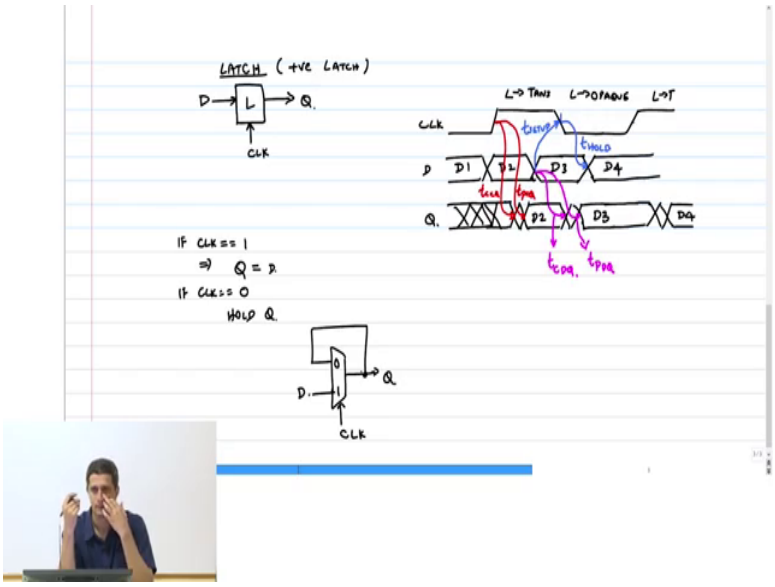

So, now we will also look at what a latch based system is ok: latch. So, I have a clock L, so if its D this is Q. A flop is h triggered a latch is level triggered right. So, in the sense this is a positive latch by default. What is positive latch mean? It means when the clock is high data can go through, the latch is transparent in the positive edge right. And therefore, I have the follow it. So, let us now do the same timing diagram that we did for the flop ok.

I am going to call some transitions here: D 1, D 2, D 3, D 4 ok, my clock D and output Q. So, we will plot the timing now for this ok. So, as usual I do not know what this state is; the negative edge forget that because we do not know what the previous state was ok. What about here? Clock has gone high and therefore D 2 should go through, correct latch becomes transparent ok.

And so, as usual you will have some curly transitions. This delay is caused by 3 is triggered by 1, by clock or data. Remember by data change before the edge, the latch was opaque at that point then it became transparent. Therefore, the delay now has to be clock to Q delay right.

So, these t CCQ and t P sorry; oh sorry correct sorry yeah. Now, there is a transition from D 2 to D 3 after the clock has gone high. What should happen to that data? It has to it has to go through and this is D 2 right. This change is now triggered by what? By data, and therefore I will have another term like this right which is t; no. The first C or P is always for contamination or propagation. So, it is CDQ and t PDQ ok.

Now, where is the setup and whole time for the latch? For a positive edge, for a positive latch what is a sampling edge? Ok. What the sampling mean in terms of transparent and opaque for a flop also. Basically, the that sequential which is going opaque at that point, data cannot go through from input to output its going to whole the state that is what it means. So, what is the sampling edge for a positive latch? If its a positive latch data can go through when the clock is high.

So, at what edge does it sample the data? Rising edge yeah, but you look at the comparison with a flop right. At what point, when I say sample it means I am sampling the data and I am going to hold it; that means, changing data after that should not be able to go through that is what I mean by sampling. I mean sample and hold, exactly. So, for a positive latch its the negative edge which is the sampling and holding edge right. So, I will not put this arrow actually I will put this arrow here, because this is my sampling edge ok. So, therefore, setup and whole time has to be defined with respect to the negative edge. This is t set up t hold ok.

So, effectively what happens is at that sampling edge D 3 will get sampled and appear at the output the change to D 4, what should happen there. It will not go through, because now the latch is opaque right. So, I will also indicate here the latch is transparent, latch is opaque right. And the change in D 4 therefore is lost. And after you come here now again the latch becomes transparent, D 4 its now still held. Therefore, at this edge you will have a change causing D 4 to even to (Refer Time: 19:40), ok.

So, let us look at the logic functionality of this, logic description of this latch; what is it? If clock equal to equal to 1 implies Y should be equal to I mean Q should be equal to D, otherwise what should you do? You hold the previous value or you just leave it actually if you are trying to write this and very long you take a leave this, right.

If I were to implement this in terms of logic gates where I have if clock equal to equal to 0 then hold Q, let us say. What is the best logic gate I can use to implementation? Mux right, a multiplexer. This is a clock, the select line is a clock if it is 1 then this is 0, this is 1, this is Q. Where should I connect D? Yeah. What should I do on the other end? Simply feed it back like this ok.

Now if I want to make a flop out of this what should I do? If I want to make a flop. So, now, this is the latch which means when the clock is high data can go through clock is no it holds, you have to just cascade two latches right. This master slave configuration that you heard of earlier. You cascade two latches, a positive latch or a negative latch and a positive latch together and you get a positive edge trigger flip flop ok. We look at that in tomorrow's class, ok

Thank you.