Digital IC Design
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Lecture - 63
Array Multiplier – Timing Analysis

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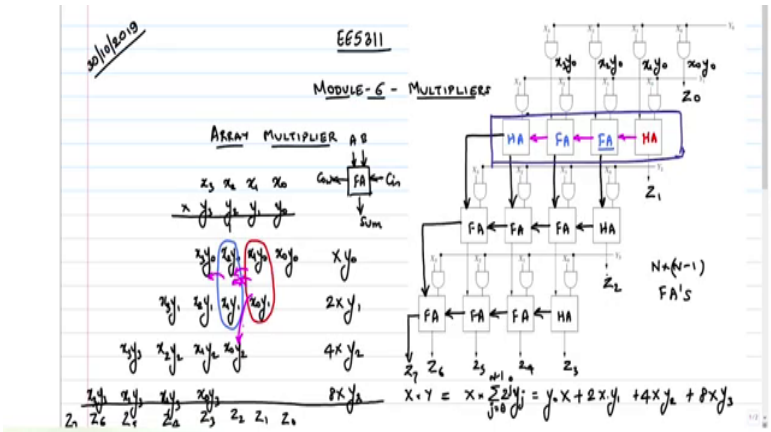

So, now let us do a timing analysis on this and see what happens ok. So, what I will do is maybe I will copy another diagram and we will do it on that.

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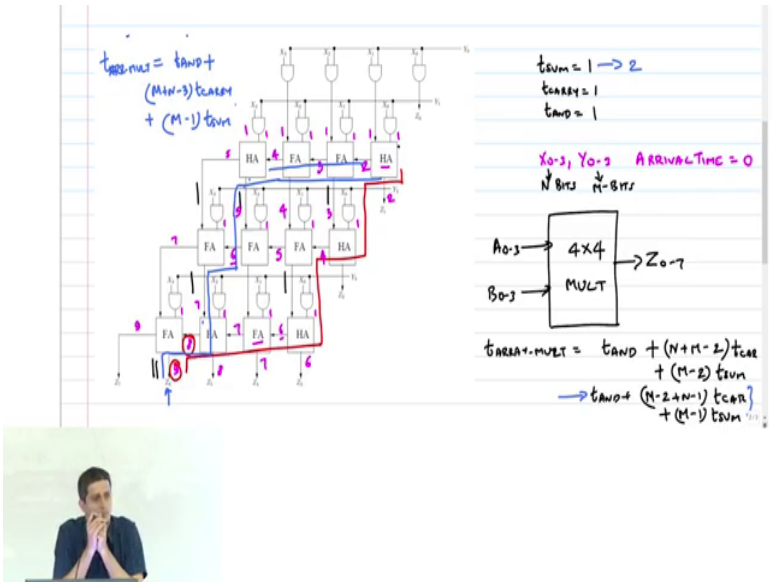

So, for simplicity now, I am going to assume the following t sum equal to 1, t carry also equal to 1 maybe we I showed you a circuit also where this can be achieved equal delay upon carry and sum ok. So now, we are going to do and of course t AND also equal to 1. So now, let us do a static timing analysis on this block and propagate these signals to the half assume everything in the full adder now ok.

So, the arrival time at the output of every AND gate, right at least the first AND gate is what actually every AND gate yeah. Because all x's and y's arrive at time 0 right, this is what is known X 0 to 3 Y 0 into 3 arrival time equal to 0. Therefore, everything will arrive at unit time here, correct. What about the; of course these AND gates also are the same, ok.

So, now the first half adder what is the arrival time for carry out? This guy, its going to be 1 plus 1, this will be 2 2 right. Full adder: the next full adder 3 and 3, 4 4, 5 5, right. Next stage:

what is this? 4, 5, 6, 7. Last stage: yeah you take max arrival time right now both input 1 and 5 5 plus 1 unit 6 6, 7 7. Now of course, the 6 6 is the same for this full adder this one A or B is arriving at 6, the carry is also arriving at 6. So, max is 6 plus 1 unit 7 right. This will be again 8 8; no this will also be what 7. So, this will be 8 8, and this will be 9 8 plus 1 correct. So, this is 6 6 plus 1 7 right and if this 8 yeah ok.

Now what is the critical path of this block? So, you got to pick the output; what are your outputs? For this multiplier block right my multiplier block 4 cross 4 mult is basically A 0 to 3 B 0 to 3 and output Z 0 to 7. Pick the output which has the maximum arrival time which one is that, Z 9 I mean Z 6 or Z 7. So, I will track this in this. Now which input has arrived last there? This guy, now which input has arrived last?

Both, right. Effectively what this is saying is there are multiple critical paths all with the same delay. So, it is impossible to sort of optimize this, because everything is equally critical. Now which one? If you want to optimize one critical path there should be another path which you can sacrifice delay on then you can optimize, but now there are multiple paths, right.

So for example, you can go like this right or you could go like this. On any other path you take right to arrive at 7 everything is similar time. So, there is nothing that you can do in order to optimize this path. So, you also notice what is happening is if you take every single stage here right, if you take a single stage as I do not know the color ok. If you take this time its basically like a ripple adder right, I am basically its rippling my carry through that stage each row I am rippling my carry through that stage correct.

So, it that is really not helping me. So now, we will come to; what he pointed out that it is really not necessary for you to ripple the carry along the same row, I need to add it right. When I do x 1 y naught I have to add it to I have to add it and get a carry and the carry needs to be propagated to the addition of and contribute to Z 2.

But it need not happen this way it can also happen this way. You add x 2 y naught x 1 y 1, and when you are adding with x naught y 2 you basically add that carry. You follow me? I need to add 3 numbers x 2 y naught x 1 y 1 x naught y 2 plus a carry that is coming from the

previous state I need to add 4 numbers that can be done in many ways. I am saying you do x 2 y naught x 1 y 1 first, then you get the sum then you add that carry.

The advantage is while x 2 y naught x 1 y naught has generated a sum that previous carry would have also got generated and the hope is this signals will arrive together, right. So, in some sense instead of adding the carry immediately you are saving the carry and adding it later, right. Therefore, the next architecture of multiplier we are going to basically call a ok.

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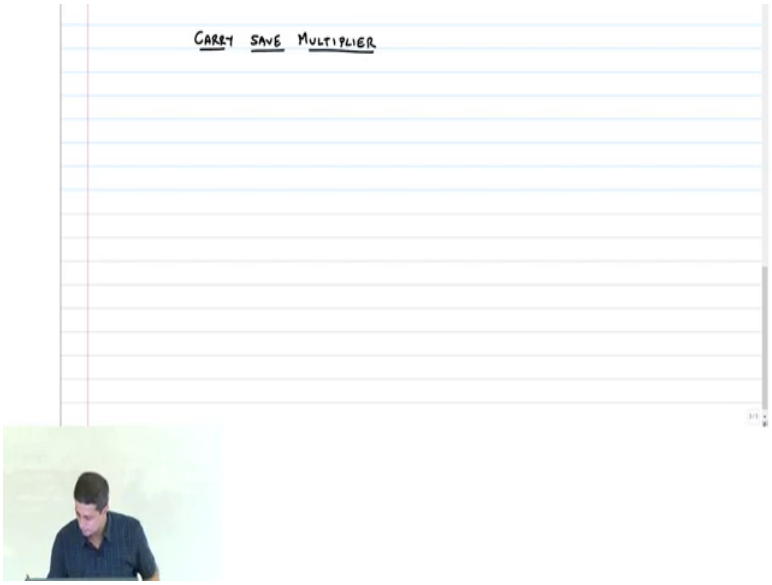

By the way, if I went to you know assume X is M bits and Y is N bits, then: what is the expression for the critical path delay of my array multiplier. Yeah. One second before I do that let me take a look if my notation is correct with M and N that what I do not remember. Sorry, X is N bits, Y is M bits I am sorry ok. So, that we do not get confused in the expressions later ok. This is M bits; N bits I am sorry N bits and this is M bits ok.

Now let us not assume t sum t carry and all that you know equal to 1 we will write it in terms of that delay ok. So, what is the delay? So, what you do is you just track this blue line here right. How many carry parts does it have to go through? No, remember this blue line ultimately has to come all the way to here. How many carry parts does it have to go through? No, if X is N bits Y is M bits, so let us write that expression the array multiple.

Of course, the first two delay is the time to generate the partial products one unit of time is needed for that which is t AND. Now it has to go through some number of sums and some number of carry's; how many of them? N plus M minus N plus M minus 2 t carry plus how many t sums; how many t sums? Basically, this is 1 t sum another t sum another t sum right. That is how many t sums yeah that is actually are carry a what I meant was this is a t sum.

So, how many how many t sums? Now we will verify this answer we know the arrival time has to be 9 right. So, we plug in these values 1 1 1 and see what we get. And then we will see where we went wrong. 1 2; I would say for 4 bits its 3 t sums right. Y ou got to go through this guy, this guy, and then this guy right. So, is this right first you substitute and see then you see for N equal to 4 M equal to 4 these and t carry are all 1. How many t carries? N plus M minus 2. So, 1, 2, 3, 4 is what I am getting here; 4 plus. Makes sense? M minus 2.

Student: (Refer Time: 14:29).

Correct ok.

Student: (Refer Time: 14:36).

M plus N minus t, ok. Now substitute and see did we get 9; we do, right ok. This seems to make sense. So, let us see if the answer matches from you know what is given in the textbook in just in case you have made a mistake.

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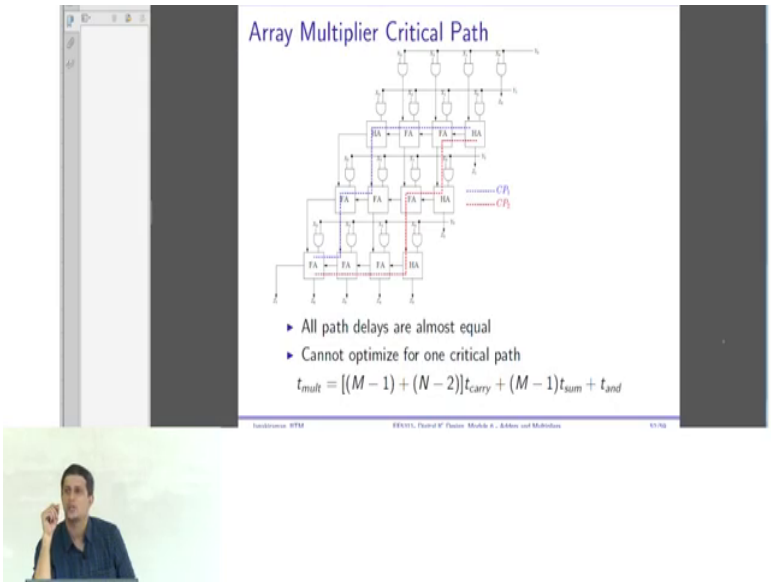

M minus 1 yeah this is what I thought; M minus 3 t carry plus M minus 1 t sum and t angle. Why did you say M minus 2?

Student: (Refer Time: 15:18).

That depends on the path, no. So, I understand that yeah it could be maybe it could be this also right; one path might be this. I think the other path is t AND plus N plus let me write it differently M minus 2 plus N minus 1 t carry plus M minus 1 t sum. I think.

Student: (Refer Time: 16:01).

Why?

Student: (Refer Time: 16:05).

No, yeah in the I agree, in the sense that this guy blue line has to go through this and then come here then it has to go here, yeah you are right yeah you are right. And then again it comes here arrival time here and then it has to go here, correct yeah. This makes sense, yes I agree with you ok.

So, basically what we are saying is there are how many t sums: 1, 2 and 3 which is M minus 1 t sums right. And the remaining are basically your carries. So, I have x being an N bit number I need to go through N minus 1 t carries and another M minus 2 t carries for the y direction, clear. So, it is just a question of counting how many carries and some 0 to go along the critical path. So therefore, I would I would think this is a more appropriate answer. Yeah

Student: (Refer Time: 17:48).

Yeah.

Student: (Refer Time: 17:52).

Correct. So, in some sense we have basically you know not representing reality perfectly here, in this arrival time picture right. So, you are right where there are mult sums that what we have to do. And in fact, if you take; so I would say you go back and work this out for if this were 2. These somewhere 2 units and t carry where 1 unit then you will find that this guy is actually the signal with most delay, because you have to wait for that sum to come out.

Then you go only along the sums, propagate it and then you can find I think this will turn out to be the right answer. Basically, I am like you said M minus 1 t sums as opposed to M minus 2 t sums is the exact answer ok. So, let me just maybe write that out again: t array multiplier is equal to t AND right plus M plus N minus 3 into t carry plus M minus 1 t sum ok.