Digital IC Design
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Lecture – 49
Pseudo NMOS Logical Effort and CVSL Logic

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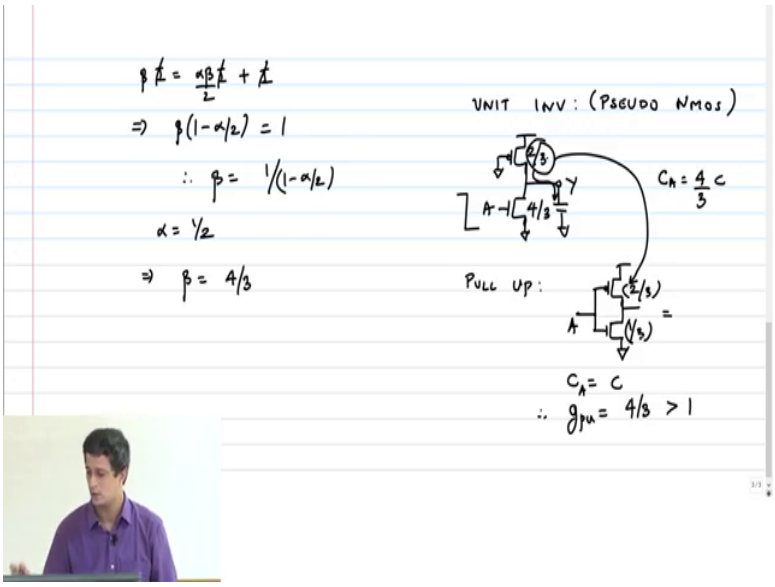

So, now I want to calculate the logical effort of this (Refer time: 00:20). So, we will first do the pull up logical effort ok. So, we will do pull up. What is the you know the load capacitor is being charged up through a PMOS transistor of size? 2 by 3. So, I first need to construct my reference static CMOS inverter of same drive strength remember that right.

Now, I am going to refine my definition I am not going to say same drive strength that can provide the same current to the load capacitor for charging or discharging. Drive strength is slightly vague. You might think it is a resistance, but because of the Pseudo P NMOS

problem where I have currents from the PMOS also. I am going to change the logical effort definition slightly to say is ratio of gate capacitance compared to a static CMOS inverter which can provide the same current to the load capacitance for charging or discharging ok.

So, therefore, here my reference inverter is the following. This is 2 by 3. Therefore, I make this 2 by 3. Now if that is 2 by 3 what should the NMOS size b 1 by 3. So, this total capacitance is equal to how much? C A. This is input A. C A is equal to how much? C. What about here? C A equals input is connected only to the NMOS transistor.

So, 4 by 3 C. Therefore, logical effort pull up is equal to how much? 4 by 3 correct. Note this is greater than 1. It is an inverter. This is just an inverter. Logical afford for pull up has gone up 4 by 3 basically because we have brought the pull ups you know the drive strength. You have brought it down you made this 2 by 3 and that is why this inverter has lower drive strength.

So, here there is no confusion because when my when the output is being pulled up it means my input fell instantaneously and therefore, the NMOS turned off. So, all the current that is coming from the supply is flowing to like this. And therefore, I said you know I can interchangeably talk about resistance and current here because the same current is flowing to load capacitor no problem. So, therefore, that 2 by 3 I replicated here constructing the NMOS size and got the logical afford as 4 by 3.

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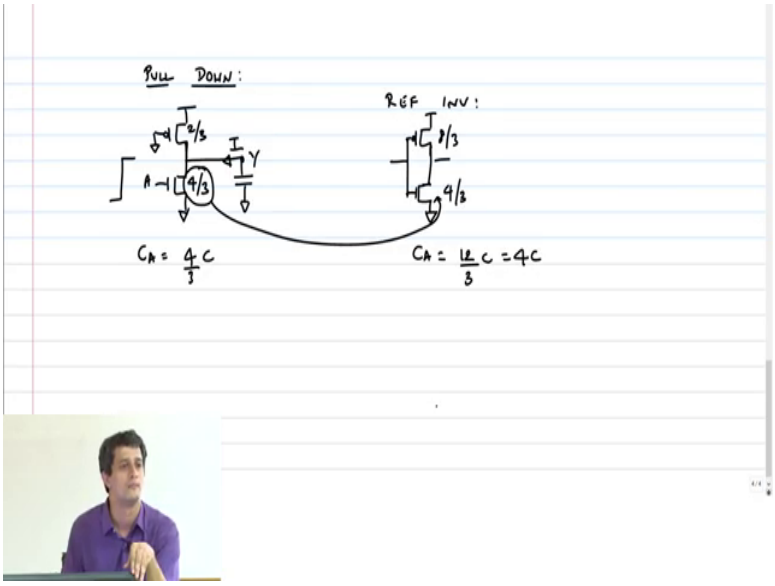

Now, what about the pull down logical effort? This is 4 by 3 2 by 3 output Y. I am going to construct my reference inverter ok. Now, question is this is 4 by 3, Can I put the 4 by 3 here? Can I make this 4 by 3? If this is 4 by 3, what should the PMOS be 8 by 3? What is the logical effort? So, C A here is 4 by 3 times C. What about C A here? It is 12 by 3 into C that is equal to 4 C.

So, is the logical effort 1 by 3? Again go back to how we constructed the unit inverter. Question is not whether the resistance is equal. How much current is available to the load capacitor for discharge is what matters. So, here in the Pseudo NMOS case what matters is this current. So, input is going instantaneously high. Therefore, we know that the current coming out of this load capacitor should be I.

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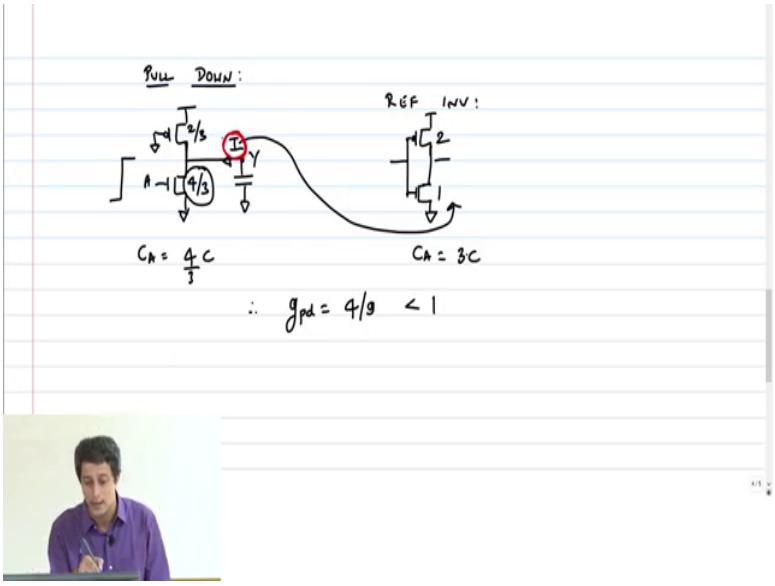

So, what you should do is not this, but instead take this I and put the number here. What is the number I should put if I? 1, if this 1, what is PMOS? 2, therefore, this will be how much C A will be 3 C which implies logical effort of pull down equal to 4 by 9 which is less than 1 much less than 1 is close to half.

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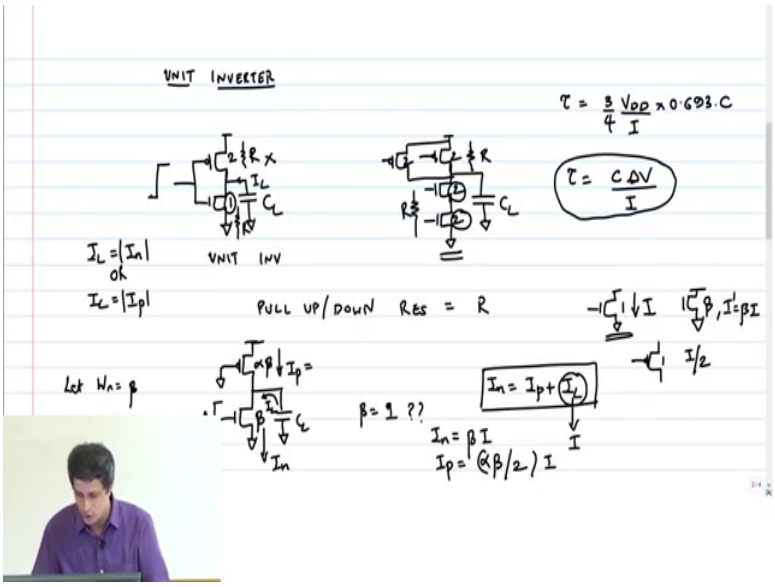

So, just to make sure that we have been consistently doing all our things correctly you go back here right.

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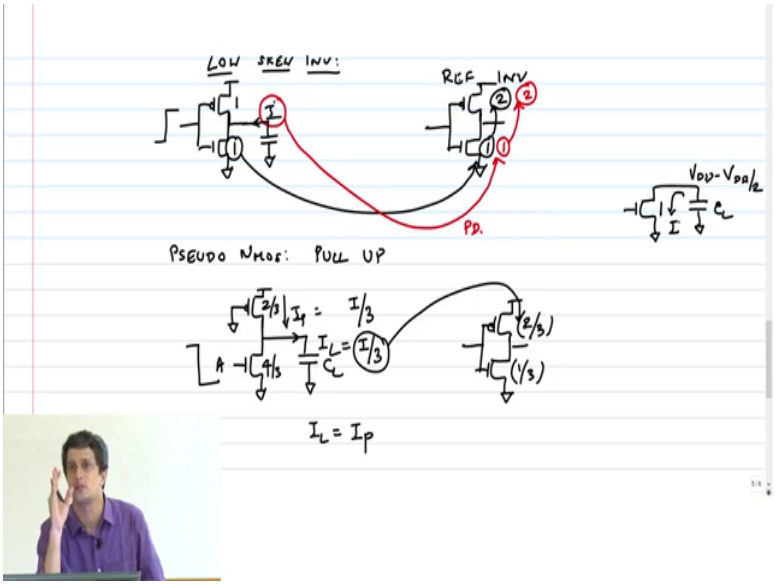

For example, let me go back and let me take the high skew inverter for example, or let me take no skew inverter. This is 1 and this is 1. This is the low skew inverter. So, in order to find the logical effort what did we do we first constructed the reference sorry reference inverter and how did we construct that. This is for let us say I wanted to do it for pull down. I needed to construct be reference inverter such that the NMOS transistor had the same drive strength. So, I said this you can put here right and therefore, this is will give you 2.

And, then we calculated the logical effort right, but this is equivalent to saying that the current to this guy is actually I because when my input goes high instantaneously the NMOS turns on and the PMOS cuts off, so, all the current coming out of the load capacitance flowing through the NMOS. Implicitly what we were doing is actually saying that if this is I then this is what I am going to put here as the size.

So, that the current through that NMOS transistor is still I and therefore, that is also 1 and then you say that this is 2. Then the logical effort is basically you know this 2 by 3 or something like that. So, what we are being doing till now is perfectly consistent with what I am telling you now for the pseudo inverse case. Because all the current from the load went through the NMOS or all the currents on the PMOS went into the load there was no current splitting there.

So, in the pseudo inverse case you only have to make sure that this current is what I have to find. I have to construct my static CMOS reference inverter to have the same drive current I as my reference as the pseudo NMOS inverter here. And therefore, the reference inverter size is going to be 1 and 2 clear.

Student: (Refer time: 09:00).

Yeah.

Student: (Refer time: 09:01).

Yes, that is exactly what it was, but if you take the no you should be careful. When I take the pseudo let me take the high skew inverter or low skew inverter, but I wanted to this was basically for pull down. When I wanted pull up what do I do then I have to take the PMOS 1 then become 1 and half. So, that will change.

Student: (Refer time: 09:30).

Yeah.

Student: (Refer time: 09:32).

Yeah.

Student: (Refer time: 09:40).

Yeah.

Student: (Refer time: 09:41).

No, I did not understand.

Student: (Refer time: 09:48).

Ah.

Student: (Refer time: 09:50).

Yeah.

Student: (Refer time: 09:52).

Yeah.

Student: (Refer time: 09:53).

No, that is what I said. So, let us, ok good question. Let us rework out this pull up case right for my pseudo NMOS pull up. A – this is my load capacitor C L. What is the definition of pull up ideally my input falls and turns off my NMOS transistor instantaneously correct. So, therefore so, if this is 4 by 3 and this is 2 by 3 I have a current I P which is equal to I by 3 correct. Now I P and then there is a load current I L.

Now, because the NMOS is cut off completely I L equal to I P. Therefore, when I now constructed my reference inverter, what do I say this is equal to I by 3. I am saying this value

has to appear here it must be compared to it reference static CMOS inverter such that the PMOS transistor provide the current of I by 3. How will you get I by 3 if the size is 2 by 3 and therefore, if that is 2 by 3 this has to be 1 by 3.

Student: (Refer time: 11:50).

Yeah.

Student: (Refer time: 11:51).

No for a PMOS the current is if my PMOS transistor as a size alpha W is alpha then the current to that is alpha I by 2 where I is basically with the current of a NMOS transistor you are right.

Student: (Refer time: 12:19).

I is always this remember do not do not forget that. It is basically a unit NMOS transistor discharging a capacitor C L from V DD to V DD by 2 that current is I. So, for that if I want the same current I in the PMOS I have to make it twice the way clear. So, it is very important to recognize that we have not been doing anything wrong or inconsistently.

It is just that I could interchangeably talk about resistance in current because there was no you know other current there. In pseudo NMOS I cannot do that absolute very carefully clear. Any other questions?.

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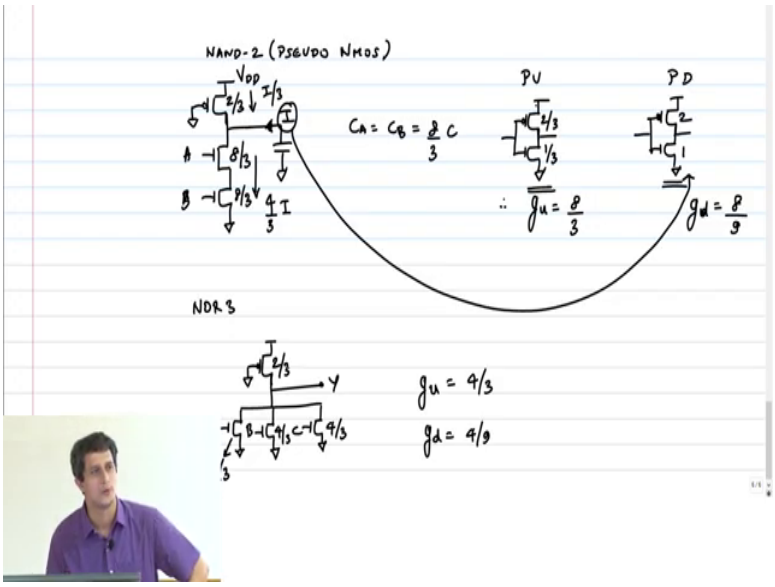

So, now I can you know take this logic further and say if I want a let us say I want a NAND2 gate in pseudo NMOS. So, what do I do? I guess we need to add another transistor that is B. This is 2 by 3. What should the size of NMOS transistors B? Inverter was 4 by 3. This would be?

Student: (Refer time: 14:11).

Sorry.

Student: (Refer time: 14:13).

8 by 3. See now I can combine resistances because two transistors are in series right the same current is going to both of them. So, this has to be simply 8 by 3 and 8 by 3 ok. Now what is the pull up logical effort of this?

Student: (Refer time: 14:38).

Right.

Student: (Refer time: 14:41).

What is pull up logical effort? C A equal to C B capacitance on the inputs what are they? What is the capacitance first? 8 by 3 times C, correct. So, what is the pull up logical effort?

Student: (Refer time: 15:06).

So, how do you do that? So, again you have to construct the reference inverter right for pull up pull down. So, pull up static CMOS inverter is like this. What should the PMOS size be? 2 by 3. NMOS therefore, is 1 by 3. Therefore, the pull up logical effort is how much? 8 by 3 clear. What about pull down? I want to construct my reference inverter again. What should be PMOS I mean NMOS size be 1. Because even here the effective current that is going to come out of my load is going to be I.

This current to the NMOS will be 4 by 3 times I. And, this is going to be I by 3. Therefore, I am going to take this current and put it at my NMOS transistors with 1 and 2. Therefore, pull up the pull down logical effort is how much 8 by 9 clear. So, you have to you know the it will turn out that these reference inverters do not change because from now I am going to size my transistor so that the effective drive strength is the same with respect to the unit gate.

So, these reference inverters will remain the same whether you do NAND, NOR whatever stack, ok. So, now, try this NOR 3 NOR 3 gate. Can you first draw a pseudo NMOS all three gate A, B, C, output Y? What should the PMOS size be? 2 by 2 by 3 NMOS.

Student: (Refer time: 18:45).

4 by 3 4 by 3. This also will be 4 by 3. What is the pull up logical effort?

Student: (Refer time: 19:03).

4 by pull down logical effort. 4 by 3. What if I made this and n input NOR gate. It is the same thing that is the key advantage of getting rid of the PMOS stack for the NOR gates where the logical effort grows because my PMOS stack size is growing I am able to make sure that the logical effort is 4 by 9 irrespective how many ever input NOR gate I have clear.

Student: (Refer time: 19:46).

Doubt.

Student: (Refer time: 14:48).

Ah?

Student: (Refer time: 14:50).

Why is?

Student: (Refer time: 14:53).

Why is the PMOS 2 by 3? Because we just calculated based on the noise margin right VOL has to be something and I said let us assume that W P by W has to be half. It gave us a good noise margin. So, I said that is 2 by 3. So, this PMOS because it is just one PMOS pulling up that is 2 by 3 always. See the worst case is 2 by 3 pull up and one of the 4 by 3 is pulling down.

So, therefore, it has to be 2 by 3 and 4 by 3 as you say clear. I know this is like it take some time to sink in settling. So, please think about it go back work out this example. So, in fact, I would suggest that you should necessarily go back and work out this whole table here ok.

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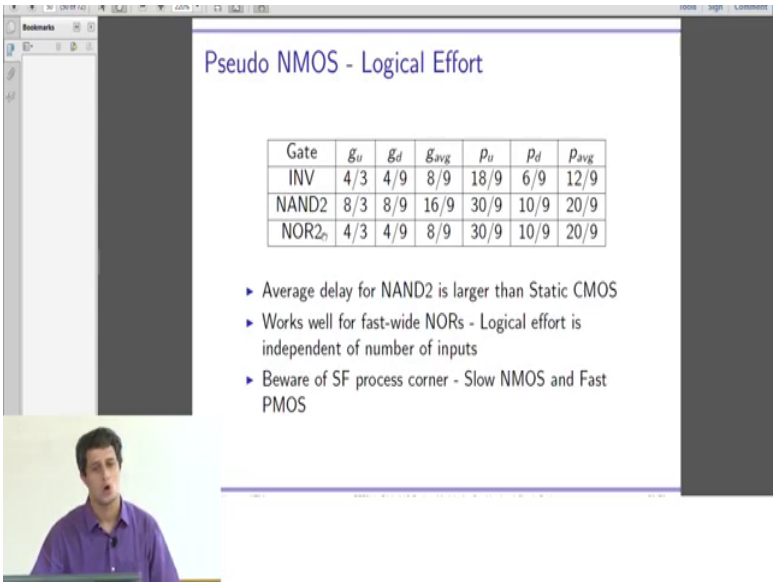

I will put this in the tutorial as well. This here right for a NAND 2 for a NOR 2 work out these thing you should get these numbers correctly clear. Now parasitic delay is what. You

just again you are going to count diffusion capacitance divided by the diffusion of that reference static CMOS inverter that we constructed.

So, work this out as well we can discuss it in a tutorial second later clear I have 10 minutes to go. So, now, clearly this is not a gate that can be used because I have a static current then the output input is high and the output is low right. I have a standard I mean a DC current right and that is going to kill your power. So, it cannot be used in reality right. So, therefore, something has to be done to exploit this fact that we are getting rid of the PMOS stack, but at the same time we are able to you know get this benefit of lower logical effort.

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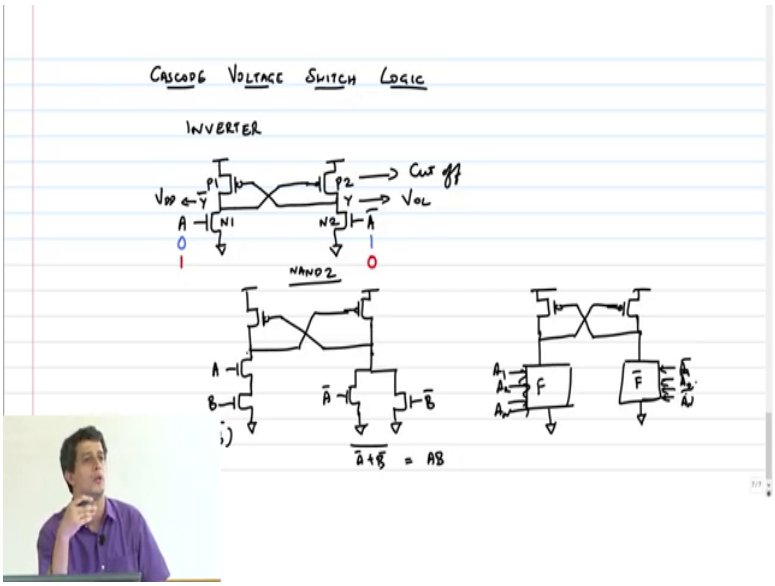

So, how do you do that? It turns out it can be done with cascode voltage switch logic. So, let us look at a simple inverter. A right normally I would have connected this with ground if I wanted a pseudo NMOS inverter. Now I am going to coming slightly different to overcome

that static current problem. A bar and I am going to cross couple it like this ok. So, let us first analyze the static cases a equal to 0 right. Let me use blue for that.

This is 0 and this is 1 V DD correct. Now if input A is 0 let me also label the transistor. So, that it is N1 P1 into P2. If A is 0 input N1 I mean transistor N1 is turned off right. Now on the other hand right. So, I assume that the sizing is very similar right. You have 4 by 3 2 by 3 4 by 3 2 by 3 ok.

On the other hand, if A bar is 1, I am assuming now that the input and its complement is available A and A bar are available together which is true in some cases and therefore, you can use it in those special cases ok. So, if A bar is 1 then what happens the N2 P2 will now start fighting right and the output let me call this Y bar and Y. The output Y is going to come somewhere near VOL right. Somewhere it is a very low value. Now, if output goes to VOL then the VGS of P1 will now become how much. What?

Student: (Refer time: 24:56).

VOL minus V DD. Again it will be approximately minus V DD it will turn on P1 very strongly and therefore, Y bar will get pulled to V DD. Now if Y bar goes to V DD and the gate of P2 is connected to Y bar then P2 will now turn off. Therefore, P 2 will cut off. So, we are using this cross coupling to turn off the other transistor.

So, this is clearly a case where it is like a pseudo NMOS transistor logical effort is low. Note very importantly my input A or A bar is still connected only to the NMOS transistor they are not connected to that cross coupled stack anywhere. If it is connected then the logical effort you go up that is a problem right. So, this cross coupling is happening only between output and this.

Of course, the logical the delay might be slightly different because of this cross coupling, but to a first order I still maintain the same logical effort, but anyway this problem of static

current flow. Similarly, if I now do the case where A equal to 1 and this is equal to 0 exactly the opposite arguments will come in and the P1 will get cut off by Y correct.

So, how do I take this logic and generalize it to any implementation right. Suppose I want to do a NOR or a NAND right. So, it is very simple all you have to do is I am going to look at a NAND 2 gate. So, normally my pseudo NMOS implementation would be like this. This is the NAND 2 AB. What should I implement on the other side?

Student: (Refer time: 27:14).

Yeah.

Student: (Refer time: 27:19).

B.

Student: (Refer time: 27:20).

No, I cannot hear you.

Student: (Refer time: 27:23).

A B.

Student: (Refer time: 27:24).

Exactly right. It is not just A B in parallel it is actually the A bar B bar. What is this logic here? This is A into B right whole bar because it connected to ground. What is this logic? It is A bar plus B bar whole bar. This is equal to A B. So, you implement true logic on one side and the complement logic on the other side then you be guaranteed that one of these stacks

will be turned off always right and this cross coupling will take effect and it will cut off the other way very easily ok.

So, in general you got to implement this. You just put implement the function f here. Then you implement the function F bar here and the inputs are connected to these sides A1, A2, An, A1 bar, A2 bar An bar. So, you can implement any arbitrary logic illness similar to pseudo NMOS style, but avoid all this static current.

Of course, the key assumption we are making is both input and its complements are available out here. I am not generating for example, if I have to generate A bar internally then this is not useful because then the logical effort will change you have to calculate what that capacitances right there is now a fan out a is driving this gate plus the inverter.

So, that is not useful A and A bar should be available from outside simultaneous ok. Then for example, if you are trying to implement a decoder typically you will find that you have A and A bar easily available ok. Now so when the decoder output is being used somewhere since both the output and complement are available you can just feed it to a CVS a logic example.