Digital IC Design
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Lecture – 48
Pseudo NMOS Inverter

Last class we were discussing about the idea of doing away with the PMOS stacks entirely right.

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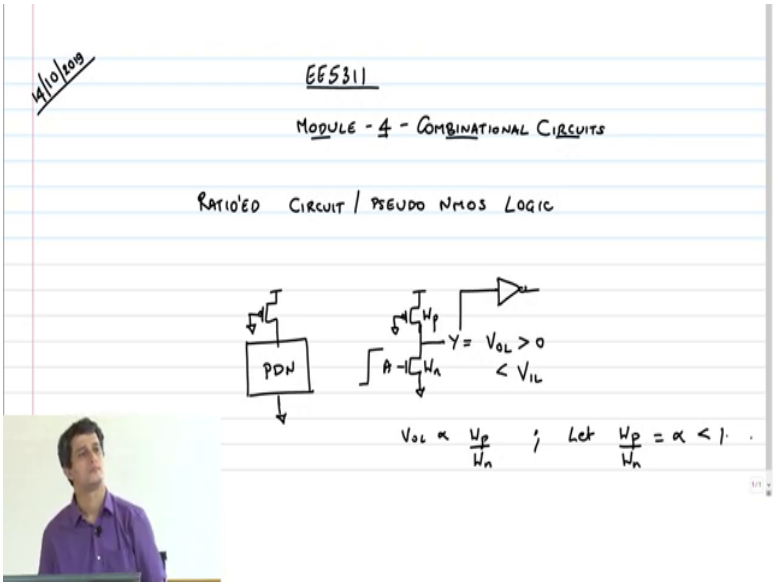

And therefore, we came up with its idea of Ratioed circuit or pseudo NMOS logic right. And the basic idea was very simple, you have a pull down network which is only NMOS transistors to ground, the PMOS transistors you replace by a permanently on PMOS transistor. Going to be connected to ground which means that this PMOS transistor is always on and the idea behind this doing this is the input is not driving my PMOS transistor.

Because the PMOS transistor by nature has to be double the size of the NMOS to get the same current; the PMOS transistor was a guide who was giving the logical effort, who was making the logical effort very high especially for nor kind of gates where the stack is now going to grow on the PMOS side rather than the NMOS. So, the point is, we had to do something in order to reduce that logical effort.

So, we said remove that PMOS do not allow the input to drive that PMOS transistor. So, the capacitance that the input sees is only because of the NMOS transistors on the pull down network right. And off course if you take now pseudo NMOS inverter which is like this, it is my output Y then the issue is, if you take the case when A is 1 or A is 0 then there is no problem.

Because the output will be VDD the NMOS transistor is going to be off; only the PMOS will be on there is no current from VDD to ground right other than we gets current and hence there is no issue when we are talking about the output going to logic high. However, if you now try to turn this input on by instantaneously taking my input from 0 to 1; then what happen is you are now going to have the fight between the PMOS transistor which is trying to pull the output to VDD and the NMOS transistor which is trying to pull the output to ground right.

And therefore, be output now will go and land up at a logic V OL Output Logic Low which is greater than 0; right and we did some calculations and we figure that V OL is simply propositional to W p by W n well W n and W p are the widths of the NMOS and PMOS transistor respectively. If you make the PMOS transistors stronger; that means, it will going to pull the output high with more current and therefore, it is going to take the output closure to VDD.

So, you have to keep this ratio appropriate so that the output logic V OL is low enough; remember that even a cascade is gate to an other inverter. Let us say right if I want to cascade this to another inverter like this in order for this circuit to work correctly V OL should be less than V IL of the next inverter; only that you did get recognize logic low. So, there is a constrain that you have to keep it low and you have to keep at as low as possible.

So, the way we do it is I will give you a specification, saying the V OL has to be lesser than this value like pay 0.1 or something like that and then you find out what my W p by W n should be ok. There I will say that depending on the spec let W p by W n equal to alpha is W p by W n that is alpha is greater than 1 or lesser than 1? I will ask you again what should V OL be? Very close to ground may be 0.1 word. So, W p by W n has to be has to be less than 1; now that is the difference between the static CMOS logic and the pseudo NMOS logic.

There is PMOS is now we are sacrificing the pull up strength of course, in the process but for the logic to work properly which is of primary importance you can do timing and other thing later. First the logic has to work correctly, the PMOS has to be weak which means the W p by W n will be a number which is less than 1, alpha is less than 1 right it can be may be slightly greater than 1, but most of the time it be less than 1 ok.

So, now with this let us first thing we will do is, to construct our unit inverter ok. We did this in all the cases, you know even in the high speed logic and low speed logic we said we will construct our unit inverter ok.

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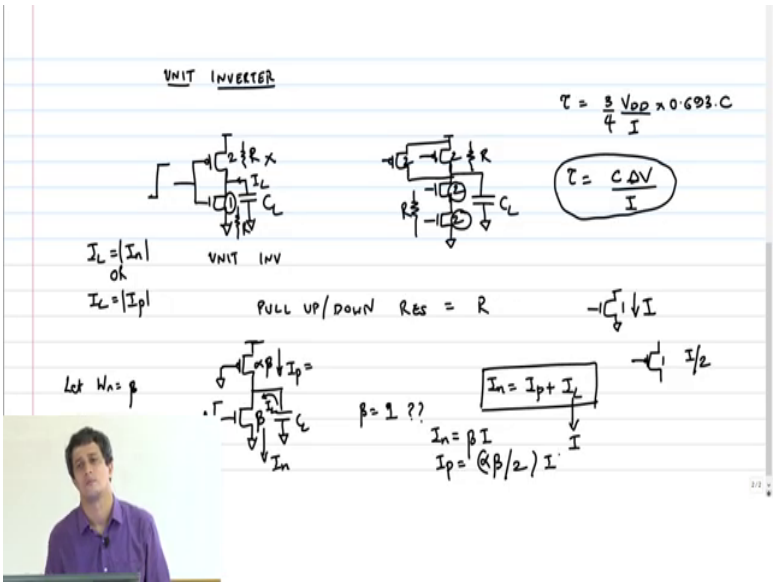

So, let us look at the construction of a unit inverter first; because if you understand this then the logical effort calculation become very simple. So, let me take a static CMOS ok, let us go back to you know how we constructed our unit gates. I had a capacitance load capacitance and I said this has to be 1 and 2 right. Now when I constructed my this is my unit inverter, when I constructed my band, it was like this right we said this has to be 2, 2, 2 and 2.

So, why did we said 2 2? So, that the effective resistance is still R right; we said this also will be here itself of R both ways right even this will be R ok. So, we were able to combine series transistors in order to find without (Refer Time: 07:17) resistance and we match the resistance in order to construct our unit gate. This gate can be size up you will get more (Refer Time: 07:27) strength.

Similarly the inverter can be sized up you will get more (Refer Time: 07:29) strength there as well right. But the unit inverter is that pull up and pull down right pull down slash down resistance equal to R and what is R is basically the resistance offered by a unit NMOS transistor right; that 3 VDD by 4 id. Now the problem is can I apply the same logic to my pseudo NMOS logic? Let us look at it, I want to ground this guy which is VDD a and b plus my output that driving a load capacitance.

We only know one thing that W p by W n should be alpha right but W n can be anything and W p will scale accordingly. So therefore, I am going to say let W n equal to beta which implies W p should be how much? Alpha times which is beta and therefore it is alpha beta. So, now, my question is the following should the unit pseudo NMOS inverter have beta equal to 1? What happens if my beta equal to 1?.

The NMOS transistor is same right that is what we have been doing; if you look at all the cases this one has been basically you have scaled; however, you get equivalent resistance there. Can I do the same here? Beta equal to 1, is it possible? The catch here is, unfortunately my PMOS transistor is also conducting when the output has been pulled low ok.

Here by the way inherently we are sort of saying I am going to pull down the logic very quickly. So, we are sacrificing pull up speed, because we are we have to lower the PMOS size we have no other low. So, that we no logic works correctly. So, in sometimes I have already compromise the pull up speed that is already been done.

So, I am not going to worry about what the pull up speed is what about the pull down speed is? That is what I want to worry about. So, in the pull down case, I have some current which is coming from my PMOS transistors always right. So, is my input instantaneously went from 0 to 1; then there is a current I p coming from the PMOS transistor. There is a current which is going to flow to the NMOS transistor I n what is going to be available to discharge the load capacitor? I n minus I p. So, I have to look at what this current feels.

Clearly, I n equal to I p plus I L. So, there is fake current which is coming from the PMOS transistors which is going to the NMOS as well; but that is not serving the probable discharging my load capacitor why was it earlier, why were we able to talk about resistances and get a way? Because is my input went uncertainly from 0 to 1, it turned out that the PMOS was cutoff immediately; assuming incontinences is rise its only the NMOS that was on and whatever current went through the load or came from the load went into NMOS transistor.

So, we had the condition that I L was equal to I n or I L equal to I p is mod let me not worry about it sign. All the current that was available from the transistor was used to discharge the load and ultimately that is what dominate is delay not dominate determines delay right. You remember we derived the expiration for the delayed as basically you have 3 by 4 VDD by I ok, I naught by I into what 0.693 which was R into C right; we got some number then we said that we could also able to C delta V by I.

Now you have to look at this definition more carefully because the current that is available to discharge the load capacitor is of key consult was not the resistant of the transistor ok. So, what is it that should be equal to I in this equation here? For my unit gate, we always said that I n or I p should be equal to I and that is how we calculated even now its a load current that we are going to face should be equal to I. This has to be I and of course, I is basically the current use the transaction the unit NMOS transistor.

So, can you now tell me what is I n in terms of beta and I? Thus width is beta if we unit transistor has a current I what is the current would be scale transistor? Beta times I. What about I p? Alpha beta I by PMOS current get scaled by mobility always cannot forget this; see if I have this gives me I, then PMOS transistor with the same width will be I by 2 because mobility is half ok. So, I p is alpha beta by 2 into I ok.

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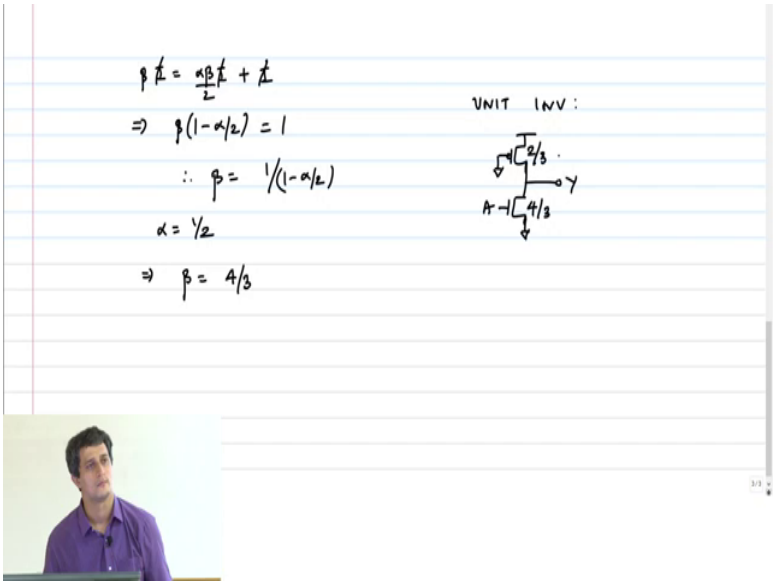

Now, I want to substitute this in my equation, I will say alpha I equals alpha beta I by 2 plus I L has to be equal to I because that is my (Refer Time: 15:07) inverter pseudo NMOS inverter. So, what is beta equal to can you calculate? I will; obviously, know and therefore, I get sorry, 2 alpha by 2 alpha minus wait let this I working out right. I want to find out beta right sorry, this would be beta time phi now makes sense right thank you beta into 1 minus alpha by 2 is equal to 1 therefore, beta equals 1 by 1 minus alpha by 2 right.

Now let us take a concrete examples, let us say I want to be alpha to be half; it turns out that the noise you know V OL is low enough if W p by W n is half is just one example ok. Implies what should beta be? Exactly so, this will be 4 by 3. So, what is mine unit inverter? This is 4 by 3; PMOS should be 2 by 3 because alpha is half, 2 by 3 ok.