Digital IC Design
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Lecture – 47
Pseudo NMOS Logic

Carrying this logic further, we can ask a more interesting question, what if I removed the entire PMOS stack, what if I just remove that entire PMOS stack, what will happen? Clearly, now no input is going to be connected to my PMOS transistor, and therefore, the capacitance is dropped not by half, but more than half. So, this brings us to the idea of ratio circuits.

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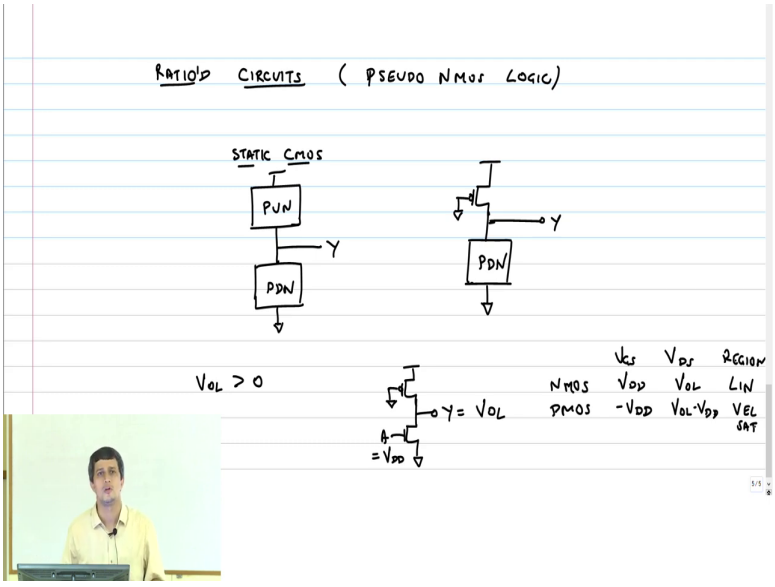

So, as this as static CMOS implementation is like this pull up network pull down network . The idea in a ratio'd circuit or it is also called an pseudo NMOS Logic is like this, pull down network. The advantage in a static CMOS logic was that there was no path for current to flow

from supply to ground means in the steady state. Of course, what we are doing here now is we are connecting that a PMOS transistor to ground with a gate connected to ground always.

So, when the pull down network is active, obviously, there is going to be current that will flow from supply to ground in steady state. So, this is not a good thing. We will see how to avoid this problem, but first let us see what advantage we get in terms of the logical effort ok. What we have been able to do is completely eliminate that PMOS pull up network right, and that is what is your killer for the logical effort always ok.

So, the other obvious problem in this is that when my pull down network is conducting and my output is low, will the output go all the way to 0? No, it cannot go all the way to 0 right, because I have a fighting between the PMOS transistor and the NMOS stack. So, therefore, the output Y VOL is going to be greater than 0 in this pseudo NMOS logic. We will first calculate what that is ok. So, let us consider a pseudo NMOS inverter, this is a pseudo NMOS inverter, only one NMOS transistor it connected to the input A, A is not connected to the PMOS transistor ok.

So, I now want to calculate what happens when a equal to V DD, Y will be VOL. Of course, VOL now has to be close to ground right; other is this that is a gate is going to be useless. So, in what region of operation with my NMOS transistor be, in what region of operation will be the PMOS transistor be? Let us not jump here, let us write it down, NMOS PMOS right V GS, V DS. What is V GS for the NMOS transistor? V DD, V DS, yeah, VOL.

Now, V DS compared to V GS minus V T, where is it? Therefore, region is linear, because VOL is much smaller than V DD minus V T. What about the PMOS transistor, what is V GS?

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Minus V DD V DS, VOL minus. Now, which region is the PMOS transistor? You have to do V GS minus V T right that is a reasonably large number about point three voltage V DD is 1 volt is about 0.3 volts, so that will be about 0.7 volt, VOL minus V DD, where will it be very

close to V DD. Therefore, this has to be saturation or velocity saturates depending on the whether it is short term or long term device right. So, let us say it is in the velocity saturation ok. So, now, we go to the same drill, equate the current in both of them and then we can find out what VOL will be ok.

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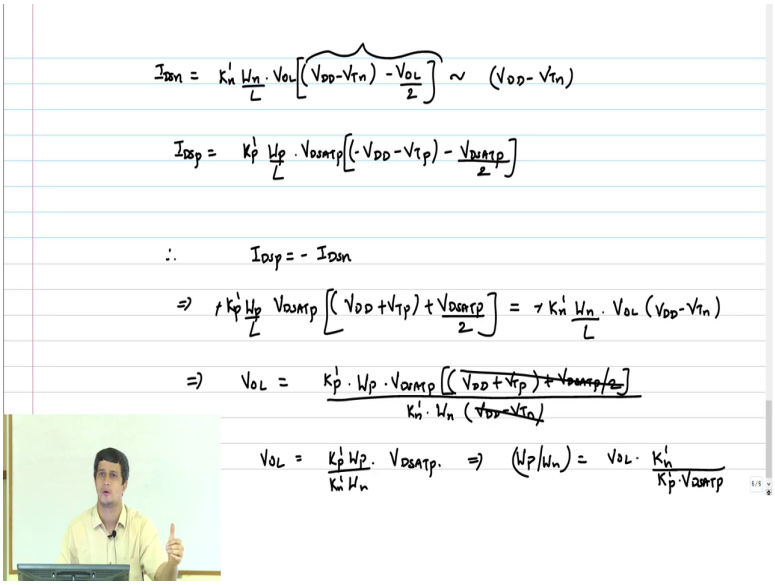

So, what is VOL? I Dsn is in linear region therefore, this is I can say K m prime W n by L into V DS that is VOL into V DD minus V Tn minus VOL by 2 right. Now, what is I DSP? K p prime W p by L into V D sat P into what is this minus V DD right; minus V T P minus V D sat P by 2 clear. Now, VOL is a very small number. So, therefore, this V DD minus V Tn minus V OL by 2, I can approximate right as V DD minus V Tn.

So, therefore, I will now say I DSP equals minus I DSM implies K p prime W p by L into V D sat P into V DD plus V T p plus V D sat p by 2 right, I am going to bring the minus sign

out equals minus K n prime W n by L into V OL into V DD minus V Tn clear. Therefore, I can now cancel out these two things, and I will get VOL as K t prime into W p into V D sat p V DD plus V T p plus V D sat p by 2 by K n prime into W n into V DD minus V Tn ok.

So, what is this tell you first of all? In order to achieve a certain V OL, so that the circuit can even function logically correctly, I need to have a certain W p by W n ratio. If the PMOS transistor is extremely strong, then when the pull down network is active, the PMOS transistor will try to pull the output closer to V DD and will not allow the pull down network to go to 0.

And therefore, in that fight output will go and land in between 0 and V DD, and that is completely determined by what your W p by W n ratio is, that is why this is called a ratio'd circuit, because it does not even function if the ratio of these PMOS and NMOS transistor is not correct.

Earlier I had mentioned that static CMOS is independent of gate size as far as logical functionality is concerned, it will work whatever size you put, whether you put one-half, one, 1 by 4 or ten 1, it does not matter, it will function correctly NMOS and PMOS. It is only for delay purposes that we had to be made it one nine two and all that stuff, logically it would still function, but this circuit will not function unless you size it appropriately, so that your VOL is meant. So, the way you do it is, you want a VOL, I will give you a VOL, and say size the inverter, so that it meets this VOL first, then you use this equation calculate what might W p by W n should be, clear.

So, which it implies now lets you know make some simplifications. Suppose those V DD plus V T p plus V D sat by 2 right, suppose the V T and V D SATs, where such that these two terms cancel out suppose right. I am not saying that V T p equal to minus V Tn, I am saying the V Tns and V D sat p together cancel out this term right, then it implies VOL is simply K p prime W p by K n prime W m into V D SATp.

This is the first order thing. But of course, you do not have to make this approximate plan just trying to bring out this (Refer Time: 13:06) ok. So, what does this say? It says that W p by W

n equals VOL into K n prime by K p prime into V D SATp. So, if your VOL goes up, then W p has to go up correct that is what is equal to W p by W n is proportional to V OL. So, VOL has to come down, then W p by W n has to come down.