Digital IC Design
Prof. Janakiraman Viraraghavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 45
Skewed Gates

Now, I am going to make one more assumption that we made. We said that the rise and fall delays are equally important. And therefore, both of them had to be equal right, instead both pull up resistance and pull down resistance have to be R. This is not always true for example, when I am dealing with a memory I might want to turn on the word line of the SRAM cell very quickly, but its to turn it off slightly close right.

Therefore, the rising edge is more critical than the falling edge ok which means, now there is an opportunity for me to reduce the logical effort on that particular edge. Till now we have said the logical effort of an input, A B C we have found out logical approach is very clear that the logical effort depends on the input. Now its not only dependent on the input, its also going to depend on the rise or fall ok. And, this leads us to the concept of a Skewed Gate ok.

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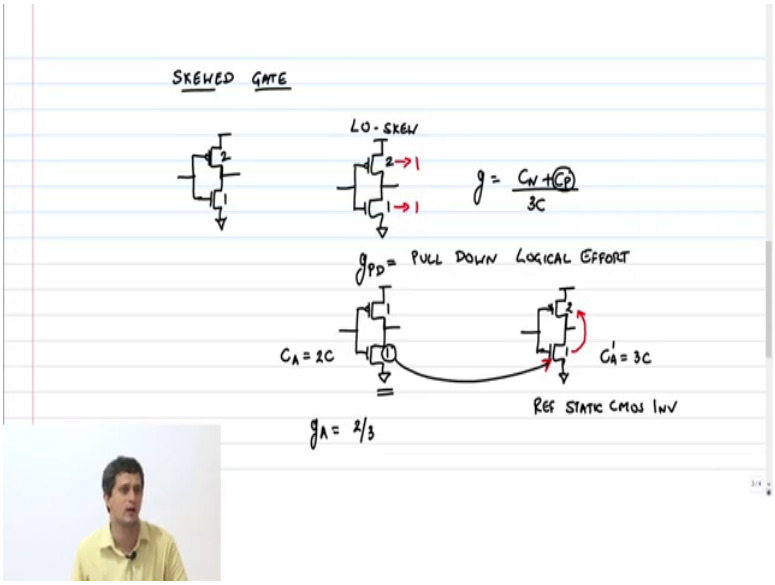

So, let me now draw the symmetric static PMOS k 1 2. Now let us say I want to favor the rising edge or no, let me take the other case first. Let us say I want to favor the falling edge; I want a favor the falling edge and therefore I am going to call that a low skew inverter, right. So, what I am going to do is, I am going to follow. I now need to size this accordingly ok, so I will not put the size down right now.

So, what I want to ask you is; if I want to favor the falling edge right and I want to reduce the logical effort what should I do? Increase the size ok. So, you are saying instead of 1 and 2 you want me to make this let us say 2, but if I make it 2 what will happen to the logical effort. It will increase, because remember logical effort is it does not depend on whether its 1 or 2 because I am going to compare it now to a reference static PMOS inverter with the same

drive strength. So, if you view here NMOS with size 2, I will construct my reference inverters it also has an NMOS of size 2, alright.

So, the key point here and I that is what even I pointed out the asymmetric gate says it may be counterintuitive that I am increasing the resistance of that transistor, but my main aim is to reduce the capacitance ok. So therefore, this is really not possible. Now again, what is the logical effort? It is basically C NMOS plus C PMOS by 3 C. Of course, if it is the symmetric inverter then is going to be the same, its going to be 1. Now, I want to improve the logical effort on the falling edge. The falling edge right is determined by the pull down stack. And therefore, it is determined by the NMOS transistors, capacitance, resistance are all that.

This guy is just a deadweight that is adding to the capacitance, if I consider only the falling edge. When I am falling, when the output is falling there is a capacitance coming from the PMOS transistors, but the PMOS transistor is not adding anything or not reducing the delay of my poly transition at all. Therefore, should I increase the capacitance of the PMOS transistor or should I decrease the capacitance of a PMOS transistor? I have to decrease the capacitance. And therefore, this 2 I will make 1 and I will keep this as 2.

Here what I have done is, since the falling edge is important I am not changing that resistance that is already R; I cannot reduce, I cannot increase that resistance now right by making that smaller. So, the other option is of course if I make this as let us say half you might think that the capacitance will drop, but then my resistance is increasing. You can only do this resistance increasing if another transistor on the stack will be able to compensate for that, clear. Therefore, I cannot make this half, I need to keep it as 1. But the top guy PMOS I can make it as 1 ok.

Now, with this kind of a sizing I am now going to go ahead and find out the logical effort for each of the edges: rising edges and falling edges ok. So, let me take this guy 1 1. And I am going to look at logical effort of pull down. This is equal to pull down logical effort. I now need to compare the capacitance offered by this gate to the capacitance of a symmetric static PMOS inverter with the same pull down strength.

Because, now I am talking of the pull down case I am talking about the falling edge. Therefore, I am now going to construct my reference PMOS inverter ok. This is my low skew inverter, this is my reference static PMOS inverter ok. You have to tell me what these sizes should be of the NMOS and PMOS transistor. I have to compare the capacitance of this low skew inverter ok. What is the capacitance by the way?

C A is 2 C to the capacitance of a symmetric static PMOS inverter with the same pull down strength. Earlier I just said same drive strength, because pull up and pull down were the same. Now I am going to add an extra rider and say with the same pull down strength. Therefore, this transistor size should be maintained the same: 1 right, clear. Now, if this is 1 and I want this reference inverter to be symmetric static PMOS inverter what is the PMOS be? Exactly. Therefore, the capacitance here C A I call it a prime is 3 C.

Therefore the logical effort g A is going to be what 2 by 3. What was the logical effort of a reference static PMOS inverter? 1, I have brought that down to less than 1. What is your intuition about what will happen to the logical effort on the rising edge? Yeah, it has to increase because that is how I have brought this guy down by sacrificing that edge. I have you know, I have been mucking around with the PMOS transistor and therefore I am I have to pay a penalty there.

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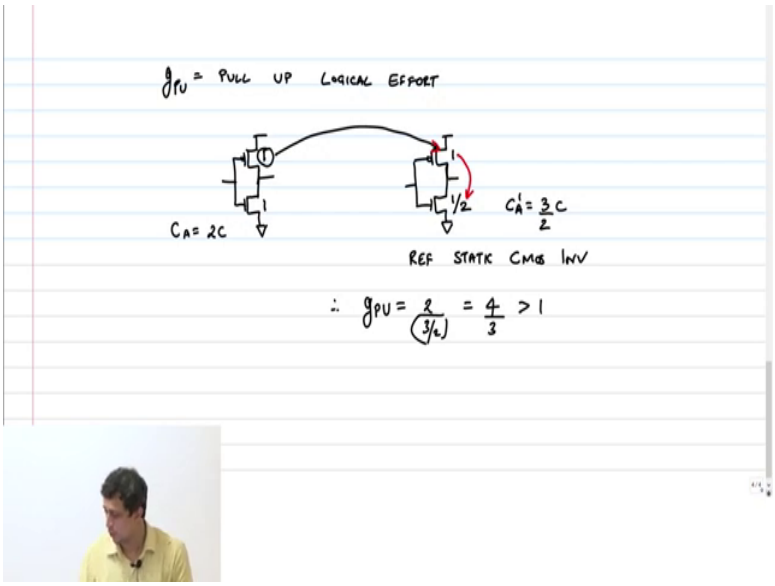

Therefore, we will now go ahead and calculate the logical effort of the pull up ok. So, here is my low skew inverter, this is 1 and I said this also is 1 ok. I am now going to compare this with a symmetric static PMOS inverter with the same pull up drive strength, because I am now looking at the pull up logical effort which implies that this 1 should be the same here ok. This is my reference static CMOS inverter that I am going to compare against, right; reference symmetric static CMOS inverter.

If that if the PMOS is 1 and I want this to be a reference symmetric static PMOS inverter what should be NMOS; half, only then that pull up pull down strength will be the same. And therefore, this will half. So, the way is this gives rise to this 1 here then this will tell me how much this should be, right. In the previous case because I am looking at pull down I first calculated this then this told me that PMOS should be 2. So, get that direction right, you have

to fix one transistor and then get the other one according to the symmetric constraint that we have ok.

Now if this is 1, so what is the capacitance, C A is how much; is still 2 C. What is the capacitance here? C A prime; 3 by 2 C. Therefore, g pull down is how much? 2 yeah it basically 2 by 3 by 2 4 by 3; oh sorry, sorry, sorry, clear. So, what did we do? This clearly is greater than 1. For a low skew inverter where I am favoring the falling edge I brought the logical effort to 2 by 3, but I had to increase the logical effort on the for this pull up to 4 by 3 in the process, clear. So, similarly you can construct what is known as a high skew inverter; high inverter.

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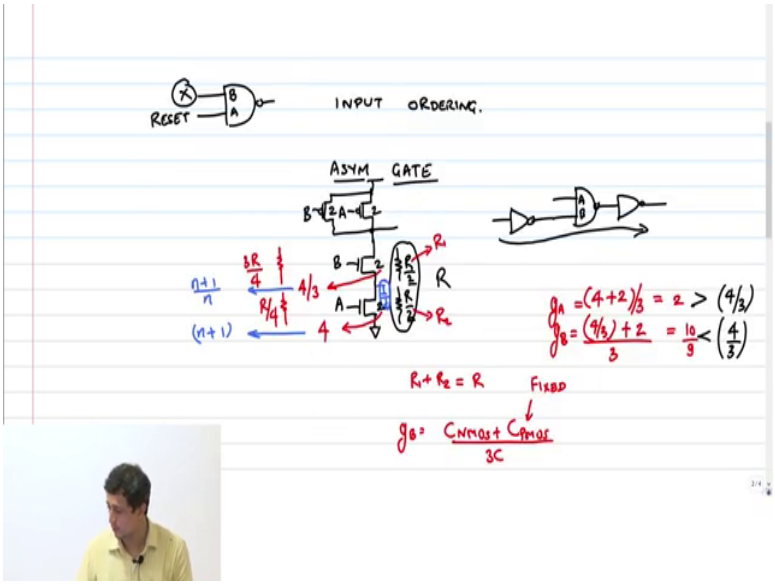

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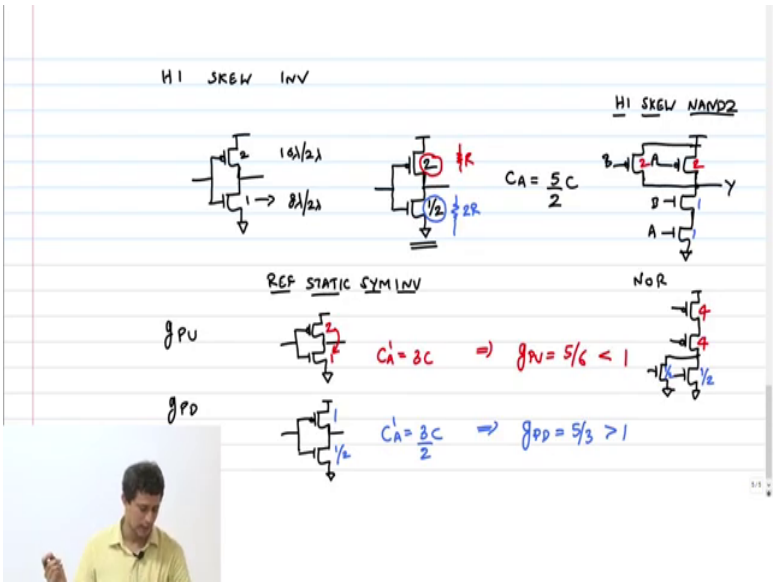

So, this is my reference static PMOS inverter. I want to construct a high skew inverter, which means I want to favor the rising edge. Rising edge is determined by the PMOS. Therefore, the PMOS I am going to leave it as it is, because that resistance is already R I cannot reduce that any further. Therefore, my high skew inverter will be like this, this is fixed.

So, when the output is rising to the PMOS transistor the capacitance that is coming from the NMOS is a dead weight. Therefore, I am going to reduce that capacitance. So, I will make this half, assuming that the unit width is larger than the minimum width allowed in the technology ok.

So, what I mean is this 1 is going to correspond to some let us say 8 lambda by 2 lambda, and this is 16 lambda by 2 lambda. And let us say the minimum width allowed in the technology is 4 lambda, then this half is still allowed that is what I meant. Does not mean that half cannot

be used, it just depends on the absolute minimum. Remember these are relative sizing that I have been speaking about. Therefore, this half is allowed, right.

So, now I am going to calculate the; so before we start logical effort of pull up and pull down which one will be greater than 1 which will be less than 1; pull down will be greater than 1, pull up should be less than 1 right; that is the that is the aim. So, what is the capacitance of this (Refer Time: 15:35) what: pi by pi by 2 C ok. Now I am going to calculate logical effort of pull up, logical effort of pull down ok, this is my reference static symmetric inverter. I am going to consider these two things.

So, I am now looking at pull up. I have to compare this high skew inverter that I have to a reference static PMOS symmetric inverter with the same pull up strength. Therefore, this 2 here has to appear on the PMOS. Now if that is 2, what should be my NMOS for this inverter to be a symmetric static PMOS inverter? 1. Therefore, this will give you 1 here. And therefore, the capacitance C A prime will be how much 3 C and implies the g PU is how much? Yeah, 5 5 6 of obviously less than 1.

Now, I want to calculate the logical effort of the pull down. What should I do? I have to compare it with a reference static PMOS inverter with the same pull down strength. Therefore, this half has to appear here, if this is half what should be the PMOS 1. Therefore, C A prime is how much? 3 by 2, which implies GDP is how much 5 by 3 greater than 1, clear. Any questions? Yeah.

So, again that means, like I told you it depends on the minimum width in the technology right, then it also depends on the layout asymmetry and all that. So, the numbers that have been suggested in the textbook are typical numbers that are further usable practical, that is all. But the idea is not do I of course, I do not want it to get stuck with these numbers, even if I make it one by 3 you should be able to calculate between logical effort right. That is its not tied to this there is nothing for; I mean there is no unique solution for these numbers here. Its driven by practical constraint and some usable numbers and sometimes its (Refer Time: 19:04) that is all. Any questions?

So, now you can take this idea of a high skew inverter and take it to a NAND gate take it to a NOR gate and so on right. So for example, if I have 2 and half right, I want to now construct a I 2 NAND. What am I going to do? Right, A B and A and B. So, what would be my sizes of the transistors? I want it to be a high skew NAND. So, the PMOS should be 2 right you do not you do not think that, this will be 2. What should be the NMOS sizes?

The net resistance should be how much? R, no what is this net resistance here the blue, this is how much? 2 R right. Whereas, this top resistant is R, because that is R I said you need you know let me just color code it, so it will be easy to follow. This should be 2 and 2, but bottom the net resistance should be 2 R. Therefore, each transistor to be R and we mean that the size should be 1 1.

What about a high skew NOR? What should be the size of my PMOS? 4 4, because the net resistance could still be R its a high skew NOR and therefore this time will be 4 4. What about the NMOS? Half and half, right. You can now go ahead and calculate logical effort for these gates also to the NORs and NANDs also you can calculate.

I will leave this as an exercise for you; please you can refer my slides here.

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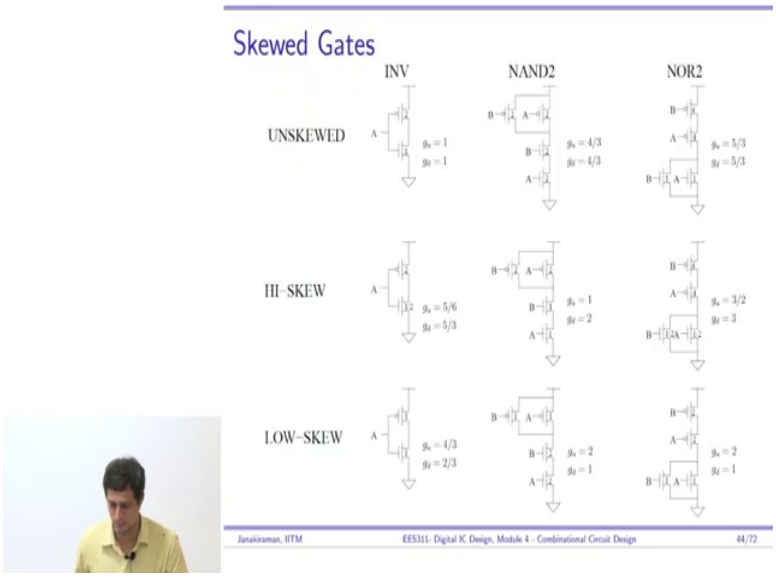

So, what is shown here is basically the unskewed gate: pull up logical effort is 1, pull down logical effort is 1. NAND 2: pull up logical effort is 4 by 3, pull down 4 3 NOR 2 5 by 3 5 by 3 right; the top row is an unskewed gate. High skew inverter we saw the logical effort at 5 by 6 and 5 by 3 right; 5 by 6 for pull up 5 by 3 for pull down. The NAND gate logical effort pull up is 1 and 2.

Now remember, its not that this should be above 1 and below 1, you have to compare this 1 and 2 with respect to 4 by 3. The pull up logical effort has become 1 as opposed to 4 by 3, the pull down logical effort has become 2 as opposed to 4 by 3. So 4 by 3, 1 has become 1 other has become 2. Similarly here with regard to 5 by 3 the pull up logical effort has become 3 by 2 right; 1.67 and 1.5, whereas pull down logical effort has become 3 ok.

So, low skew again the inverter we saw is 4 by 3 2 by 3. The pull up logical effort now has become 2, pull down logical effort has become 1 ok. This is a low skew inverter remember; therefore, the sizes are 2 2 1 1; the PMOS has been compromised, clear. Similarly, for a NOR: the pull up logically point again is 2, pull down logical effort is 1.

So, please go and work these out on your own ok. It is this you do the same thing you have to construct the symmetric static PMOS inverter. That is the only step that you to get correct. Once you do that its just a question of dividing by the capacitance, clear.