Digital IC Design
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Lecture – 40

Logical Effort

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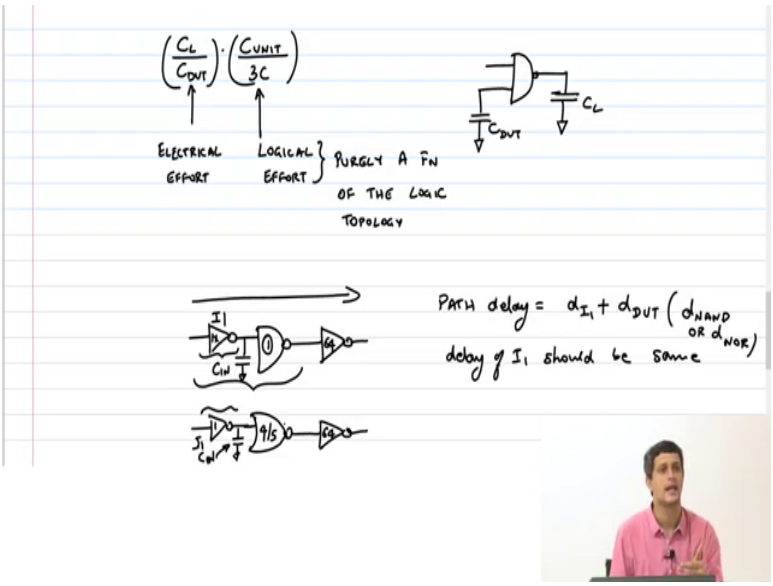

So last class we, so, let us consider this particular example. I have an inverter driving a NAND and driving another inverter. This is let us say 1 x inverter this is let us say 64 x some larger inverter, this has some arbitrary size or let us say it is a unit gate this is a unit gate. Now let me pose this hypothetical question to you, suppose I were allowed to replace this NAND gate by a NOR gate logically without changing anything in the logic, I am just allowed to replace the NAND by NOR hypothetically assume that right then I have the following circuit ok.

This is 1 64, what the size of the NOR is I will not tell you yet ok. Now I want to ask you a question is a NOR gate better or a NAND gate better in terms of delay. Assuming logic functionality is unaltered in both cases, purely from a delay perspective is a NAND better or a NOR better which one is better?

Student: NOR.

Why?

Student: (Refer Time: 01:58).

Correct, but the problem there is you I mean that seems like a first correct intuitive step to the answer. But the problem is I cannot even answer this question meaningfully unless I normalize the input capacitance of both these gates. Why because the delay of this path is determined by delay of three gates right. Determine by delay of this inverter by this guy or let us say I am looking and delay only from here to here, the last one is just a load. Let us assume. Then it is determined by delay of two gates; one is delay of the inverter and then the delay of my device under the test which is either NOR or NAND correct.

Now, delay of the inverter depends on what load capacitance that inverter is see, we just derived the whole expression we derived there is a load component to the delay and there is a parasitic component to the delay. Now in order to compare these two I have to first say that this input capacitance offered by this NAND gate. So, let me call it as C in and this input capacitance should be the same, only then the delay of this inverter and this inverter will be the same. Are you following me here?

What I am basically saying is he is he made a point that the NOR gate had larger delay, but I can upsize by NOR gate you understand. To now charge the same load capacitance I can make my NOR gate bigger and then opt reduce my delay because you saw that the load component falls off as 1 over k right of the delay.

So, how much can I up size my NOR gate that is the question I am trying to answer here. So, the first thing I have to do is to in order to compare a NAND and NOR which seems an otherwise meaningless thing to do, I have to first normalize the input gate capacitance of both these gates. Only then the delay of I 1 in both cases will be the same, delay of I 1 should be same because path delay is delay of I 1 plus delay of my DUT, which could be delay of NAND or delay of NOR right. So, if I now want my NOR gate to have the same input capacitance as that of a NAND gate ok. So, I want to find out the following.

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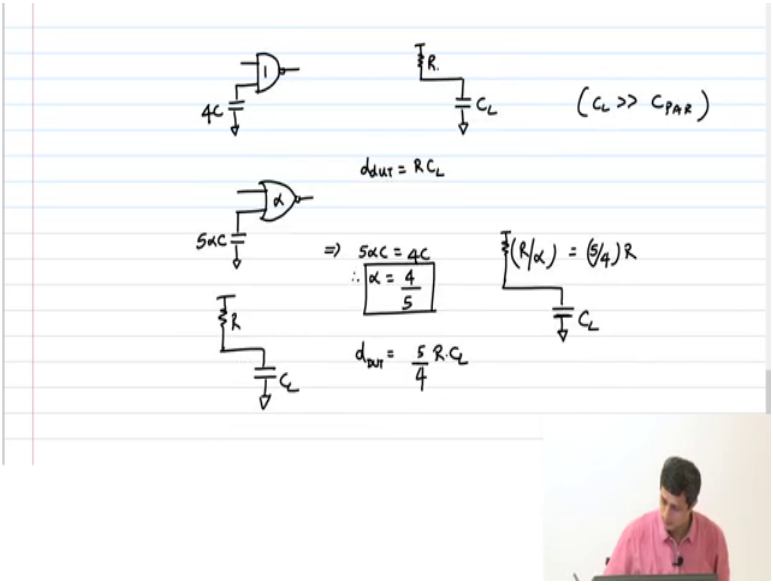

So, if I have NAND 2 gate which has a size of unit size what is the input capacitance here? 4 C. Now I have a NOR gate I am going to upsize this by a factor of alpha. What is the input capacitance of this NOR gate? Yeah.

Student: phi alpha.

Phi alpha into C because a NOR gate has transistor size is 1 1 4 4. So, each input C is a capacitance of phi C and if I up size by a factor alpha I will get 5 alpha C right.

Now, what is my aim? I want to make the input capacitance of these two gates the same. So, I have to choose the alpha so that these two are the same. So therefore, phi alpha C should be equal to 4 C therefore, alpha should be 4 by 5 ok. So, here if I make this 4 by 5 times size of a unit inverter I mean unit NOR 2 gate, then the input capacitance will be the same as that of a NAND 2 gate.

Now I can ask the question which path delay is lesser right. I can now ask that question because I have make sure that the delay of the previous inverter is the same now, it is seeing the same load capacitance in both cases right.

Now, tell me what is the delay due to this NOR gate and what is the delay due to the NAND gate. So, you can draw the equivalent thing it is going to be R right, this capacitance will be R and there will be a CL right plus some parasitic delay ok. Assume that the load capacitance is much larger than the parasitic delay in this case, we will not worry about the parasitic it is a constant number assume that CL is CL much larger than larger than the parasitic capacitances.

So, the delay because of the NAND gate is R into CL right this is my delay of the DUT. Similarly here delay of my DUT for the NOR gate is what it is not 5 by 4, it is resistance is.

Student: (Refer Time: 09:10).

Yeah you are right it will be 5 by 4 R, because the size is let us write that down explicitly R by alpha right and alpha is 4 by 5 and therefore you will get 5 by 4 times R and this has to drive my load capacitance right that 64 x inverter whatever it is. So, this will be 5 by 4 R into C R. Now you compare these two expressions compare these two expressions, obviously the

NOR gate has 20 percent higher delay right or 25 percent correct 25 percent higher delay compared to a the NAND circuit.

What is this telling us it is basically telling us that if I have to present the same gate capacitance to my previous driver stage, then the NOR gate whatever you do will have a lesser drive strength on the resistance compared to a NAND gate and this is not a function of up sizing the gate nothing it is purely because of the logic function that is being implemented, one is a NAND which has 2 NMOS tax other is a NOR which has two PMOS tax.

And therefore the gate capacitance is going to be higher for a NOR gate for the same drive strength, this is one way to look at it or the other way to look at I told you. If I want to present the same gate capacitance to the previous stage then the NOR will necessarily have lesser drive strength in the resistance.

That is what the meaning of logical effort is purely because of what logic you are trying to implement you pay a penalty in terms of how much capacitance you will offer in order to obtain a certain resistance at the output. I cannot do both what I mean is if you take a NOR and say I will upsize the NOR and then reduce my delay to charge CL right. I could the other option right, for example here I will say let me not do it this way I will keep my unit NOR gate as it is right in which case the delay to charge CL, will just be R and CL right. If I use the unit NOR alpha equal to 1, but if you did that then the capacitance that it offers to the previous gate will be phi C, whereas the NAND offered only 4 C.

So, there is a trade off in how much capacitance you can offer to the previous gate to how much drive strength I can get to charge the a given load capacitance, this trade off is captured by what is known as the logical effort. The inverter because it has no stack no NMOS no PMOS stack has the best logical effort of one defined to be 1 ok. Any other gate the moment you implement any logic there is bound to be some sort of a logic stack, which means your capacitance goes up because you have already upsize the gate a little bit right by a factor of two or three or whatever it is. In order to reduce normalize the resistance that is what logical effort is all about.

So, if I give you two gates and say logical effort of gate a is less than logical effort of gate b. Then it means that it is better to use gate a than gate b, because I can get the same drive strength by presenting a lower gate capacitance to the previous guy using gate a than gate b. Any questions? Yes.

Student: (Refer Time: 13:59).

Yeah.

Student: (Refer Time: 14:04).

Ok.

Student: (Refer Time: 14:15).

No I understand, so do not go into that in that case what I will do is I will not compare it with a unit NAND and a unit NOR, I will say you upsize the NAND also by 20 x and then this you compare accordingly then no problem. So, do not worry about that aspect right now right. So, let us assume that those widths are allowed I am just trying to give you an intuitive picture of what logical effort is, all I am trying to say is you cannot achieve higher drive strength by upsizing the gate without resulting in higher input gate capacitance to the previous stage. Your delay will get affected either to itself it is own delay will get affected or the previous guys delay will get affected. This is the idea behind logical effort so.

In fact, that is the reason why we have made it as why we express the delay as output load capacitance by input load capacitance, fix that input load capacitance and then write it in terms of the topology of the gate right. So, if you look at in out here I can write down the delay in both paths let me do that actually right.

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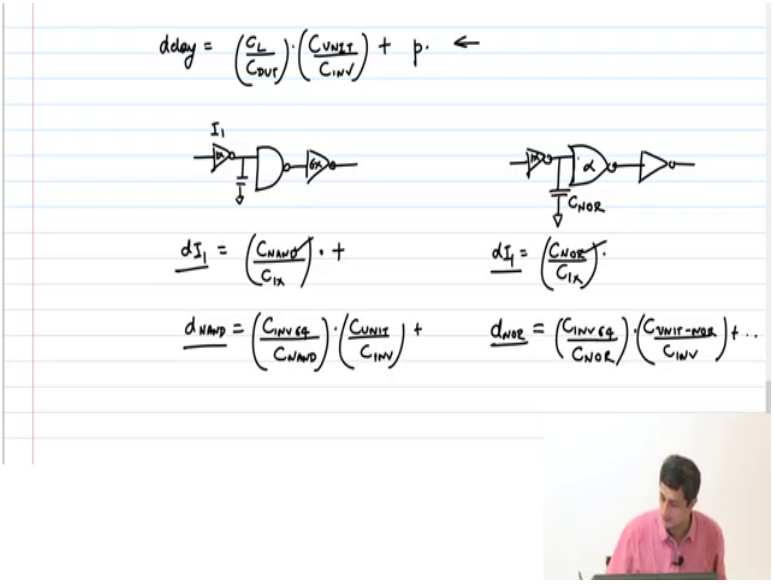

So, we said delay was C l by C DUT into C UNIT by C inverter right plus some parasitic delay, in path one I had it like this. So, delay of inverter I one by the same formula out here is output load capacitance right that is C NAND right pi this is a 1 x inverter C 1 x thing into C UNIT inverter by inverter that is the same capacitance basically right plus something.

Similarly, the NAND delay will be I have an inverter here which is 64 x right C inverter 64 x by C NAND into C UNIT by C inverter plus the parasitic delay. On the other hand if when I took the second path this is 1 x this was sized up by a factor of alpha and alpha was 4 by 5, but we ensured that these two capacitances are the same right. So, d I 1 is C NOR by C 1 x right into something d NOR is the again the 64 x capacitance, 64 divided by C NOR into C UNIT NOR by plus some parasitic delay.

So, what we ensured was C NAND and C NOR are the same when we sized and we got this 4 by 5, 5 by 4 and all we said these two are the same. Therefore, these two delays have to be the same, now I can compare just the delay of the NAND and the NOR and tell you which of these two paths is better is what we said right. So, this is the idea of logical effort.

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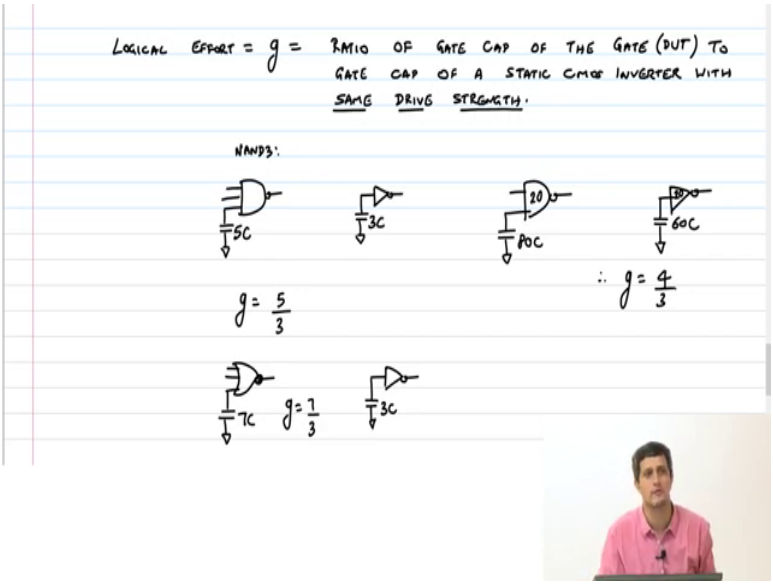

So, what is Logical Effort formally it is called g, the variable is g. It is basically ratio of gate cap of the gate right with all the DUT device under test, to gate gap of a static C mos inverter with same drive strength right. This term in the delay I am calling as g logical effort ok. So, if I asked you for example, what is the maybe we do not have to do all that what is the logical effort of a NAND 3 gate.

NAND three gate what is the input capacitance?

Student: (Refer Time: 21:14).

45 right PMOS is all of them are to each NMOS because, they are three NMOS on the stack each NMOS will be 3, so net capacitance will be 5 C ok. And I am now going to compare it with an inverter of the same drive strength remember. What is the inverters capacitance yeah?

Student: (Refer Time: 21:46).

Sorry?

Student: (Refer Time: 21:47).

Three C therefore, logical effort is 5 by 3 ok. If I have a NOR 3 now what is the input capacitance what are the sizes for not three first of all NMOS is all 1 1 1 PMOS will all be 6 6 6. So, net gate capacitance will be 7 C I am now going to convert compare this to an inverter with same drive strength which is 3 C. Therefore, logical effort is 7 by 3. So, clearly as you can see more transistors you add to the stack in order to get the same resistance, we already started up sizing those transistors the net pull down the resistance we wanted to make it R.

So therefore, we kept up sizing these transistors which means that the capacitance offered to the previous stage is going to go up now and that is captured by the logical effort. How much ever you size up size your gate by you know by increasing drive strength and all that you will pay this penalty of drive strength versus capacitance that it is going to offer. So now, let me ask you this question suppose I have a NAND 2 which is which is has a drive strength of 20, that means what is the input gate capacitance twenty into.

Student: (Refer Time: 23:51).

Eighty C right what is the logical effort of this NAND gate yeah.

Student: (Refer Time: 23:53).

Same thing because you have to underline this part of the of the definition, compared to a static C mos inverter with same drive strength. So, if I want to compare this with an inverter with same drive strength the inverter should also be stronger by the same factor right. So therefore, I will make this stronger by 20 x and you will get a capacitance of how much 60 C and therefore g will always be 4 by three for a NAND 2 gate with whatever drive strength. And that is understandable because it is called logical effort which means it depends only on the logic that is being implemented by that particular gate.

Clear this may take some time we will do more examples in the next class we will start using it more and more and hopefully it should become clearer as you go along. But go back and think about what I told you today especially, how I compared NOR to a NAND why did I normalize the input capacitance, why did I do a only then you will see the whole picture emerging out of this ok. So, we will meet tomorrow morning we will start with a quiz again as usual ok.

Thank you.