Digital IC Design
Prof. Janakiraman Viraraghavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture – 39
Gate Delay with a Load Capacitance

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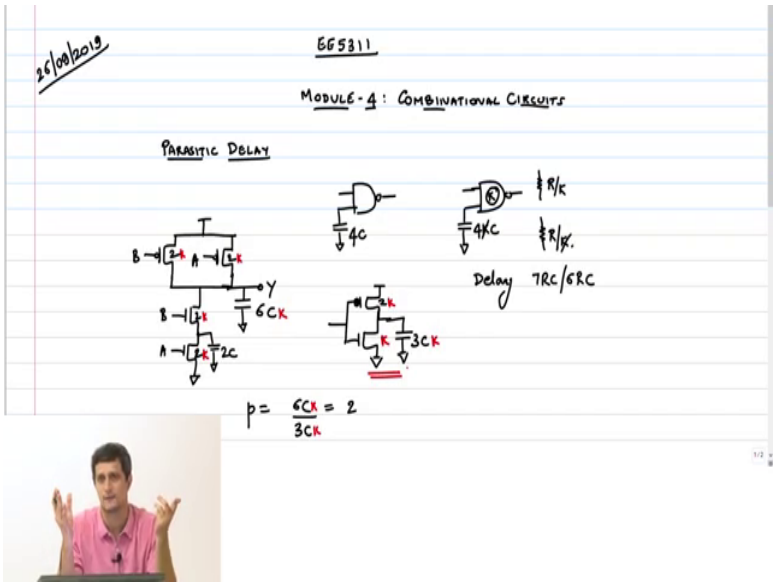

So last class we summarized our discussion on Parasitic Delay, right. And we basically said that parasitic delay is independent of gate strength, drive strength, right. And what do I mean by drive strength? Is I have a NAND gate of unit width, of not unit width a unit NAND 2 gate; then if I have another NAND gate which has a drive strength of K, it means every transistor is upsized by a factor of K in this gate. What does that mean? It means that, if the input capacitance of this unit NAND 2 is 4 C; then what is the input capacitance of this NAND 2?

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Yeah? 4 into K C, right. And the resistance will drop now; it will become R by K, R by K. And because the two K's will now cancel, your delay will still be just the old expression; either it will be 7 R C or 6 R C or whatever it is, right.

So, to a first order parasitic delay was independent of gate drive strength. This was the key conclusion that we came to last time and I also asked you to make an approximation instead of doing all this complicated Elmore delay type of evaluation for delay each time. You just count the capacitance on the output node; diffusion capacitance of the output node and divide it by the diffusion capacitance of an inverter, you will get the normalized parasitic delay, right. So, let me just remind you about that once. So, if I have right A, B right; then this capacitor, capacitance parasitic capacitance is 6 C right; size is 2, 2, 2 and 2, ok. If this is 6 C, you just divide it by the capacitance of a unit reference inverter; 1, 2 and this is 3 C.

So, the parasitic delay P will simply be 6 C by 3 C; basically the R is the same, the gate has been sized, so that the R is effectively the same, right. That is how we started; therefore, you I am leaving that R out automatically and you are going to get the normalized delay as 2. What are we leaving out here?

We are leaving out this 2 C effect, which is what made it 7 C earlier, right when we did all the calculations. But I am I am not saying that is negligible; I am saying it does not matter in light of what we are going to do in a couple of classes which you will see, ok. So, this approximation is do not get carried away with parasitic delay too much is all I am saying; because it is independent of gates sizing that is the key thing that I want to convey here, ok.

Now what if this gate was upsized by a factor of K? So, you should divide it by the capacitance not of the reference inverter always, by the inverter which has the same drive strength. So, this also has to be K, K; then this will become 3 K C right, then it will become 3 K C by K C and then you will still get 2 as the answer. The bottom line is if I scale the transistors by the same amount, delay should not change.

So, when you are doing this normalized delay calculation, it has to be done with reference to the inverter which provides the same drive strength as your NAND gate at hand or the device at hand. For a NOR gate it will be a different thing again, right. The reference inverter and the you know the inverter here might be the same as long as I scale NAND and NOR by the same amount it does not matter, clear. This is just an approximation we will come back to this a little later ok.

We will use more of this later and we will come back to it.

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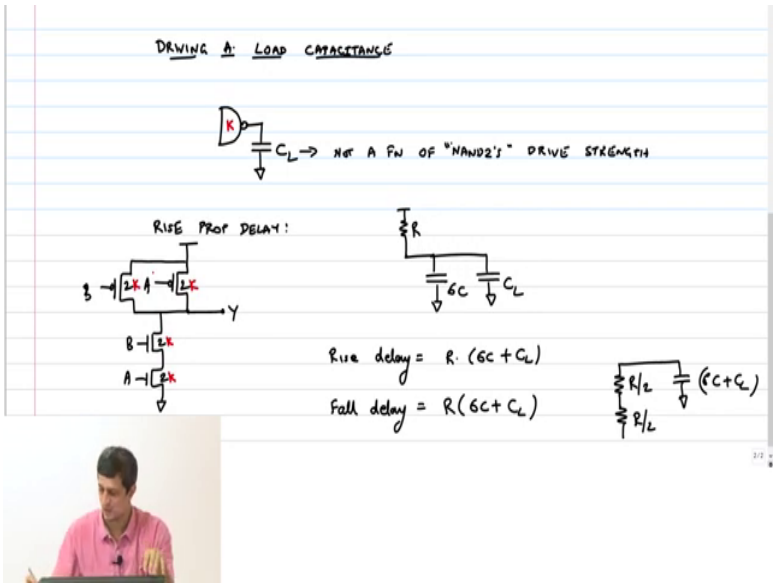

Now, I want to move on to driving a load capacitance. What I want to now do is I have a NAND; of course, there are its own parasitic capacitances, but I now want to drive a fixed load capacitance C L. And then I want to see how does the delay equation change, right? Because this is the most realistic scenario that you are going to encounter; the gate is driving

another gate and therefore, there is an external load capacitance which is fixed, right. And most importantly this is not a function of NAND 2's drive strength; it is not a function of that.

So, if I upscale the NAND 2 by a factor of K this capacitance does not scale, it is a fixed capacitance; because the capacitance is coming from outside from some other gate, ok. So, let us go ahead and look at again the rise propagation delay. So, what is the equivalent circuit? I have R right from the PMOS of the NAND; then I have its parasitic capacitance. How much is the parasitic capacitance for the NAND at the output node? 6 C; 2 C from each two PMOS and one 2 C from the NMOS; 6 C and then I have a C L, right. Therefore, the delay is now simply going to be R into 6 C plus C L.

Similarly the fall delay right, this is rise; fall delay will be how much? It could be the same thing, it could be 6 R C plus C L right 6 R into C plus C L; no, R into 6 C plus C L or it could be that other Elmore delay that you want to apply. Let us not worry about the intermediate capacitance for now, ok. So, I am going to just consider this case for the fall, R by 2 R by 2 and a net capacitance of 6 C plus C L. So, this will be R into 6 C plus C L,.

Now the question is what happens if I increase the drive strength of this gate? This NAND gate I am now going to make it stronger by a factor of K; which means all transistors in this gate will be upsized by the factor K. Therefore, just to make sure people remember that notation let me sorry maybe A, B. So, now, I am saying this was 2, 2, 2, 2; now I am making it 2 K, 2 K, 2 K, 2 K, right.

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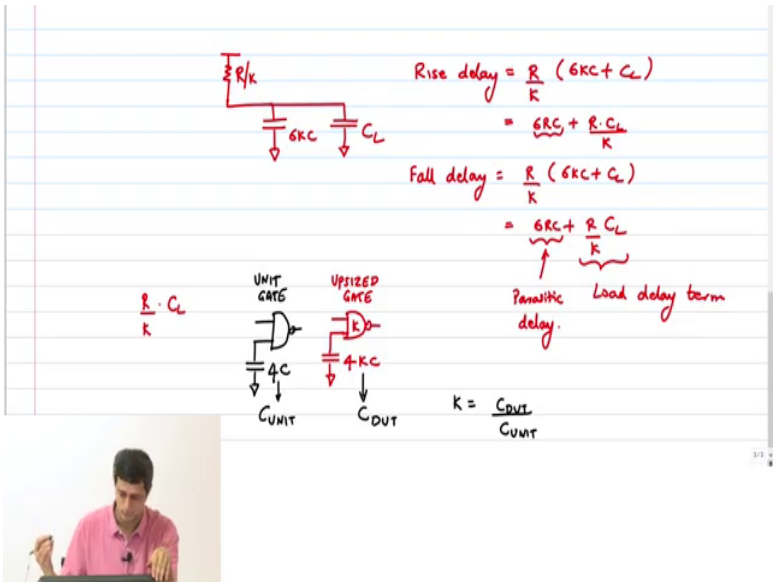

Therefore the equivalent circuit will now become R by K, right. I have sorry I made the transistor bigger, resistance will drop, right. What is this parasitic capacitance? 6 K C.

But the load capacitance now remains the?

Student: Same.

Same, right; and therefore, rise delay on upsizing will become R by K into 6 K C plus C L. This I can further simplify as 6 R C plus R into C L by K, ok. So, now, what does this tell us and similarly fall delay will be no different by the way; it will also be just R by K into 6 K C plus C L, no difference plus R by K into C L. So, what is this tell us now? The delay has two components; one is a parasitic delay which is completely independent of the gate size that we have chosen or the gates drive strength that we have designed, right 1 x, 2 x, 3 x it does not

matter, the parasitic delay is a fixed number. On the other hand the load the delay that is incurred in charging the fixed load capacitance falls as 1 over k; which is totally understandable, because that is a fixed load capacitance. And what I am doing by increasing my transistor size is to reduce the resistance; which means, the delay has to fall over all, right. So, this is the load delay term, this is parasitic,.

But it is not that we are done with the delay whatever partition; we can partition this even further and get many more insights into the delay of logic gate in general, ok. So, let us look at this term R by K into C L. What is K? So, this is my upsized gate and this highly capacitance of 4 K C, ok. This is my upsized. What about a unit NAND gate? This is just 4 C.

So, if in general for any logic gate I can write this as C unit; the gate capacitance presented by a unit gate, right. I told you for NAND gate the unit gate is 2, 2, 2, 2 sizes; for a NOR gate it is 1, 1, 4, 4 right NOR 2; NOR 3 it is 1, 1, 6, 6, 6, 1, 1, 1, 6, 6, 6. Like that if you define a unit gate; then whatever capacitance that unit gate presents, we will define as C unit. And this guy is my capacitance of the DUT, device under test, right. In my slides I have called it C gate C g a t e; but maybe this DUT might be better, ok. So, the factor K is nothing, but the ratio of the capacitance of the device under test which has been scaled up by some factor divided by C unit, right.

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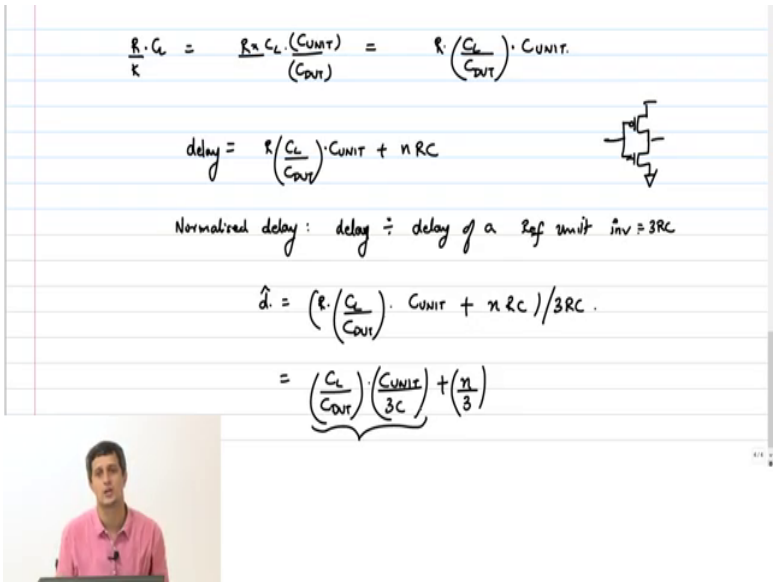

Therefore I will now write this R by K into C L as R by R into C L into K was what C device under test into C UNIT, ok. So, I am going to write it like this, R into C L by C DUT into C UNIT, ok. Now what is the net delay? What is the net delay that we had? The load term R into C L by C DUT sorry into C UNIT plus some n times R C; where n will depend on the gate whether it is a NAND, NOR whatever it is, ok, but some number multiplied by R C.

So, now, what I will do is; I will to get the normalized delay, why normalized delay? Because it is enough if I characterize just the inverter. In a new technology if I characterize the inverter and get the delay; then all the other delays are fixed if I normalize to the inverter delay, right. So, that is why we are going to normalize all the delays to the delay of the inverter, ok. Normalize delay is delay divided by delay of a reference unit inverter, ok. So, d hat is a normalized delay is R into C L by C UNIT. And what is the delay of a reference unit inverter

which is driving no load? See this, I mean there is no load here. So, what is the delay of this inverter?

So, this is nothing but 3 R C, ok. So, I am going to plus the parasitic delay n times R C whole divided by 3 RC. So, now, what happens your R is gone; you will get C L by C DUT into C UNIT by 3 C plus n times n by 3, right. What was this by the way? This was nothing, but our normalized parasitic delay; but we had, you just count diffusion capacitance on the output and divide it by the diffusion capacitance of the corresponding inverter. You will get the answer there and you get just n by 3. So, for a NAND gate n equal to 6, you will get parasitic delay of 2, normalized parasitic delay of 2,.

So, let us now more carefully look at what this term means, ok.

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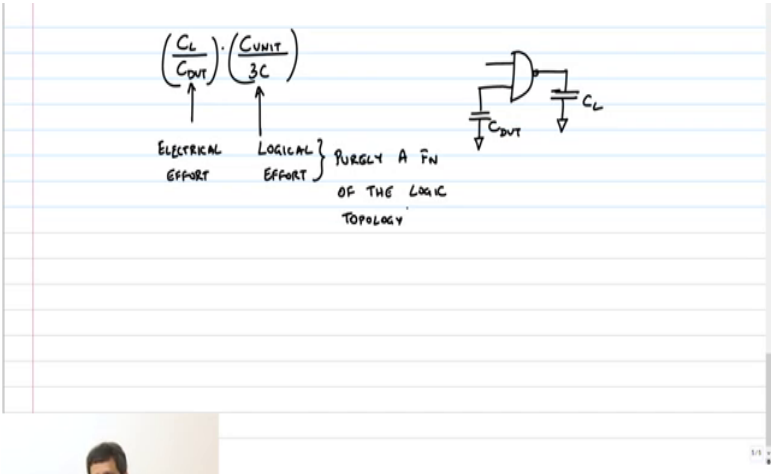

So, we have the delay normalize delay defined in terms of C L by C DUT into C UNIT by 3 C. This is basically just ratio of the output capacitance of that gate to its input capacitance, right. So, if I have a NAND gate which is driving a load like this; this capacitance and the input is C DUT, this is C L. So, delay is just one of the terms in the delay is just ratio of output capacitance to input capacitance presented by that gate, ok, this is just one of the terms. This guy is called electrical effort,.

Now there is another term which is basically the ratio of the unit gate capacitance; the unit gates capacitance to the capacitance of an inverter that is called logical effort. Why is it called logical effort and why is the other thing called electrical effort? Electrical effort is, it is because it has to actually charge that particular capacitance value, ok. It has to do the work to charge that capacitance in that particular circuit whatever value there is.

On the other hand logical effort has nothing to do with what load capacitance there is, what input capacitance there is; it is purely a capacitance that arises because of the topology of the gate. If you implement an inverting function, inverters function; y equal to A bar, then the logical effort is minimum. Anything more than this, you are going to pay a price; what price we will see. But this logical effort is purely a function of the logic topology. How many transistors you have on the NMOS stack, how many transistors you have on the PMOS stack; this will purely determine what the logical effort of the gate is, ok.