Digital IC Design
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Lecture – 38
Parasitic Delay

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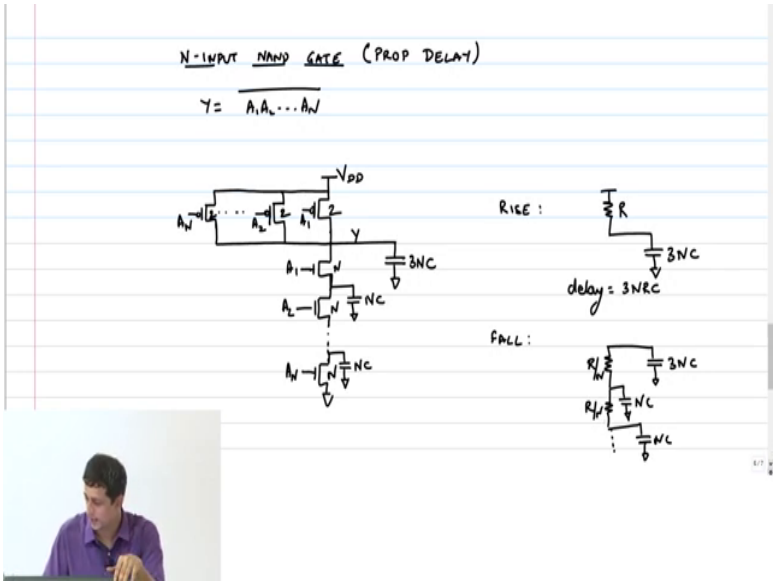

But now can you extend this same thing to an N input NAND gate right. Y equal to A 1, A 2 AN. First draw the circuit get the sizes right then evaluate the delays and only propagation delay. So, what is the size of the PMOS transistors for an N input NAND? All 2 no change is there right for a NAND does not matter how many inputs PMOS is always is 2 what is the size of the NMOS? N. So what is the total output capacitance?

Student: 3 N (Refer Time: 05:23).

3 N in to C. What is the intermediate capacitance of each of those nodes? NC, they are all shared uncontacted diffusions NC, ok. So, the rise let us first do the rise in propagation delay; rise is very simple, what is the answer? 3. Let us also draw the equivalent circuit it is basically a single R with 3 NC right therefore, rise delay 3 NRC what about fall? So, let us get the equivalent circuit right first, I have 3 NC what is each resistance in this network? R by N, going to a capacitance of NC R by N and so on.

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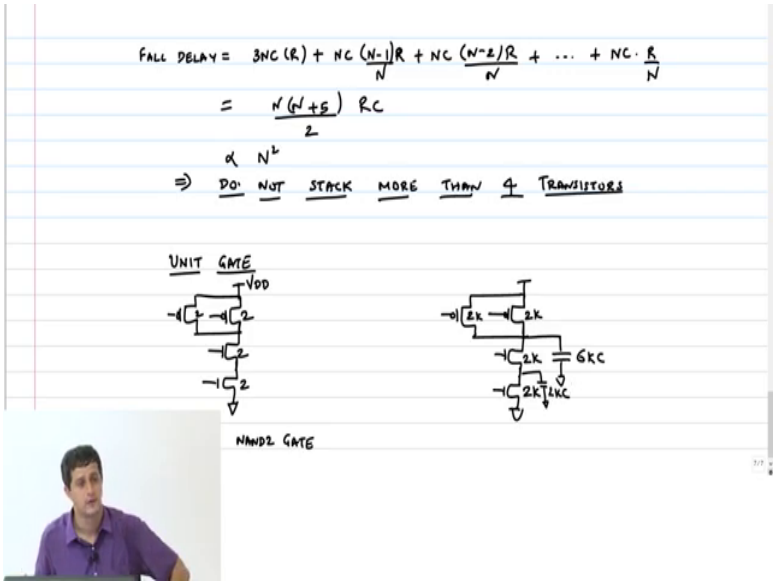

So, what do you get as the final answer? You will get 3 N; 3 NC right; 3 NC into R plus NC into N minus 1 N minus 1 by no, I have R by N and I have N minus 1 of them right. So, N minus 1 R by N correct, plus NC into N minus 2 R by m and all the way down to NC into.

Student: (Refer Time: 07:55).

R by N. So, what does this evaluate to? Yeah, N into N plus 5 by oh N plus 5 by 2 ok; sorry is this correct ok. Go back go back and evaluate it that is not the that is not the point of the discussion here.

So, what is it that you note? Whole by 2 yeah that is what even I thought but does not matter anyway that is beside the point go back and check the answer. The key point to note is, that the this delay by the way is called the parasitic delay of the gate; because this delay is coming in because of its own capacitances its not that we have added any load capacitance to this gate, just because of its own diffusion capacitances right.

Think about it we have not considered even one gate capacitance here right that is that is what will form the load capacitance on the next gate. These are all just diffusion capacitances from its own layout and that grows as N square or maybe I should say N square use N delay grows as N square.

And therefore its not a very good idea to make logic circuits with more then 4 input NAND gates or 4 input NOR gates. If you want to make a 6 input NAND gate, then you split it up as 2 3 input NAND gates and then combine them appropriately in the logical logically correct way right. So, the key conclusion here is do not stack more than 4 transistors.

In general PMOS or NMOS; PMOS will actually be worse doubling the capacitance everything. You will see later there are other reasons also why we should not do this therefore, its a generally good idea that people stopped with 4 input NAND gates ok; typically 3 is preferred but at most 4 not more than that ok.

So, now let us proceed with another interesting thing, because it's not possible for me to do achieve the timing that I want on the circuit with just these unit gates when I say a unit gate, let me define what I mean unit gate. So, for example, a NAND 2; 2, 2, 2 and 2 this is what I call a unit NAND 2 gate.

Just like the reference inverter where we had the size of 1 and 2 for the NAND I am saying the unit gate is 2, 2, 2, 2 all sizes. For a NOR it will be 1, 1, 4, 4 which is my unit gate right. These gates unfortunately are not sufficient to solve my timing purposes you know timing constraints because they have limited driving capability. The current is limited by the fact that the width is 2 right there is only so much current that he can deliver.

And therefore, it cannot be used for example, to charge a very large load capacitance therefore, we need to do something known as gate upsizing we will upsize a gate by a factor of K. So, what does that mean? I will simply say that I increase the size of every transistor on this logic gate by a factor of K; so, I will make this 2 K, 2 K, 2 K, 2 K ok.

Now, I want you to calculate the 4 components of delay for this configuration; rise fall, propagation, contamination delay. Before we do that can you tell me what the capacitance on each node is? What is the capacitance on the output node? 6, 6 K C. What is the capacitance on this node? 2 KC, very good. Yeah, now can you tell me the delay?

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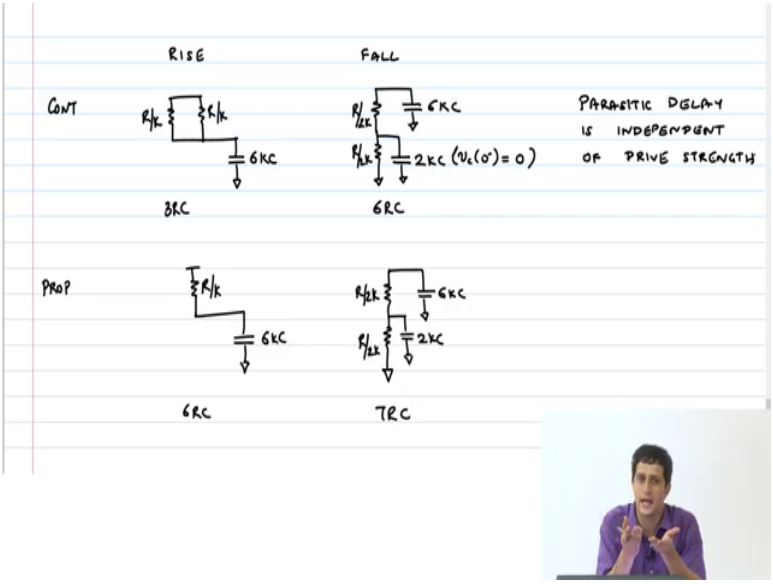

Student: (Refer Time: 14:27).

So, for rise delay what is the value of each resistance of the PMOS transistor? R, So, you get 2 R by 2 K; so, you get R by K; R by K. And this is what about the NMOS R; R by; R by 2 K. So, its only for the PMOS that you have to do 2 R by W for the NMOS it just R by W. So, do all of you get these four equivalent circuits first correctly ok. So, now, tell me the delays numbers here contamination rise how much? 3 RC here fall contamination fall.

Student: (Refer Time: 17:21).

Propagation rise 6 propagation fall RC. What is the key conclusion you get from this?

Student: (Refer Time: 17:39).

Parasitic delay to a first order is independent of the gate size or the gate drive strength; because this thing of sizing it up by a factor of K is making it a stronger gate you are giving it more dry strength but parasitic delay is independent of drive strength.

So, parasitic delay is independent of drive; why is that, because when I upsize a transistor the capacitance goes up by a factor K; the resistance falls exactly where the same factor K and its RC which is the delay. And therefore, they cancel out the to a first order this is true ok. Now, because of that the fact that it does not depend on delay what we do is, we do not worry about all this contamination delay and all that stuff.

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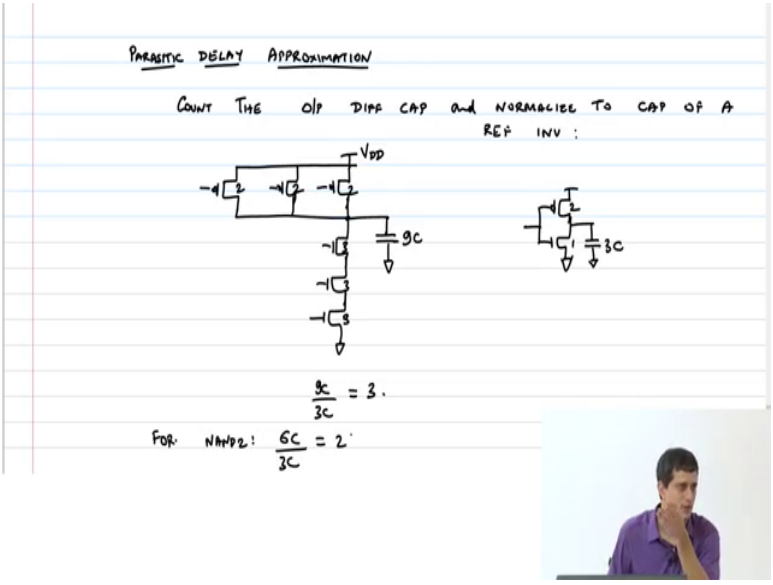

We just simply look at the output approximation, simply count the output diffusion gap let me say ok. So, if I have for example, NAND 3, what is the net cap here? 3, 2, 2 and 2; 9 C right, you count the output diffusion cap and simply divide it by the cap of a reference CMOS inverter you will get the right this is my reference CMOS inverter 1 2; capacitance output diffusion capacitance is 3 C.

So, you basically just count the output diffusion capacitance of the logic gate and divide it by the diffusion cap of your reference CMOS inverter; you will get the normalized parasitic delay ok. What I am saying is, instead of that 7 RC I am just saying make it 6 RC it does not matter whether its 7 or 6 because when I upsize the gate it does not change that number does not change.

In some sense when I do gate optimization later you will find that this parasitic delay is just a constant addition and it does not alter any of my gate sizing algorithms. And therefore, I do not need to worry about these gory details, when I am doing my calculations whether its contamination delay or propagation delay or whatever.

So, its a very reasonable approximation to make that as follows. Count the diffusion capacitance on the output node and divide by the diffusion cap of a reference CMOS inverter, you will get the normalized parasitic delay right and normalize to cap of reference inverter. So, the delay will simply be for this will be 9 C by 3 C equals 3; what will it be for a NAND 2? 2 right; so for you will get 6 C by 3 C equals 2. So, we are not considering that case where the propagation delay had that 7 RC you are saying effectively is just 6 RC ok.