Digital IC Design
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Lecture – 37
Gate Delay

Good afternoon. Let us continue with our discussion on the capacitances right. So, last class, we concluded by discussing about the capacitances of various nodes in a NAND gate, right and we discussed the concept of a shared uncontacted diffusion versus a shared contacted diffusion right.

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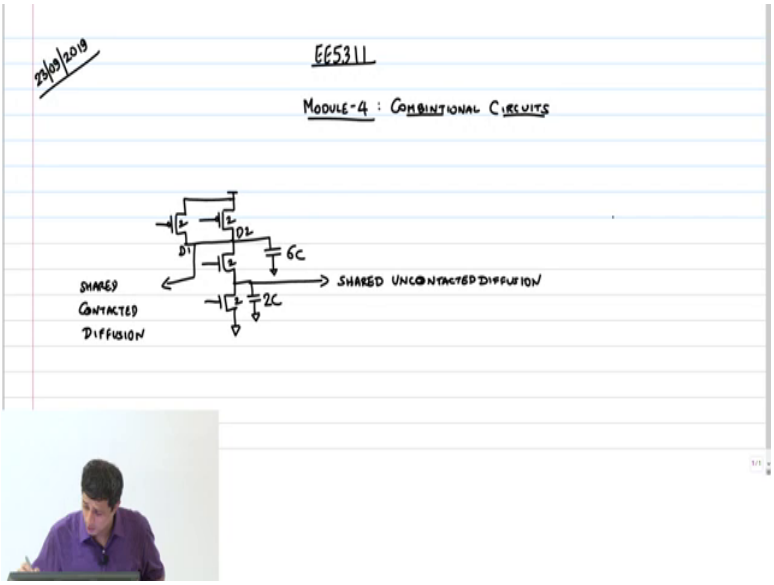

So, if you had a NAND gate like this right size 2, 2, 2 and 2 right, then the net capacitance here would be 6C; 2C coming from each of the two PMOS's right and one 2C coming from NMOS on top. The intermediate node would have a capacitance of only 2C as opposed to 4C

because this is a shared uncontacted diffusion node right. So, this is a uncontacted diffusion. Whereas, if you look at the 2 PMOS transistors even though the drains of both PMOS transistors you know drain 1 and drain 2 are shorted they are a contacted diffusion and therefore, you need more space.

So, effectively the capacitance goes up because of that race it is not like you have just one diffusion there for both these transistor there are two diffusions and you have to have a have to have sufficient space to connect these two diffusions together with a metal and therefore, this will basically be a shared contacted right. And therefore, each of the nodes will contribute to a capacitance of W into C, clear?

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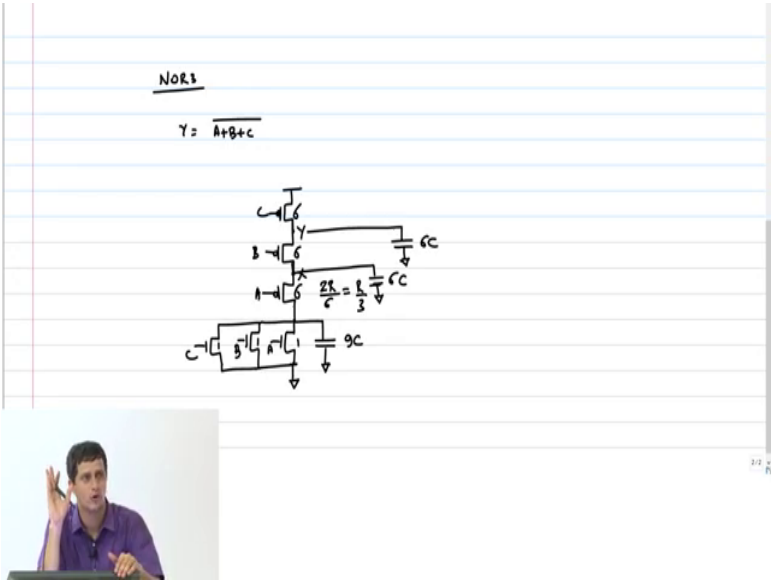

So, now let us go ahead and use this concept to figure out what the capacitances offer NOR let us say a NOR3 gates straight away right. So, first can you sketch a NOR3, Y equals A plus

B plus C whole bar? So, how many transistors on the PMOS stack? It is a 3-stack thing right. So, yeah A, B, C; A, B, C, right. So, what are the sizes of the NMOS transistors? 1, 1, 1 right because the worst case is only one of them turning on. PMOS? 6, 6 and 6 right. So, this is 6, 6 and 6. So, remember I told you that the resistance of a PMOS transistor with W will be 2R by 6, 2R by W right.

The normalized resistance will be 2R by W and therefore, the this will be R by 3 and you add 3 of them you will get a net resistance of R on the pull up path as well. So, what are the capacitances now at various nodes? What is this capacitance? From the NMOS how much what is the capacitance? 3C right. From the PMOS, how much of capacitance will you get on the PMOS? 6C. So, this is 9C. Now, what kind of a node is this node X, node Y? Shared uncontacted diffusion again. So, therefore, I can put a capacitance of how much, 6C here; similarly, Y another 6C ok.

So, remember that this shared uncontacted contacted diffusion only in this NAND and NOR case simple cases it is easy to figure out without doing the layout otherwise you have to go into the layout to figure out what happens ok. So, we are not worried about those things right now. In the sense that ultimately when you when you do a simulation with the layout extracted net list you will get all that information appropriately right.

But, it is not easy to always say that if I give you any arbitrary circuit how many of them will be shared un contacted or how many of them will be shared contacted diffusions that depends on how you lay them out right and it can vary from person to person there will be multiple ways of doing it also right.

So, this is just something to keep in mind where when there is clearly a shared uncontacted diffusion do not double count the capacitance. That is the that is a very reasonable approximation and it is it is also valid in reality right, but it is not easily extendable to every single case of layout that we do ok right.

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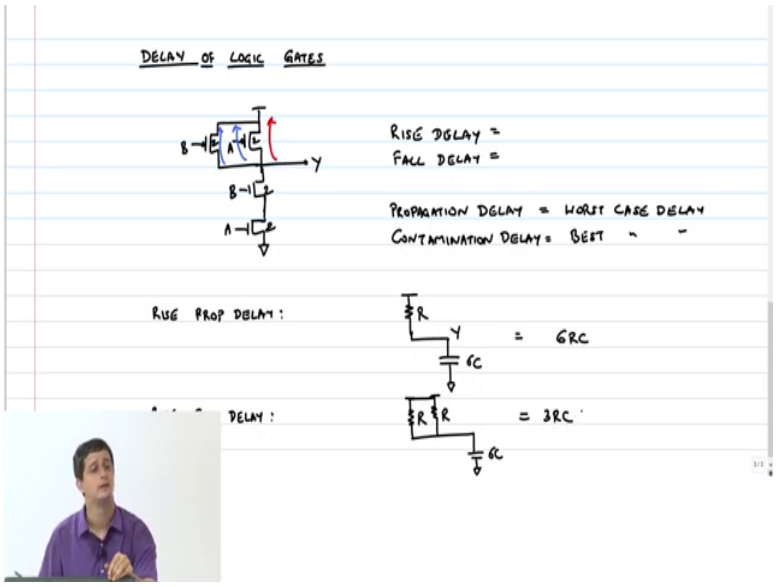

So, with that we can now start calculating delays of logic gates ok. So, let us start with a simple NAND2 example. I want to calculate rise and fall delay ok. Now, sorry, in each rise and fall there are two kinds of delays that we will see, the worst case delay and the best case delay ok.

Why is that because for example, if you take the rise delay only one transistor pulling up the output would be the worst case delay, right. If this happens then it happens through resistance of R and therefore, that is going to be your worst case delay. On the other hand if it gets pulled up by both transistors together, then it is an R by 2 resistance and therefore, that is your best case delay right.

So, the definition of these two delays is I have for each of these two I have something known as propagation delay and contamination delay. So, this is your worst case delay, this is your

best case delay. Contamination has a negative connotation to it because in sequential circuits contamination delay can actually affect your circuit quite significantly because data can raise through the gate and go and affect your flop in the next stage right.

While the flop is trying to capture data of this particular state data of the next state can just race through and go and contaminate that flop and therefore, it has a negative connotation to it. It is called contamination delay right that is all, but just keep these two in mind for now.

So, now I want you to calculate rise propagation rise fall delay I mean rise propagation rise contamination; fall propagation fall contamination delay ok. So, let us start with rise propagation delay. So, what is the equivalent RC circuit first for this? Yeah rise propagation delay.

Student: (Refer Time: 12:03).

Yeah, there is just one resistance R right size of course, is 2, 2, 2 and 2 right then there is a capacitance which has to charge up and what is it capacitance value and output node? Yeah 6C right. So, the delay is how much 6 into RC right. What about rise contamination delay? What is the resistance? Yeah. So, I will write this explicitly both resistance is turned on 6C you will get what? 3 RC as my delay.

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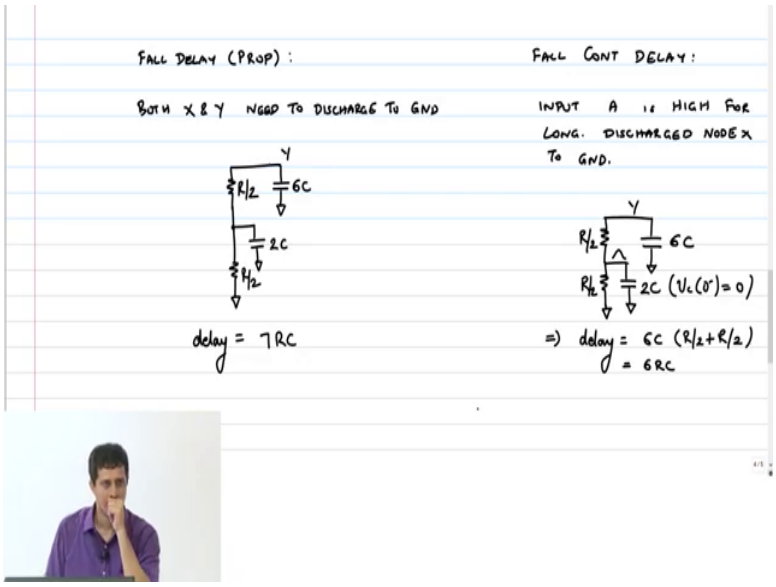

So, now let us come to the fall delay fall delay propagation ok. So, I have: I have my output or maybe I should start with contamination delay what is the what is the case for contamination delay? Louder, I cannot hear.

Student: (Refer Time: 13:54).

I just cannot here today maybe because I am little down, but. So, the bottom transistor suppose that input was high for long enough and it has discharged that intermediate node X to ground already right then the output Y needs to be pulled down to ground that is all.

As opposed to if the out A input also had to discharge the input X to ground then it is both these nodes that had to be discharged to ground at some point. So, therefore, the contamination delay is right sorry, fall contamination delay input A is high for long right and

discharged node X to ground. Therefore, if you look at the equivalent RC circuit you have the node Y with a capacitance of 6C, you have a resistance of how much how much?

Student: (Refer Time: 09:51).

R by 2, NMOS size is 2 right R by 2; 2C is the intermediate node capacitance, but that has already been discharged to ground right. So, therefore, if you remember this problem I gave in the quiz where one of the nodes was already discharged slightly, then you apply that condition and that thing will just vanish that capacitance will vanish ok. It does not mean that the resistance will vanish that is the key point here. The current still needs to go through that bottom NMOS transistor connected to A and that still offers a resistance it is just that the capacitance has already been discharged ok.

And, therefore, the net delay will be will be 6C into R by 2 plus R by 2, 6 RC right. You apply the same thing that we I gave in the quiz initial condition where instead of 3 by 4 V DD I said you should you make that ground, that term will just vanish that capacitance term will just vanish right. But, the on-path resistances will still come for the other guys correct and therefore, that becomes 6 RC ok. For propagation delay both X sorry X and Y need to discharge to ground right.

So, what is the equivalent circuit? I have here I think I should write this V C of 0 minus equals 0 yes, true. So, that is where the approximation that we made for this l node delay model comes in. It is true that this node for it to accommodate some current will actually bump up slightly. So, this is only an approximate answer.

It is not an exact answer that node has to bump up slightly to allow some current and therefore, you will have some charging of this capacitor also slightly in the process and all that stuff. So, those are second order effects. The first order effect is you can neglect that and you will have 6 RC the fact is contamination delay is lesser than the propagation delay in these two conditions as I told you. You can check it out through simulations it may not be exact that is all ok.

So, her question was if this capacitance was already discharged to ground; that means, the V DS of that bottom NMOS transistor is 0. So, how can you have any current flowing through that? So, she is right because for to accommodate some current the V DS has to bump a little bit right.

Only then you can have some current so, but that becomes a second order effect right. So, in the l node delay approximations we made we said that everything falls as V DD e power minus d by RC right. So, those approximations are those are only approximations right. So, you can go check it out in simulation for yourself, but to a first order this is a reasonable approximation to make.

So, node Y capacitance is 6C, I have a resistance of R by 2, 2C R by 2. So, what is the delay? What is your answers 7RC right the l node delay of a model you use you will get 7RC as the answer sorry.

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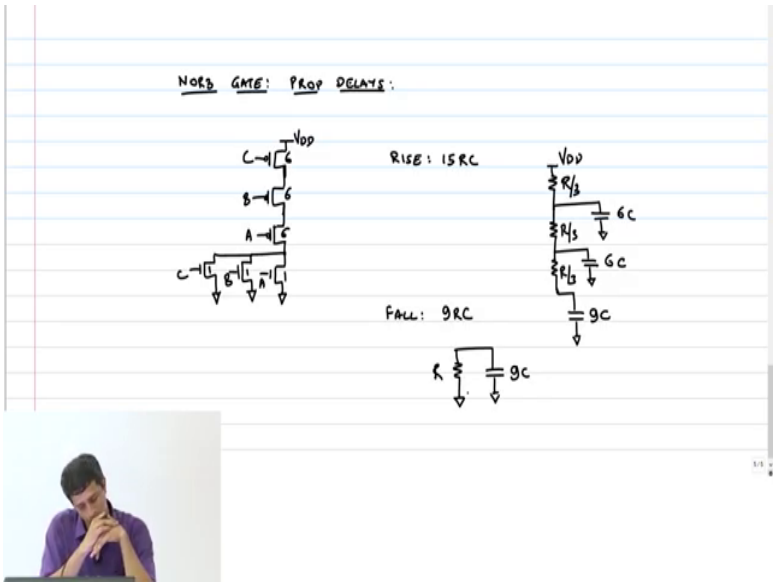

So, can you work out for a NOR3 gate now? The NOR3 gate only the propagation delays, yeah. So, what is your answer? Rise delay, 15 RC right which is 9 into things 6 into 2R by 3. So, R by 3, 4 and yeah 15 RC and fall delay? 9RC yeah, that is very simple because it is just this and 9C and this will be R, 9RC. What about contamination delay? Rise is just 9RC, is it? Correct, exactly and fall?

Student: 3.

3 RC ok.