Digital IC Design
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Lecture - 32
Ring Oscillators and Process Variations

So, in this module we have actually studied quite extensively about the inverter right, that is the only logic gate we have looked at in this entire module question. Now, is what can I what circuit can I construct with just an inverter ok, is there any useful circuit that I can construct with just an inverter. Of course, with NAND, NOR and other gates you can make any logic there is no doubt about it right. Or if I just give you a NAND its enough you can make any logic, but with just an inverter what can you do right.

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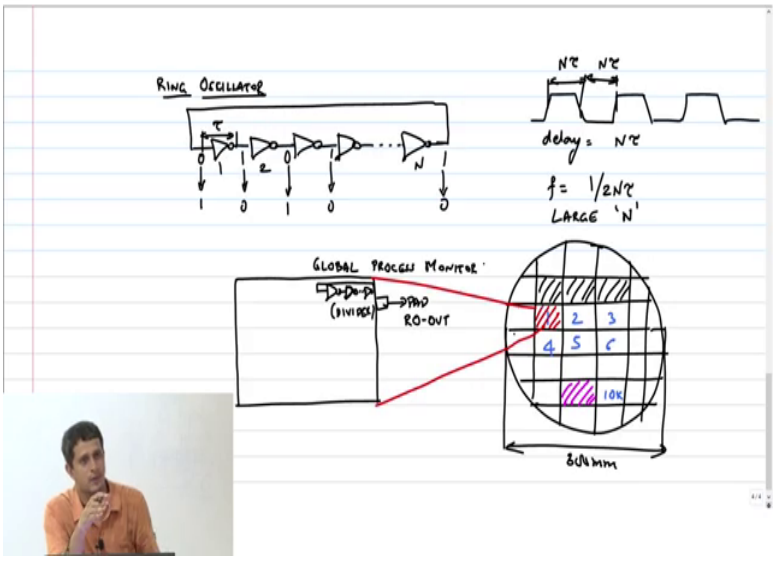

So, it turns out that there is one interesting circuit as follows right, I have a chain of inverters like this. Now, what if I just connect the output of the last inverter back to its input what do you think will happen?

Student: (Refer Time: 01:19).

Right, so what happen if N number of inverses right 1 to N, if N is 2 what will happen?

Student: (Refer Time: 01:31).

It will basically just remain at whatever state it comes to right, because of noise or whatever if there is a 0 at first input. Then the output of the first inverter will be 1, output of the next inverter will be 0 again that is fed back, it will remain in the stable state for ever right. However, if there is and there are odd number of inverters in this chain right, then what happens is let us say that this is 0 ok.

Then this basically will make the output of the first inverter toggle to a 1 after some delay right. So, this will become 1 then this will become 1 after some delay 1 0 and then eventually because N is odd this will switch to a 1 right. And since its fed back right, this will now change to a 1 right and this will switch to a 0 1 0 and this will keep going on and on and on and not surprisingly this is called a ring oscillator. Now where is this circuit useful?

So, it turns out that when you manufacture a particular chip send it for fabricates and you get it back, its not guaranteed that all the transistors are going to come back from the fab as you had expected ok. So, what happens is I have a large circuit right like that microprocessor I showed you which has 8 billion transistors and so on right.

So, it can so happen that when I manufacture these chips one after the other across in a wafer right. What is a wafer? Wafer is basically a circular thing where you have diameter of this would be 300 mm ok. It is a silicon huge silicon subtract ok, and on that what you are going

to do is you are going to manufacture your chips like this, so each block here is basically a chip ok.

So, on a wafer you could have many many chips like this, you know some may be 10 k or something depending on the size of the chip you can manufacture a lot of these unit. Now, this particular chip here chip 1 need not get manufactured with the same specifications on the transistors as chip 999 ok.

So, if you look at it this guy will have one particular bias in the manufacturing ok, which means what does that mean. So, your level one model like we spoke about has a parameter vth naught gamma this that, that vth naught can shift vth naught can shift slightly right. Instead of 300 milli volt it can become 350 milli volt right, all the transistors in that chip by the way that is what I mean here.

Every transistor in this chip 1 can have a vth naught of vth plus delta, this magenta guy every transistor in this can have a vth of vth minus delta right. So, it is not guaranteed that all the chips that come back from the fab are going to come back in exactly the same specification that you had manufactured it that you designed it with.

So, the first thing you need to figure out is where how I mean how different are these transistors from my intended design value ok. So, what you do is in every chip right, so what you see here is this is my chip I am going to put a ring oscillator like this ok. With some odd number of inverters typically this will be a large number, because this what is the frequency of oscillation by the way of this ring oscillator?

Student: F by (Refer Time: 06:31).

Student: F by n.

What is f by n?

Student: (Refer Time: 06:37).

No, so if a if the input switch to a 0 at time equal to 0, how long will it take for the input to switch to a 1?

Student: (Refer Time: 06:47).

Student: (Refer Time: 06:49).

So, let us assume that the delay across each inverter is tau ok. So, what is the delay for the 0 to propagate across all inverters n tau right n tau, now what is the frequency of operation?

Student: 1 by n (Refer Time: 07:15).

1 by.

Student: (Refer Time: 07:16).

1 by 2 n tau because, now that 0 has to become 1, 1 has to become 0 right. So, if you look at the output of this ring oscillator it will go like this right, this is too clean a wave form, but you know it may in look like a sinusoidal wave form in reality by the way. This delay for output to go from 0 to 1 is basically my N tau this is another n tau.

Therefore, the frequency of operation is 1 by 2 N tau ok. So, let us do a quick calculation if N is 30 picoseconds and let us say I mean tau is 30 picoseconds N is 11 what is the frequency of operation?

Student: (Refer Time: 08:33).

Somewhere in giga Hertz right, the problem is if I have an a signal that is oscillating like this at high frequency I cannot bring this out of the chip, what will come out to the chip is only somewhere in mega Hertz ok. So, you have to do lot of things to first of all get this signal out of the chip ok, if you want to do on chip measurement that is a different story right.

But, if you want to get this out of the chip and make a measurement outside then you have to slow this down significantly. So, therefore, what people do is they choose very large N first. So, that the frequency itself is in some reasonable it is still be somewhere in the 100s of mega Hertz range right. Further what you do is you put a divider frequency divider right by 2 by 4 by 8 and then you bring it out right.

So, after all that you can bring this oscillating signal out from the chip ok. So, therefore, you put a ring oscillator which has large number of stages followed by a divider also. And you get this out on a pad ok; this is will be called ring oscillator out ok. So, you can observe this on an oscilloscope right or you know the tester can do automated measurement whatever it is and you can find out what the frequency of operation is.

Now, if all your transistors have gone from VT to VT plus delta, what will happen to the delay? Every transistor is had has got a higher VT now, so what will happen to the current first of all? It will.

Student: Decrease.

Decrease right, VGS minus VTS where it appears, if current decreases what will happen to delay increase right, its c delta v by i you remember that that expression right, so therefore, the delay will now increase ok. So, they the ring oscillators are therefore, used primarily as global process monitors ok, I will tell you what global is? Global process monitor.

What is global mean here? It means that every transistor in this chip has moved by the same amount the VT or all the process parameters right. It not just VT by the way, it could be the channel length, it could be the oxide thickness. Every single model parameter has moved in

the same direction and therefore, this is called a global shifting process or manufacturing variations. Now, chips are now quite large that even within the chip I could have these variations ok, so what are the origin of this variations first of all ok?

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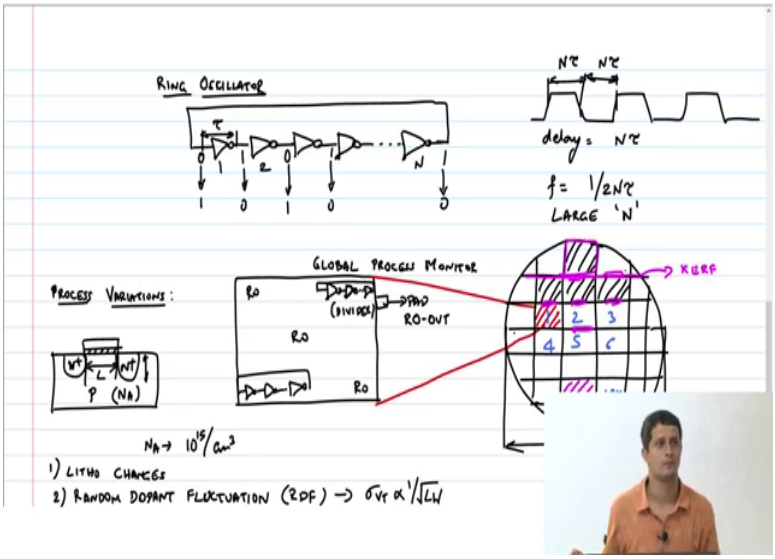

Process variations, so you take a transistor and this is my not gate N plus P oxide thickness and all that right. So, first of all we are now trying to manufacture physical dimensions of what order of magnitude 14 nanometer, 20 nanometer and so on. Unfortunately the wavelength of light that is used to do this process of lithography is 192 nanometer is much larger than the dimension that we are trying to manufacture.

So, how are these thing manufactured you basically make a mask and then shine light the shadows that is cast is suppose to you know hide some places and expose the other areas. But,

because the wavelength is 192 nanometer and you trying to do manufacturing of 14 nanometer, 20 nanometer and so on you will have diffraction ok.

So, what happens is, it is impossible to manufacture a million transistor right 8 billion transistors are there in my chip and across the wafer also. Impossible to manufacture all of these with exactly the same length. So, each transistor technically can come out with the slightly different channel length ok, this L itself can now change because of lithography problems.

Other thing is we derived the expression for the VT right, you remember it goes a square root of NA, where NA is basically the dopant concentration of the P substrate. Now, it goes the square root of NA, we made a big assumption there that every dopant atom has got ionized appropriately right. Under the channel we are assuming that every single dopant atom has got ionized properly. Now, let us see how many dopant atoms do you think will be there under the channel order of magnitude?

Student: (Refer Time: 14:14).

10, 1 million, 1000, 10000.

Student: (Refer Time: 14:22).

10 power.

Student: B.

Let us now what is NA by the way? NA is about 10 power 15 per centimeter cube, this is the typical dopant concentration. So, I am asking you how many dopant atoms are there under the channel or a magnitude? Like just say 10000, 1 lakh, million.

Student: Million.

Million, 10 power 6 right ok, go back and do this calculation assume that the channel length is may be 22 nanometer, width is about 44 nanometer right. And you can assume this that to be some even 1 micron, go back and do it you will find that the answer number of dopant atoms under a channel is about 100, 10 power 15 I know looks very large.

But, that is across 1 centimeter cube; if I take 1 centimeter cube of volume I have 10 power 15 dopant atoms, this is a very very small fraction under the channel. Now, think about this, if I have 100 dopant atoms and 10 of them are not ionized correctly which means there is a defect. They are not participating in terminating the electric field or whatever it is they cannot give me a free electron, what will happen to the VT? It has to go up because I have to put in more effort to get other dopant atoms to give me you know more free electrons I have to deplete the channel more and all that stuff right.

So, when you start making the channel smaller and smaller and smaller you also have this effect of random dopant fluctuation ok; so 1 is litho changes ok, 2 is called random RDF. Now, suppose I had a long channel device ok, why is this not a problem in a long channel device? Suppose I had like 10000 I mean long enough channel, so that I had about 1000 atoms dopant atoms under the channel right.

For 100 I said 10 were failure because typically root N will fail, so if it is 1000 what is the root N 30 right somewhere 30 40; now, in 1000 if 30 fails nothing really changes right. So, this random dopant fluctuation is a big problem only for these minimum size devices very very small devices if I have a large width also this effect will go away.

So, in fact, the standard deviation of VT give to random dopant fluctuation goes as 1 over root of L into W. Which means that if I have a larger area right like I told you it means I have 1000 atoms; in 1000 atoms if 30 fail not much will happen, which means that the standard deviation right. So, if I take 10000 devices and plot the histogram I will get the spread in the VT right.

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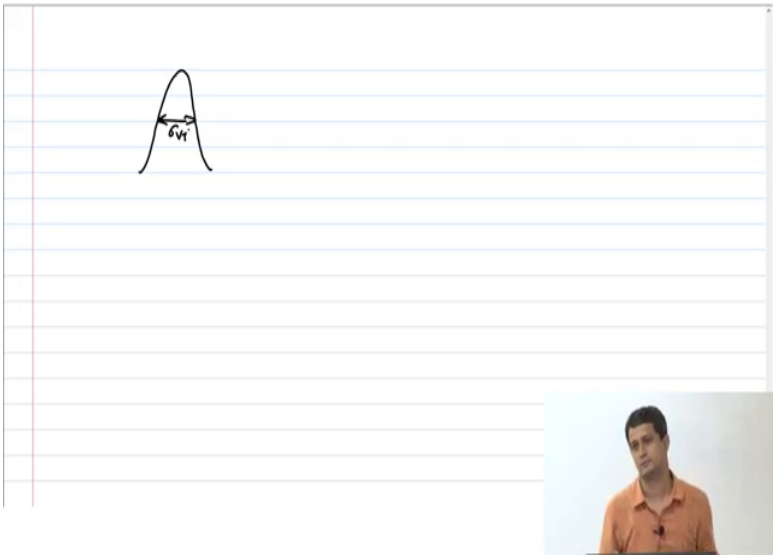

If I plot the histogram the VT will look like this right, in a Gaussian shape and somewhere here this is my sigma VT; sigma VT goes as 1 by a root of L into W. So, the variations come down if I have a larger device ok, so the source of variations are so many such factors ok. And therefore, I could have variations between two wafers I mean between two dies on a wafer right.

Here chip 1 and chip 2 can have different parameters; within the chip I could still have variations; which means that the ring oscillators sitting at this corner will be different from the ring oscillator sitting at this corner right. So, typically what people will do is they will put ring oscillators in multiple location on the chip if it is a big chip ok.

They will put one Ro here, one Ro here, and may be one Ro in the center also and all of these will be accessible through pads. So, the first thing you do is get the chip back measure these

parameters of the ring oscillator; if the frequency is not as what you thought it was it means there is a drift in the process parameters.

Then you can correct for this appropriately which means that if you know for example, that all transistors are become slower because VT went up then I can increase my V DD slightly these corrections can happen. So, ring oscillator is primarily used as a process monitor both for within die variations this is called a within die variation; within the die two different points can have different variations right. It is also used as a global process monitor, in the sense that every transistor on that die will basically have the same variation, but it can change from die to die.

Now, the other thing is this is from your designer's perspective, from the fab perspective I need to guarantee to the designer that my process is not shifting over time. Means, which mean that I have told you that the VT is going to be at this particular value, the current will be at this particular value and so on.

Now, with time if this just keeps drifting away that is not good, so the fab also has to monitor this right. So, how does the fab do it right, because remember real estate space is very very expensive. So, for example, the fab cannot say look I will use this one particular chip to figure out if you know my process is correct or not that is too expensive you are wasting very expensive real estate space.

Also by monitoring just one corner it is not going to help, I need to monitor it everywhere right. So, what the fab does is in this wafer here this is actually the place where the wafer will be deist means you are going to cut it right. You will cut it on these directions and send this chip back to the customer.

But before you cut it you have access to that space ok, this space is called the KERF all this is for your information by the way. It is not like you know not going to ask this somewhere in the exam, so that you just get a complete picture of what happens from the fab and the designer's perspective.

This KERF is where I will cut, so what the fab will do is in this KERF region they will put there ring oscillators here; multiple ring oscillators in all KERF regions. So, the fab what it does is? It manufactures the wafer, gets all the dies then they make measurements on all these KERF structures. If the process has shifted significantly it is a problem it is a red flag.

So, the moment they see that the process variation is more than the acceptable limit they will have to go back and debug and correcting manufacturing process, so that it does not continue right. So, you make measurements here, make sure everything is fine and then you cut it ring oscillator it does not matter after that, because once you made the measurement you can as well clear.

So, it is interesting that a simple circuit with just inverters actually has so many uses ok. So, it is lot of a brief overview of what process variations are and why you have to deal with it in the as a designer ok. Any questions here ok, so we will stop here I will see you tomorrow at 9.

Thank you.