Digital IC Design
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Lecture – 31
Stacking Effect and Sleep Transistors

So, good morning, let us continue with the discussion on the Stacking Effect.

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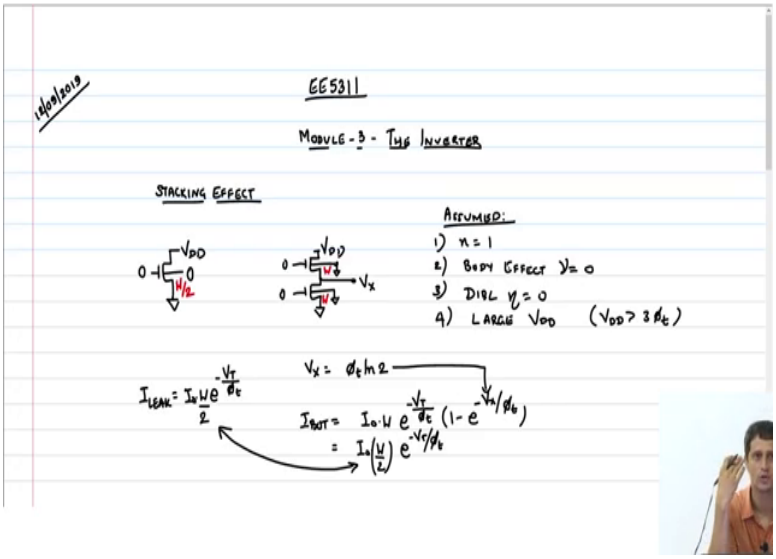

So, the idea was this. Suppose you had a single NMOS transistor with a gate grounded of course, the body is also grounded here, maybe I should write that explicitly and suppose you had two transistors in series like this, this is also V DD, both these gates are grounded, both bodies are also grounded now right and the assumption was ok, this is of width W each of these transistors has a width of W, W right.

So, now the question is how different is the leakage current through these two stacks, right. So, we made some assumptions if we assumed 1 ideality factor n equal to 1, right then body effect gamma equal to 0 then DIBL eta equal to 0 right, We made these assumptions and maybe some one more assumption, but we will come to that when needed, right.

And we found out that if you make these assumptions then this intermediate node V X, basically goes and settles at phi t lan 2 correct and therefore, if you look at the leakage current through this stack, I think I had the current through the bottom transistor right is I naught into W e power what, V GS is 0 right. So, it is minus V T by phi T into 1 minus e power minus V DS that is V X by phi t, right.

And if you substitute V X equal to lan 2 into this equation here, what do you get? You get this to be I naught into W by 2 into e power minus V T by phi t. This is what we got and if you look at the leakage current through this transistor I leak, it is basically I naught into W right e power minus V T by phi T right, assuming that V DD is much larger than phi T, you can neglect that term, right.

So, the assumption was also large V DD and typically if you have to quantify this large V DD is greater than 3 times phi T. that is when that 1 minus e power it will become 1 minus e power minus 3 and that is negligible is approximately 1, ok.

So, the first conclusion that we got from this was if you do not have any of these short channel effects then the 2 transistor stacks simply reduces to a single transistor with half the width, right. So, if you look at this if I now make this W by 2 right then this equation would become W by 2 and the 2 currents will be equal. So, putting 2 transistors in series is like adding 2 resistances; so, if a width w gives your resistance r then the net resistance in series will be 2 r which is equivalent to a width of W by 2, right. So, that is the basic idea here.

But so, therefore, this is really not the stacking effective since there is no big advantage here right, because I am just getting the effective width reducing because of this. So, if I have to make a comparison, I have to really make it with these 2 transistors width of W by 2 single

transistor stack, width of W 2 transistor stack right then I have to see if I get a current saving its only then that I actually can use the stacking effect very effectively. So, now, let us look at what happens when we introduce these short channel effects, ok.

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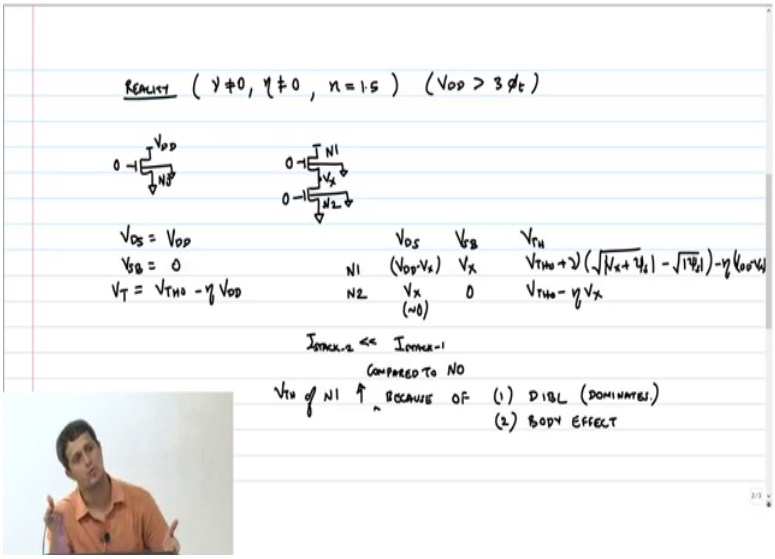

So, this is in reality, right. So, I have a single transistor V DD and ground 0. So, do you remember what I called n 1 and what I called n 2 in last class, can you tell me?

Student: Top is n 1.

Top is n 1, just to keep the notation consistent n 1 n 2, ok. This body is grounded, this body is grounded this thing, this ground, ok. So, now, let us just calculate various parameters and we will see what the effect of these short channel effects are, right which means basically gamma is not equal to 0, eta is not equal to 0 that ideality factor it does not matter too much, ok. So,

we can also put that in n is equal to 1.5 now, but V DD is still large, V DD is greater than 3 phi T that still holds, ok. So, the V DS of this transistor here right, let me call this n naught of n naught is what V DD, right V DD; now what is V SB? 0, right. So, therefore, what will happen to this V T V T of n naught; it will be V T naught, but there will be this DIBL effect right, there is going to it will basically V TH naught minus eta times V DD, ok.

Now we will write down the corresponding equations for these 2 transistors stack as well, ok; N 1, N 2, V DS sorry V DS V SB and a V TH, ok. What is V DS for so, this is by the way V X; so, for N 2 what is V DS V X right and V X is where phi T lan 2. You just saw it right somewhere very close to ground couple of milli volts actually right, it is not even if phi T is 26 milli volt lan 2 is less than 1. So, it is even less than 26 milli volts. So, it is nearly ground, ok.

Now, what about V DS V SB? 0. V TH for this bottom transistor? So, it will be V TH not minus eta times V X. Now, V DS for N 1?

Student: (Refer Time: 08:51).

V DD minus V x, right. V SB is what?

Student: (Refer Time: 09:02).

No, V X; now V TH therefore, should be V TH naught plus gamma times root of V X plus psi S, right minus root of mod psi S right and minus eta times.

Student: V DD (Refer Time: 09:33).

V x, Yeah. So, now, what is happening is the top transistor right so, this V X is going to go up little bit by the way ok, is it will not be exactly phi T on to it will be in reality it will go settle at some different value. You can actually calculate it correctly by substituting this

equation in there. You take V TH to be you know V TH naught plus gamma times root of that minus eta times V DS.

If you apply that equation and solve it you can find out exactly I will point you to a paper where the discussion has happened, you can read it for your own understanding, ok. We will just look at the intuition here now. So, now, what is happening is the top transistor is seeing a much lesser V TH than n naught. So, the transistor N 1 is seeing a much lesser V TH than N naught, and when I say much lesser remember because the leakage is exponentially dependent on V TH even that small DIBL effect can make a big difference to this leakage current right.

And; obviously, amongst N 2 and N 1 right, the guy who has who can permit lesser leakage is going to sort of determine the leakage eventually because it is a series path, right. So, therefore, in reality this I stack 2 right will be much lesser than I stack 1, primarily coming from DIBL right 1. Now, what about the body effect, if you take N 1 transistor, the V SB is; obviously, greater than 0 because V X is settling at some value between 0 and V DD. So, V SB is nonzero and therefore, V TH goes up also because of the body effect, right.

So, basically V TH of N 1, increases because of 1 DIBL; 2, increases compared to N naught V T H of N naught is minus eta times V DD, here it is minus eta V DD is there, but there is plus eta times V X. So, the V TH increases compared to N naught transistor and 2 because of body effect, right of course, this is the one that is going to dominate, ok.

So, any questions here you can refer that paper and go through that whole derivation right, it is a very interesting derivation that happens. The key point I want to convey here is you know if you just take a long channel device without all these short channel effects then you will not get that much of a saving. It comes because of all these short channel effects that is the key point that I want to convey here, and of course, leakage itself became a problem only because of short channel effects. So, you know you have to use it only it you do not have to use it in a long channel device, ok. Now, what how do I use this technique, ok.

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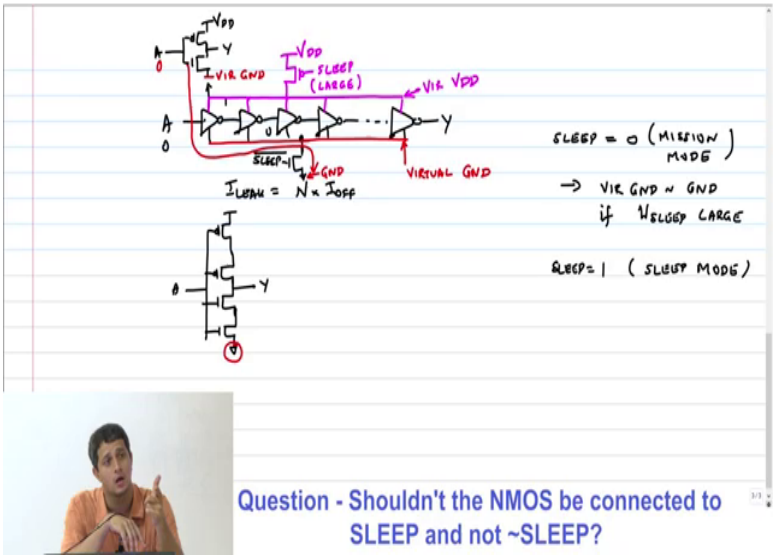

So, let us look at this this consider a simple inverter chain circuit because we have not done other gates till now, I will not go into that. Let us assume that this is my circuit, my input A output Y, ok. Now, if the input is 0 here this will be 1 0 and so on and then you are going to have a leakage current, right. So, let us assume both NMOS and PMOS leakage are equal, right. So, if there are any gates the leakage will be N N into I off either the NMOS or PMOS, it does not matter, let us assume both are the same right. N gates are now leaking in parallel and let us say this is very high, now how do I reduce the leakage, ok.

So, the thing is one thing to do is to take this inverter and convert it to a 2 stack inverter like this A Y. So, now, what happens even if it is 0 then I have a 2 stack NMOS transistor stack right and therefore, the leakage will be exponentially in itself per gate if it is 1 then the PMOS will be leaking and I will have a 2 stack PMOS this thing, right. Of course, the issue here is later we will see that the delay will go up significantly because now I have to discharge

through 2 transistors in series, effectively it is like r plus r the resistance is 2 r rather than discharging through just r, delay is going to go up significantly.

So, therefore, this cannot be done at every single gate level, ok. So, for that reason what is done is people adopt this technique of a sleep transistor, ok. Sleep transistor idea is like this I am going to pull out the ground nodes of all these inverters right that is basically this node, ok. Normally, I would connect it to ground I am now going to disconnect it from ground and what I will do is I will add 1 transistor like this, maybe I should draw in red.

So, that I can maintain the color consistency that ground node I have disconnected and put an NMOS transistor in series between that ground. So, this I am going to now call as virtual ground and this is my actual ground. So, between the virtual ground and the actual ground, I have added a NMOS transistor and I will control this by the signal called sleep or I will call it sleep bar. So, what will happen when sleep equals 0, yeah.

Student: (Refer Time: 16:41).

Yes, the NMOS transistor right and this transistor I am going to call it the sleep transistor. The sleep transistor will turn on and connect the virtual ground to ground, right only thing is it has to be really large. Because, now what is going to happen is all these inverters at least every alternate inverter because the signals get inverted every stage will discharge simultaneously into this, they can be a parallel current right all these currents and these I am talking about on currents, ok.

So, I have 2 modes of working, one is the sleep state other is the actual state, right in mission mode. In mission mode I want that this virtual ground to be as close to ground as possible; for that reason my sleep transistor has to be very large this is basically called mission mode, right. Virtual ground is nearly ground if W of sleep is very is very large let us say large, ok. Now, if sleep equal to 1, this is basically sleep mode right, what will happen when sleep equal to 1 the NMOS transistor is sleep transistor is off.

Now, what happens to the stack of every single inverter now, every single inverter on this right is now going to see 2 stack transistors from the output to the ground on the NMOS side only not on the PMOS side, right; you are following me. So, if I take this particular inverter, this guy is actually just our regular inverter PMOS, NMOS and then it is coming to the virtual ground A Y, this is my virtual ground.

So, if I take this path it is from Y let us assume that this a was 0 then the NMOS transistor supposed to leak, but the NMOS transistor is now seeing its source connected to virtual ground which means that there is a path that goes through this sleep transistor. And therefore, every single gate in that circuit will now see at least 2 transistors on its stack which means that the leakage is going to drop exponential, right; I can do the same thing on top as well because for the PMOS I need another stack, right. So, therefore, you take the power connection of these things, right call it the virtual V DD ground in the V DD connection and connect this to through (Refer Time: 20:31) PMOS transistor to V DD, this is virtual V DD.

This also will be connect sleep bar, is it sleep or sleep bar because when sleep is 0 I wanted to be in mission mode correct, it should be connected to sleep right this transistor also has to be large, ok. So, this stacking effect. So, the idea is very simple you make your logic circuit as you want, you do not worry about leakage at that point, right make everything then the you can put NAND gates, OR gates everything right, then you get a circuit where you are connected between V DD V DD and ground.

Finally, you just remove this V DD connection make it a virtual V DD ground make it a virtual ground and connect the sleep transistors in between the virtual grounds and actual ground, ok; our virtual V DD and actual V DD correct right then you are able to control this very effectively. So, this is a very powerful technique through control the leakage in the sleep state. So, when your mobile is not being used for example, then the operating system can actually figure this out and put it into the sleep mode.

Student: (Refer Time: 22:01).

Why?

Student: (Refer Time: 22:04).

Because no when sleep equal to 0, I want it to be in mission mode that means, the PMOS should turn on correct, when sleep equal to 1 it should be off, yeah.

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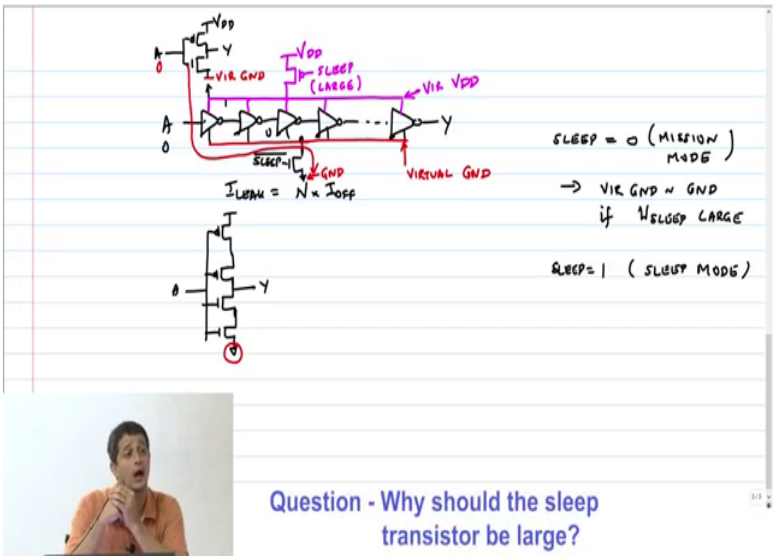

Student: Why should the sleep transistor be large?

Why?

Student: (Refer Time: 22:21).

Should be large, ok.

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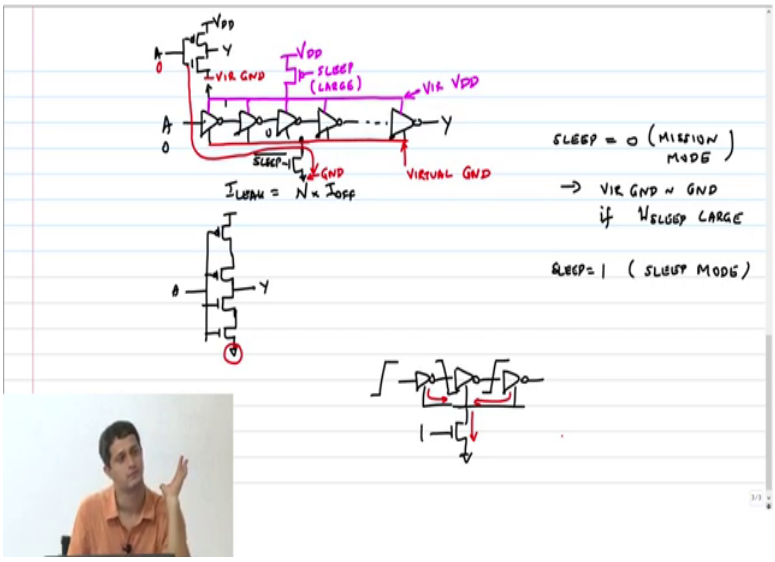

So, now let us look at what is going to happen in my mission mode, ok. I am going to connect all these things through, so in mission mode this is connected to 1, right. So, let us assume that the input made a transition; this will now make a transition like this then like this, right. So, what will happen is from every alternate inverter you are going to have a discharge current, right. And this is on current mind you, this is not off current right, in the transient phase this is an on current and all that current has to flow through this.

Now, if this transistor has a very small width then the only way this transistor can accommodate a very large current is to increase V DS, correct.

Student: Yeah.

If V DS increases by ground node is actually going to bounce. The ground virtual ground node which should be very close to the ground is actually going up, now that will ruin your circuit. So, the only way you can maintain that high current through this and also keep the virtual ground node very close to actual ground is to have a very large width, right.