Digital IC Design
Prof. Janakiraman Viraraghavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture – 30
Inverter: Leakage Power and Transistor Stacks

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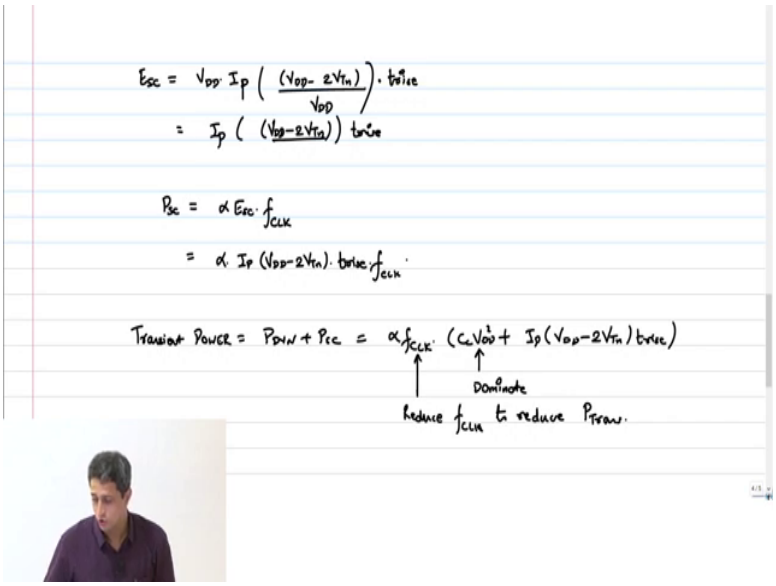

Now, the third component is very important in scale technologies because leakage current as we discussed many times is going to happen across all the billion transistors in the circuit. But, more importantly this is not a transient phenomena, it is a steady state phenomena. So, even if you slow down your clock and try to you know make your dynamic power lower right. For example, if you look at this right if you look at the transient power is equal to P dynamic plus short circuit. You will get this to be alpha into f clock into C L V DD square plus you know I P into V DD minus 2 V Tn into t rise right.

Now, if I want to reduce the total transient power one way is of course, I can reduce my V DD square V DD actually right. Therefore, V DD square will reduce dynamic power come down and of course, dynamic power is going to be the dominant component of this transient power compare to short circuit and dynamic power right. This will dominate, but beyond a point I cannot keep reducing my supply voltage you know there are certain limitations in scaling the supply voltage also.

So, therefore, the best way is to actually reduce your frequency of operation also if you want to make the power lesser right. You can reduce f clock to reduce P transient. This is the very effective way right. Unfortunately, you should you should be very careful of this because. The next component of power that we are going to talk about is going to happen only in the steady state. So, if you slow down your clock and give more steady state period to the clocks then you are going to leak more and more amount of leakage power at that time right.

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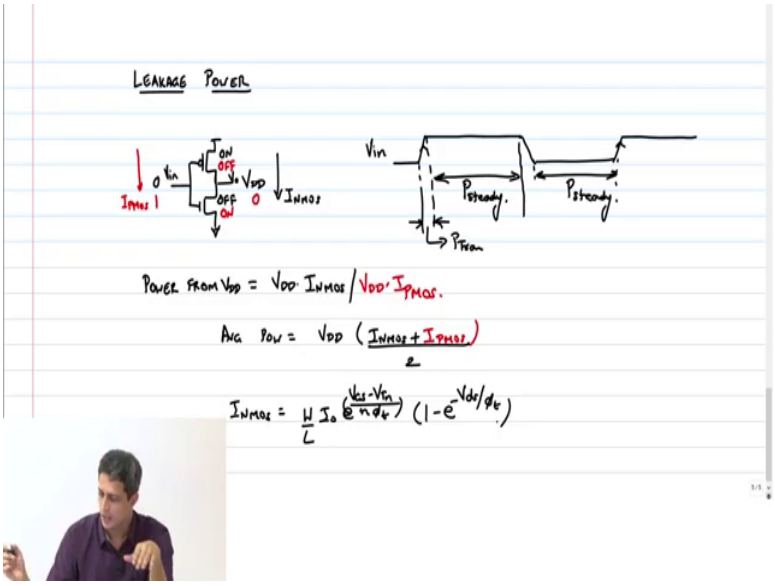

So, this is the. So, leakage power is like this. So, if my input is 0, output is V DD right in which case the NMOS is ON and PMOS is OFF. On the other hand, if my input is 1, output will be 0 right, the NMOS will be ON and PMOS will be OFF right. So, therefore, the ON guy is going to connect you to the supplies either V DD or ground. So, who is the guy who is going to leak current when the input is 0? It is the NMOS transistor that is going to leak current. So, you have I NMOS when the input is 0.

Similarly, when the input is 1 I have I PMOS that is going to leak right. So, if I look at my switching here let us say my input switch is like this V in V out right. Then, during this period I am going to have all the transient power. During this period here I am going to have steady state power right and also here and if you take a slightly slow clock effectively it is the entire clock period during which you are going to have this leakage current this is also P steady.

So, what is the power from V DD in steady state? It is V DD into it is just vi steady state current is I NMOS or I PMOS right this is I NMOS right or it is going to be V DD into I PMOS ok. I am matching the color in all of these diagrams ok. So, therefore, I can say may be I can say average power is V DD into I NMOS plus I I PMOS by 2 across the entire cycle right.

So, unlike dynamic power or short circuit power this just not depend on the clock frequency power, but if I ask you what is the leakage energy then I have to tell you for how long because it consume this much power and if I multiplied by the time then I will get the total leakage energy ok. So, one is dominated by energy the other is dominated by power right and you must keep this in mind always ok.

So, now, the question is what is this equation by the way I NMOS and PMOS right? It is going to be some W by L I naught e power V GS minus V Tn by n phi t into 1 minus e power minus V ds by phi t ok. So, question is find I do have leakage power right it exponentially depend on all these parameters and so on, how do I reduce this leakage power right because remember that this is the guy that is going to kill your battery. Your phone is doing nothing, but still there is power being drawn from the battery. So, when it is idle if I can do something to just reduce this power it is going to be very helpful ok.

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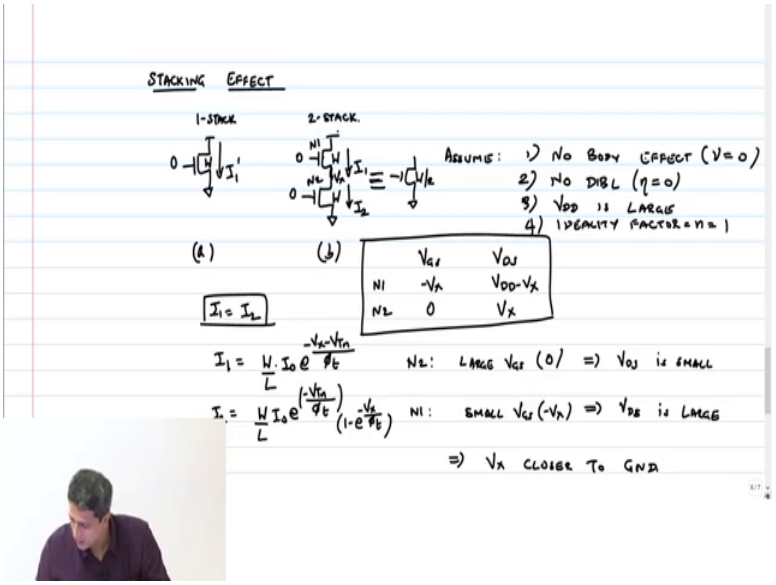

And, that is what is known as stacking effect ok. So, let me show you this sorry no sorry PMOS 0. Which amongst these two do you think will have lesser leakage current? So, this is slightly an incomplete question because I have to tell you, now what the wits are because I just showed you that in the previous expression it also depends larger the width it is going to leak more current right and going to go linearly.

So, therefore, let me say that this is W right this is W and this is also W. Now, amongst these two which ones do you think which one is going to leak lesser current? Yeah a b a or b, a will have higher leakage, why? V ds is ok.

So, good you are getting there. So, let us first of all try to evaluate what this leakage current is in the ideal case. I am going to consider now an ideal transistor slightly differently define from what I used define call an ideal transistor earlier ah. Ideal transistor earlier was no

leakage current. We had only the you know the (Refer Time: 09:55) model linear saturation, (Refer Time: 09:58) saturation and then I of 0. Now, I am saying this is another kind of ideal transistor where I have no short channel effects ok.

Let us assume 1, no body effect will come to all this later let us assume; that means, gamma is 0. 2, no DIBL – no drain induced barrier lowering; that means with V ds my V t does not change ok. So, eta is equal to 0 right. Now, we can evaluate what the leakage current through this stack is. Of course, this is a single stack 1 stack and this is the 2 stack. So, how do I evaluate the leakage current through that stack right.

What you do is you have to assume that this is going to be this transistor let me call it N1 N2. Current through N1 is I 1 current through N2 is I 2. What is the constraint I 1 it has to be equal to I 2 ok. So, what is the value of I 1? From the previous equation W by L into I naught what is V GS of the first transistor, yeah?

No ok. So, N1 N2 V GS V DS first tell me what is the V DS of let us assume the this intermediate node is V X. So, what is V DS of N2? V X. What is V GS of N2? What is V GS? 0, gate is grounded, source is also grounded. N 1 transistor what is V GS? minus V X V DS V DD minus V X ok. Now, first to simply our evaluation we have to make some you know get a feel for what this V X will be will it be close to ground or will it be close to V DD first of all? Close to?

Why? No, no leakage current will be less is not something that it will fix V X so that the currents match that is all whatever current you get you get. So, since I 1 has to be equal to I 2 right the V GS and V DS have to adjust itself for both transistor so that the two currents are the same correct. So, if you look at N2, V GS is 0. Compare it with N1 V X is some value between 0 and V DD, I do not know what it is. We need to figure that out.

If V X is even 100 millivolt right V GS for N1 is minus 100 millivolt it is actually lesser; that means, because of V GS N1 can permit much lesser leakage current already, correct? N2 can permit much higher leakage current because V GS is 0. So, now, tell me will V X be close to

ground or V X be close to V DD? So, N2 has large V GS compared to N1 compared to N1 N2 has large V GS, N1 has small V GS right this is minus V X 0.

Now, if both currents have to be the same the V GS has to be compensated by the V DS only then you can have these two currents to be the same, correct? You agree with me? So, if N2 has a large V GS, then V DS has to be small how will N 2s V DS be small V X is close to 0 right. So, implies V DS is small therefore, right now. Here N1 since V GS is small implies V DS is large. So, if V X is somewhere close to ground compare to V DD that is right, then these two will easily match. So, conclusion V X is closer to ground and assume third assumption V DD is large ok.

So, now, let us write down these current equations I 1 is going to be or let us write I 2 first because it is easier. I 2 is W by L I naught e power, what is V GS? I 2 look at this table 0 right. So, it is minus V Tn by phi t I am going to make one more assumption ideality factor n is 1 let us assume that you are able to manufacture the device. So, well so that the sub threshold slope is really minimum and all that all that no issue right into 1 minus what V X by phi t, correct?

What is I 1 e power V GS is minus V X minus V Tn this is where assuming that the body effect coefficient is 0 helps because for N1 the source is not at 0 it is body here will be at 0. Therefore, there is going to be a body effect that will come in there, but for initial just to give you the intuition I am now assuming body effect is also absent right. So, therefore, both V t's will be the same V X minus V Tn by phi t into 1 minus e power minus V DD minus V X by phi t, but V X is close to ground. So, therefore, I can just make that 1 minus e power minus V DD by phi t.

Now, V DD is large enough which means it should be greater than 3 times phi t. What is phi t? 26 millivolter room temperature. So, if you are over 100 millivolt which V DD for sure is right you can neglect that 1 minus e power minus V DS by phi t right. So, I am going to just say this ok. So, now, I wanted to equate these two currents and find out what that intermediate node voltage V X is phi t now.

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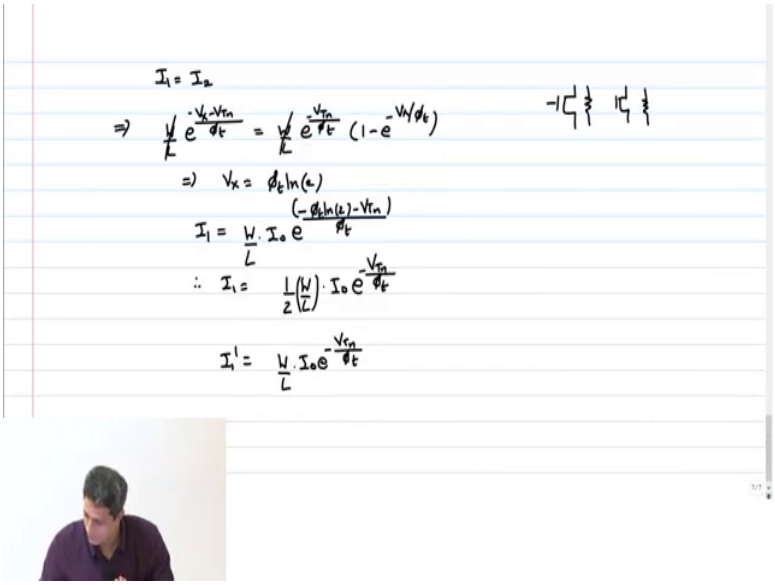

So, cancel everything implies V X is phi t ln 2. Now, tell me what will happen to the leakage current I 1 or I 2 if I substitute this value in, what is I 1? Yeah, 1 by 2 W by L into I naught e power minus V Tn by phi t ok.

Now, let us go back and you tell me what is the leakage current through this guy? Let me call this I 1 prime. What is I 1 prime? What is I 1 prime? What is V GS for this transistor? 0. What is V DS? V DD. So, I can clearly write I 1 prime as W by L into I naught e power minus V Tn by phi t, correct? What this is telling us is putting two transistors in series is simply giving me the effect of halving the width, correct? V X has gone and adjusted itself at phi t ln 2, so that the leakage current through the 2-stack NMOS transistor is half that of the single NMOS transistor with the same width W, ok. So, this actually is not stacking effect.

If I put two transistor in series right, for example if I put two transistors in parallel right and I do something this is like one resistants, this is like another resistants parallel resistant is R by 2. Similarly, series resistant is 2R which mean it is like halving the width in general right, this is not the actual stacking effect. So, what I wanted to show you here is if I do not consider all the short channel effects leakage current is not going to come down drastically because what it saying is now instead of this guy. I will simply use a transistor like this because even when you consider delay and other things that is exactly what it is. It is going to result in a transistor width W by 2.

This is equivalent completely with respect to delay and everything. So, why will I even go and add the extra transistor make it more area more this thing and then get the same leakage current, it is not beneficial. What happens is because of short channel effects, for example, now consider DIBL the bottom transistor V X is very close to 0 right. So, we the DIBL effect is extremely less there. The top transistor V DD minus V X is going to be very high right and it is going to be close to V DD right. So, what will happen to the threshold voltage of that transistor there?

Yeah, it will reduce, correct. So, these two fighting will actually cause a significant reduction than just having that V DD. So, what happens is because my top if I consider let me write that all I think I cannot just talk through it.

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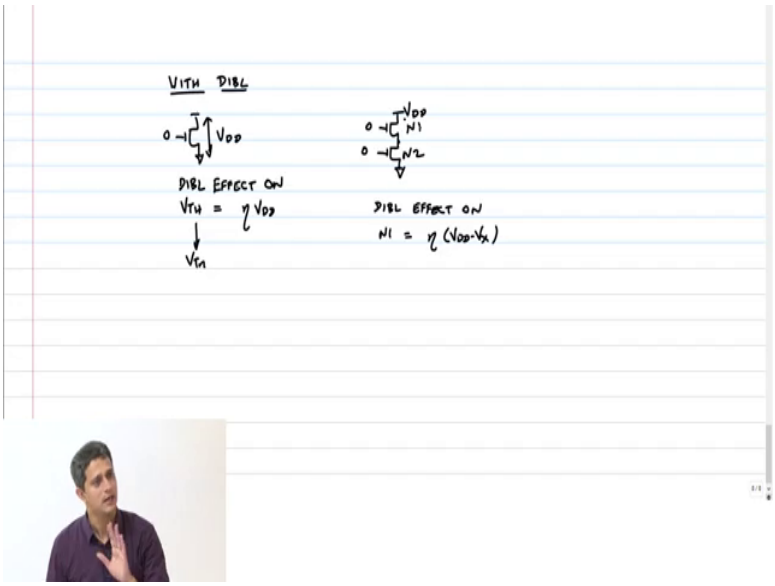

Now with DIBL single NMOS transistor is like this right V DS is just V DD right. So, the DIBL effect on V TH is equal to eta times V DD now here when I consider two transistors stack 0 0 right V DD the DIBL effect on the top transistor right is V DD minus V X on N1; N 1 is equal to eta into V DD minus V X right. Since that is lesser if you consider the V Tn of this transistor here it will be lesser by eta times V DD whereas these two transistors now they will not have the same V Tn of course, because of DIBL right.

The two transistor N1 and N2 will have a different V TH, but it will also be higher than the V T of this single NMOS transistor ok. So, what I will do is since we have run out of time please think about this and come back. Just stacking two transistors does not give you the needed impact right that is not why people have use this technique. So, effectively that is what I wanted to show you through the derivation.

Ideal case it just reduces to a half the width transistors leakage which is useless. I might as well use the transistors single transistor with W by 2 and get the same effect right it is because of short channel effects that you get much more of a benefit in through the stacking effect. So, I would even urge you to do a simulation now right, you can go with your simulator lt spice put a single transistor, put a double transistor see how much of reduction you getting in current. Of course, put the appropriate W's and see. You just see you will find that it is much more than just W by 2 I will explain that in the next class.