

**Digital IC Design**  
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**Lecture – 29**  
**Inverter: Short Circuit Power**

So, let us continue with our discussion on Power, right. So, that is what we were discussing last class.

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EE5311

MODULE-3 - THE INVERTER

POWER:

- 1) Dynamic power
- 2) Short circuit power
- 3) Leakage power

1) Dynamic Power:

$I_{Rapp} \quad \frac{1}{2} C_L V_{DD}^2$

$I_{Rdyn}$

$C_L$

So, we said there are 3 components of the power; 1 is dynamic power, 2 is short circuit power right and 3 is leakage power, ok. So, the idea here at least for the first two is the following if I have an inverter like this right and the input prices it is some finite rise time and then falls

with some finite fall time, then the output would basically go like this, leaving all the you know second order bumps.

That I spoke about earlier it would look like this and in the process you would have a capacitor that is being charged and discharged right each time the output rises and falls, ok. So, we said that when the for dynamic power for dynamic power we said that when the capacitor has to charge there is an  $r$  equivalent of  $p$  which is going to charge like this right and of course, the NMOS is cut off.

Again, the assumption here is the though I showed in reality that the input has a finite rise time and fall time. Here we are assuming that the input rises instantaneously or falls instantaneously which means that the PMOS is a perfect resistor and the NMOS just cuts off right and therefore, the charging is going to happen where all the current from the supply will be used to charge the capacitor to  $V_{DD}$ , right.

And similarly, when we are talking of the discharging case, the PMOS will be cut off and the capacitor will get discharged through the NMOS transistor like this, right. So, each time the capacitor charge to  $V_{DD}$  and energy of  $\frac{1}{2} C_L V_{DD}^2$  gets stored in this capacitor. Of course, the power supply has supplied  $C_L V_{DD}^2$  that is the amount of energy that this power supply gave where it the remaining energy go, it got dissipated in the resistances heat in the through the PMOS transistor, ok.

So, irrespective of what the resistance is or what the width of the PMOS transistor is the same amount of energy is dissipated in that PMOS transistor always, right. And of course, when the capacitor gets discharged right when the output sort of false then the same  $\frac{1}{2} C_L V_{DD}^2$  square gets dissipated through the NMOS transistor and all the current flows into the ground, right.

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MODULE-3 - THE INVERTER

POWER:


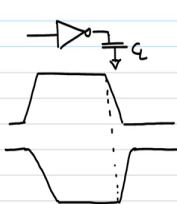
- 1) Dynamic power
- 2) Short circuit power
- 3) Leakage power

1) Dynamic Power:

$\frac{1}{2} C_L V_{DD}^2$

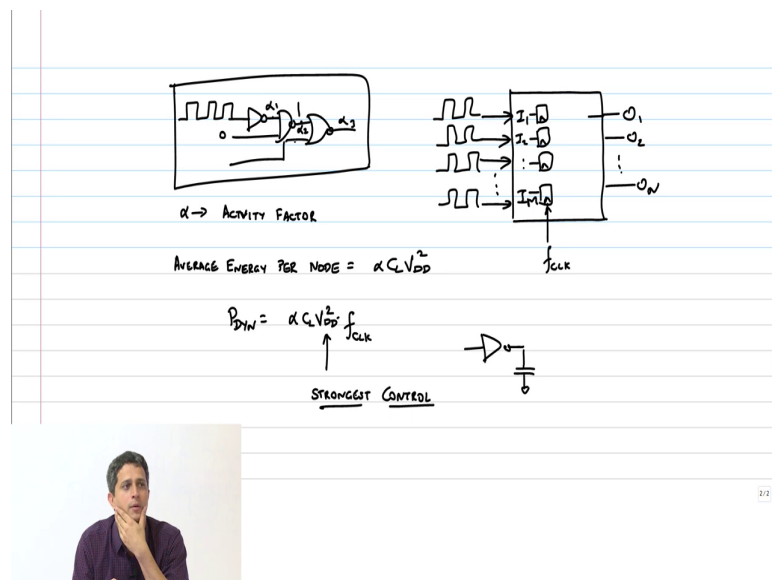
$\frac{1}{2} C_L V_{DD}^2$

FOR EVERY CHARGE/DISCHARGE CYCLE Energy =  $C_L V_{DD}^2$  (J)



So, overall for every charge discharge cycle right energy equals what?  $C_L$  into  $V_{DD}$  square right of course, this is going to be in Joules because this is energy, right. Now, what we are talking about is dynamic power when we say dynamic power it is only the power that is dissipated because of charging, and discharging that load capacitor including its own capacitance actually right that total capacitor that is the power that we are referring to in dynamic power, ok.

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So, now the point is if I have an arbitrary circuit like this right and let us say that this input is 0, and then this input is switching constantly what will happen to this input, it will be?

Student: 1.

1 right, NAND gate output will be 1 if the input is 0. So, if the other input is not switching the output can just remain there forever. So, what is the dynamic power that is dissipated by this NAND gate it is basically 0 in steady state, right. So, it is not sufficient if we just say that every cycle that gate is going to charge or discharge that capacitor that is not true, it depends on the inputs, it depends on the input combinations, input transition combinations and everything right, there are so many things that it depends on.

And therefore, we define something known as an activity factor, how often does this node switch for a given circuit, ok. So, for example, if I have a circuit with  $n$  inputs  $I_1, I_2, I_m$  and outputs  $O_1, O_2$  and  $O_n$  right. Now, the inputs could actually be switching every time it does not matter right, this could be ideal clocks it does not matter to me right or it could be some other arbitrary signals, ok.

Now, the question is I need to find out how often every node inside this circuit is going to switch. So, how do you do that you just have to run a probabilistic simulation; feed random input combinations and allow random transitions to happen and just count the number of times that this node has actually switched, that gives you the probability of that node switching. So, question is why cannot I do it for all possible combinations of the inputs if I have  $m$  inputs. How many input combinations do I have?

Student:  $2^m$ .

$2^m$  now how many transition combinations do I have that is much worse right. So, therefore, you cannot exhaust all these things, but it is sufficient if you just take for example, maybe a million transitions you just allow a million input patterns to be applied to this circuit. And you just count what is the probability of each of those nodes switching now that becomes the activity factor of that particular node right and therefore, the energy right average per node will become  $\alpha C_L V_{DD}^2$  depending on how often that is going to switch, right.

Now, if you have something like a clock the activity factor for a clock is 1, it is switching every single cycle, right. So, that is the highest possible active activity factor that you can have for every other node it will be somewhere between 0 and 1 right mostly it will be actually quite low, right.

So, now how do we convert this to power? So, what will happen is typically these inputs here if you look at this circuit will get buffered through flip flops ok, there are flip flops here. So, what will happen is the input actually can change only every rising edge of the clock even

if you apply it at a faster rate changing somewhere right, it will not reflect in the change inside the circuit.

So, you can assume that all the inputs are synchronous and there is a central clock which is controlling the entire circuit, right and if that clock is running at a frequency of  $f_{\text{clock}}$ , right. Let us assume that this clock is running at  $f_{\text{clock}}$  then what is the dynamic power it is the rate of change of energy, right. You have  $\alpha C_L V_{DD}^2$  which is the average energy depending on switching factor and all that and this is going to happen at a rate of  $f_{\text{clock}}$ , right.

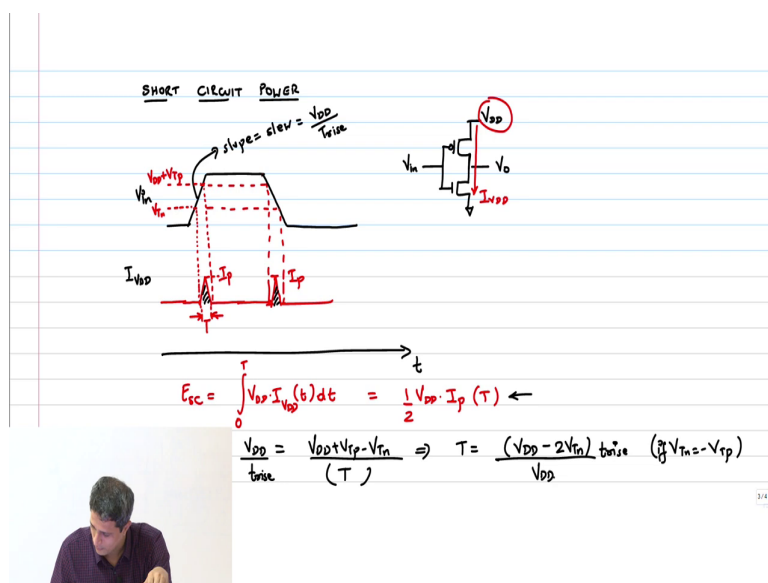
Therefore,  $\alpha C_L V_{DD}^2$  into  $f_{\text{clock}}$  is the dynamic power for a logic gate in general, ok. So, if I ask you what is the dynamic power of this inverter well it does not it not the question is not complete, you have to tell me where I place this inverter in which circuit and how right then you have to tell me what its load capacitance is right. You give me all this information then I can say that yes for that particular node which has a capacitance  $C_L$  it is going to have a dynamic power of  $\alpha C_L V_{DD}^2$  into  $f$ , right.

Clearly  $V_{DD}$  dependence being quadratic is the strongest way in which you can control dynamic power if you drop  $V_{DD}$  by half your dynamic power will drop by one fourth right So, this is the strongest control of dynamic power, ok. So, what do you have to do is if I am given a particular circuit like this here and I want to calculate a total dynamic power.

I need to estimate first what is the switching factor of this node, what is the switching factor of this node, what is the switching factor of this node then I have to estimate what the total capacitance is on each of these nodes right, then for each of them we are its going to happen at  $\alpha C_L V_{DD}^2$  in to  $f$  ok, any questions here.

So, during steady state there is no the dynamic power is not even defined because the capacitor is just holding charge and it is being driven to either  $V_{DD}$  or ground no problem ok, any questions on dynamic power ok.

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So, let us now move to short circuit power. So, we made an assumption in dynamic power that the input is going to change instantaneously right; that means, the PMOS becomes a resistance, the NMOS becomes a cut-off switch or vice versa, NMOS is the resistance PMOS is a switch that is cut off completely in that model. There is no current between supply and ground at any point in time be it in steady state or in during the transition, right.

Of course, in reality that is not true and therefore, we need to consider that also into our calculation here,  $V_{in}$   $V_{out}$ . So, my input as I told you is going to go like this,  $V_{in}$ . So, let us now plot the current  $I_{VDD}$  ok, there is going to be a current that is going to flow from  $V_{DD}$  to ground like this; obviously, in steady state it is going to be 0, right at what point will the  $I_{VDD}$  become non 0 first?.

Student: V input.

When V input crosses  $V_{Tn}$ ; obviously, it is going to turn on the NMOS transistor, PMOS is obviously, turned on already therefore, you will start having  $I_{VDD}$  after V in crosses  $V_{Tn}$ . Now, at what point will it turn off will it come back to 0 again or  $V_{DD} \text{ minus } V_{Tp}$  or you say  $V_{DD} \text{ plus } V_{Tp}$ . So, here; so, this by the way this for this graph this is time, ok.

So, therefore, here this is my these are the two points  $V_{Tn}$   $V_{DD} \text{ plus } V_{Tp}$ , right. So, now, in between your current is going to go up and then come down right as the input crosses  $V_{Tn}$  and starts turning on the NMOS transistor, NMOS starts in saturation PMOS in linear slowly. The PMOS will also come to saturation mode at which point the current will be maximum, what is that point called? Trip point  $V_{in} = V_{out} = V_m$ , right.

After that again the PMOS starts going into saturation and NMOS will come into linear therefore, reducing the current and then back into cutoff. So, in this region you can approximate the current as a triangular region like this right and this we are going to call it as that let me call it  $I_{naught}$  right or no let me call it  $I_{peak}$ ,  $I_p$  ok. This is that current that we evaluated at  $V_{in} = V_{out} = V_m$ .

Now, similarly in the falling edge you are going to have exactly the same kind of thing somewhere out here it will happen, out here it will happen and the current will, maybe I should remove all these too many too many lines. So, this is again my  $V_{DD} \text{ plus } V_{Tp}$ . So, this again will go up like this come down to 0 and then you will be done, ok. So, now, we just need to calculate the short circuit energy, right. So, what is the short circuit energy  $E_{SC}$   $\int V I dt$ , right.

So, let us assume that this is going to happen for a particular time T, right. So, it will simply be 0 to T what is V; where is the current coming from,  $V_{DD}$ . So, what is the V in this equation  $\int V I dt$ , the current is coming from this supply I am looking at the power delivered by the supply. So, what is the V in that equation?  $V_{DD}$  it is a constant into I short circuit of T right or I called it  $I_{VDD}$  into  $dt$ , right.




So, basically it is just multiplying by  $V_{DD}$  and finding the area under this triangle, right. So, that is nothing, but half  $V_{DD}$  into  $I_{peak}$  right into half base into height right into  $T$ . Now, you can if I give you the slope at which the input is rising then you can calculate what this  $T$  is how long it takes to go from  $V_{vTn}$  to  $V_{DD}$  plus  $V_{Tp}$  right given the slope is say  $V_{DD}$  by  $T_{rise}$ . Let us assume that this slope or it is also called slew is  $V_{DD}$  by  $T_{rise}$  and this slope is  $V_{DD}$  by  $T_{fall}$ .

So, let us assume  $T_{rise}$  is equal to  $T_{fall}$ . So, can you tell me what the answer is for the short circuit power I mean energy. Let us make an assumption that  $V_{Tp}$  is minus  $V_{Tn}$ , right. So, you can write this as minus 2  $V_{Tn}$  by what  $V_{DD}$  into  $T_{rise}$  right assume that  $V_{Tn}$  equals minus  $V_{Tp}$ , if. Of course, this expression here is only for the rise for a rise and fall it is going to be twice that, right.

So, I can just say  $V_{DD}$  into  $I_p$  into  $T$ ,  $I_p$  into  $T$  and then you substitute this expression you will get the expression for the short circuit energy, clear right. So, remember that this is going to happen for a very very short period of course, it does not happen in steady state, but in the transition period even this thing is going to happen for a very short period, ok.

So, maybe if your slew is very very bad then the amount of time at which the current can flow is going to be large right, but usually in high speed circuits you will ensure that the slew is also very good and therefore, it is a extremely short period, clear.

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$$\begin{aligned}
 E_{sc} &= V_{DD} \cdot I_p \left( \frac{(V_{DD} - 2V_{tn})}{V_{DD}} \right) \cdot t_{rise} \\
 &= I_p (V_{DD} - 2V_{tn}) \cdot t_{rise} \\
 P_{sc} &= \alpha E_{sc} f_{clk} \\
 &= \alpha I_p (V_{DD} - 2V_{tn}) \cdot t_{rise} f_{clk}
 \end{aligned}$$


So, therefore, you can write  $E_{SC}$  as can someone tell me the expression?  $V_{DD}$  into  $I_p$  into  $V_{DD}$  twice  $V_{DD}$  minus  $2 V_{Tn}$  into  $T_{rise}$ , correct. No, I thought we removed the half because this is for rise and fall, see this was basically the half b h of here right in this region, what about this region. So, when it rises and falls the charge discharge cycle is what I am asking for.

Student: (Refer Time: 23:52).

See  $T$  is because what I am saying is its going from 0 to  $I_p$  in a time of  $T$ , right. So, you are right; you are right sorry you are right, this is not  $T$  by 2 correct. So, it is the input is taking a time  $T$  to go up you are right sorry, that is a mistake. So, this will vanish ok, is that fine?

Student:  $V_{DD}$ .

$V_{DD}$  will get canceled  $V_I$  into  $T$  correct power into time is energy, ok. Now, again just like dynamic power this is a transient phenomenon only when the input is making a change will this happen. And therefore, the same things that we discussed there will apply here also, you need the activity factor only when that switches is going to happen and so on; therefore, the short circuit power is going to be  $\alpha E_{SC}$  into  $f_{clock}$ , ok. So,  $\alpha$  into  $I_p$  into  $T$  rise into  $f_{clock}$ .

Student: (Refer Time: 25:34).

Why?

Student: (Refer Time: 25:39).

No, but actually pointed out, see the I am giving you that the input rise slope is  $V_{DD}$  by  $T$  rise, correct. So, it takes the input takes from 0 to  $T$  to go from  $V_T$  end to  $V_{DD}$  plus  $V_T$ . So, you have to look at this guy, this is  $T$  if you look at this triangle this is  $T$ , and that is the slew that is what I am defining as the slew clear. So, therefore, that is, ok.