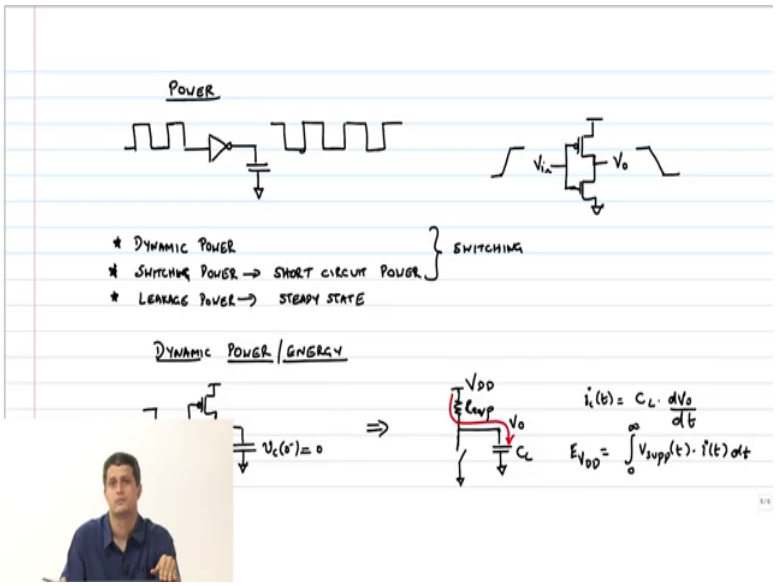
Digital IC Design
Prof. Janakiraman Viraraghavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture – 28
Inverter: Dynamic Power

(Refer Slide Time: 00:15)



So, now let us move on to Power. And this will be the only discussion I will have on power in this course, ok. This will be a very short discussion maybe 2 classes or so; but nothing more, we would not have time for anything more in this course, ok. So, what do I have an inverter as usual and my input let us say is switching like this. What will happen?

The output also is going to switch in the opposite polarity, right. So, each time the input goes high, what will happen to the capacitor; when the input goes high, capacitor discharges and each time the input falls, the capacitor charges. So, there is this continuous charging and

discharging process that is happening in a digital circuit, right. And obviously, this is going to constitute to some constitute some power, ok.

So, we need to now quantify how much of this power is or how much this energy is, ok. So, it turns out that there are 3 kinds of power or energy that will be involved in CMOS circuits; one is dynamic power. Dynamic power is just what I told you; input is switching, output is switching which means the capacitor is continuously charging or discharging, right and this is leading to some power loss, ok. So, it is purely this capacitor charging, discharging power that we are talking about when we is talk about dynamic power.

Second is switching power, right or I do not know what that, forget what the other term is or it is called short circuit power. So, here V in, V out my input is rising like this; my output will therefore fall like this. At some point of this transition between 0 and V DD for both input and output; my NMOS and PMOS will start conducting, right.

So, clearly as soon as my input crosses V T N; it is going to both transistors will start conducting some current, that will peak when both of them go into saturation and after V DD plus V T P both of them will shut off again, right. This is a short circuit power, because essentially now there is a sort of a short circuit between the power and ground; which otherwise is not there by the way, there is no current in steady state, it is only in this transition that you have some current like this.

So, for every switching that happens, I do have some short circuit power that is burnt in the process, right; we will quantify this number also. The third one is the steady state power which ideally was supposed to be 0; because there was no leakage, but of course, we do now, have a reasonable amount of leakage. And therefore, we have leakage power as well, both of these happen only during switching; but this happens in steady state, ok.

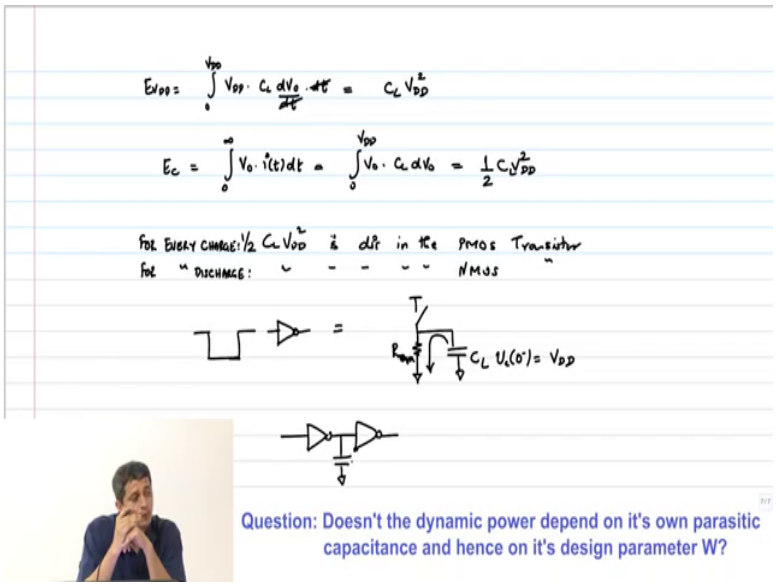
So, let us start with dynamic power, ok. So, we will start with actually energy first. My, let us assume my capacitor is now being charged; initially it was discharged to ground. Now I am

going to get my input to go low, instantaneously assume; again now we will go back to this instantaneous assumption.

Input is falling instantaneously, right; which means, now there is no question of short circuit power and all that. Because I just shut off the other guy, other transistor instantaneously; only the PMOS has some equivalent resistance right, this equivalent circuit is like this R equivalent P C L going to V DD and of course, my NMOS has been cut off. So, all the current coming from the supply is going entirely into the capacitor for charging, right.

So, what is the capacitor current? So, let us assume by the way that this node voltage is V naught. So, what is the capacitor current? C L into d V naught by d t, ok; now, of course, the same current is being drawn from the power supply also, correct. So, how much of power, how much of energy is actually delivered by the power supply first of all? V into I integrated over time, right. So, the energy from supply E V DD is integral V supply of t into I of t d t from 0 to infinity actually; how much of our time it takes. What is V supply of t? It is just V DD; it is a fixed number, right.

(Refer Slide Time: 07:48)



So, E V DD is V DD into; what is the current C L d V naught by d t into d t. So, I will just switch the variable of integration V naught is going from 0 to V DD; therefore, the net energy that is delivered by the power supply in this charging process is C L into V DD square.

Is this energy completely lost? So, half we will come to, but clearly some of the energy is actually stored in the capacitor; because now the capacitor is charged to V DD, right. So, what about the energy in the capacitor, right? Again we can do the same thing; V naught into i of t into d t, right. So, this is basically 0 to V DD V naught into C L d v naught, right.

This is half C L V DD square; of course, half C V DD squared is the energy stored in the capacitor, right nothing surprising about this. So, the remaining half C V DD squared where it

did go? It dissipated in the PMOS resistance as heat and it is lost, right. So, for every switching, for every charging half C L V DD squared is dissipated in the PMOS transistor.

Now what happens in the discharging cycle? Now the input has fallen, instantaneously it again rises, right. So, that time, the model is my input has basically fallen like this and then is rising instantaneously again, right in my inverter, right. So, the equivalent model is PMOS has been cut off; there is an NMOS R equivalent of n C L and this V c of 0 minus now is V DD.

Clearly you are going to discharge this capacitor through this to ground and that entire half C V DD squared that was stored in the capacitor after the charging cycle is now lost in the NMOS resistance, right. So, for every discharge half series is dissipated in the NMOS transistor.

The important thing to note is neither this energy for discharging or charging depends on the resistance, it is not a function of R equivalent n or R equivalent of P; therefore, it does not depend on any of the design parameters of that transistor. Of course, if I now connect one inverter to the next inverter; then the capacitance on this node will depend on the input capacitance of the next gate. So, there yes it does depend on the width of the next transistor; but not on the width of it iself, ok.

So, this is totally independent of any design parameter of the transistor here, of the inverter here yes. So, you are saying that it is own parasitic capacitances ; question is do we isolate that somewhere ok, you are right in the sense that it does depend on it is design parameter W P and W N through the capacitance, but not to the resistance, I stand corrected, correct ok.

So, with that we will stop today's class. In the next class we will continue with the discussion on power; we will cover the short circuit power and leakage power and wind up this module in the next class, ok.