Digital IC Design
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Lecture - 26
Elmore Delay Model

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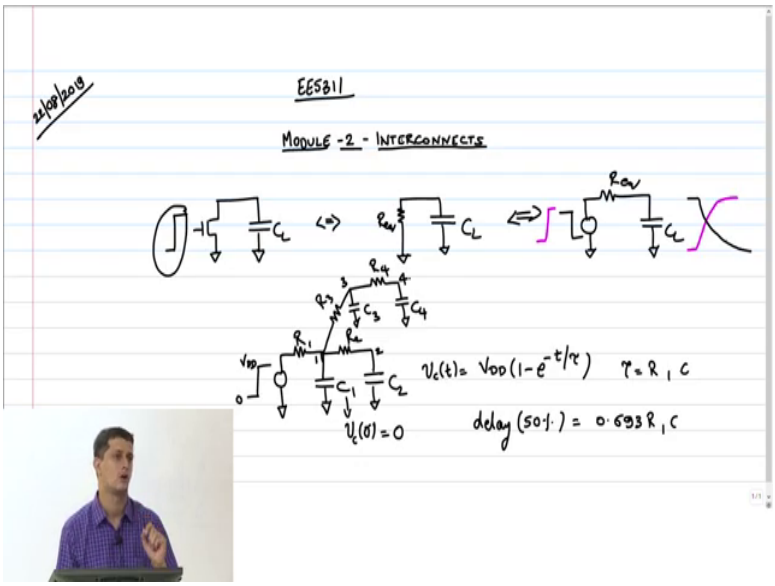

So, with that let me just get started, right. So, in the last module let me just sort of recollect the last discussion we had. We had a transistor that is discharging a capacitor right and, we said that the gate is going to go instantaneously to V DD and turn on my NMOS transistor and therefore, I can treat this as a resistance R equivalent into C L, right. Of course, now when I do this where is the source yeah, no of course, that is this thing, but where is the switch that is actually turning it on.

Student: (Refer Time: 01:18).

Correct. So, in this RC model where should I put my source?

Student: (Refer Time: 01:36).

So, you agree that when I moved from the transistor model to the R equivalent model I captured the resistance, but what I am not captured is really this effect where is that source, where do I put it. So, it turns out that this has to be placed like this C L are equivalent and I have a source like this and this source is falling instantaneously, it is like a switch the moment you turn that switch on, it gets shorted to ground and the capacitor starts discharging, ok.

Of course this we know very well right the alternate is I can also instead of making the supply fall, I could say I want to charge this right, though it will not happen through an NMOS transistor that will happen through PMOS we will come to that later. But, I could have this equivalent RC model and I say that the source is going to charge in which case my C L will also charge like this, right. In the earlier case remember that cl would start at V DD and then discharge exponentially, ok.

So, in summary if I have an R and the C, and I have a unit step function as the source voltage assuming that this capacitor is discharged at t equal to 0 v c of 0 minus equal to 0. Then, what is the equation for the capacitor voltage with time; let us say this goes from 0 to V DD. What is it, V DD into 1 minus e power minus t by tau where tau is equal to R equivalent into C and then we said that the delay to actually charge the gate delay right was fifty percent.

So, you do point six nine 3 RC and all that right. So, delay right which is defined as the 50 percent is 0.693 R equivalent in to C, right and let me call this R equivalent. So, now, the interesting point and it turns out that we will see more and more of this model coming into our you know logic gates and other things what happens if I have another leg like this.

So, this is R 2 C 2, this is R 1 C 1 I will call this R 1 C 1. What will happen if my capacitor is loaded with another RC, ok, The problem becomes even more interesting if I have another ring like this where I have R 3 and then C 3, then I can put 1 more C 4 R 4.

Now, I could ask you what is the delay right from the input to the any of the destination nodes right my destination code node could be node 1, node 2, node 3, node 4, any of the 4 nodes. If I ask you what is the delay at node 4 given that the input went instantaneous from 0 to V DD what is the delay for the node 4 to go to V DD by 2 for example or node 3 node 2. So, this is the problem that the Elmore delay model solves ok; so, ok.

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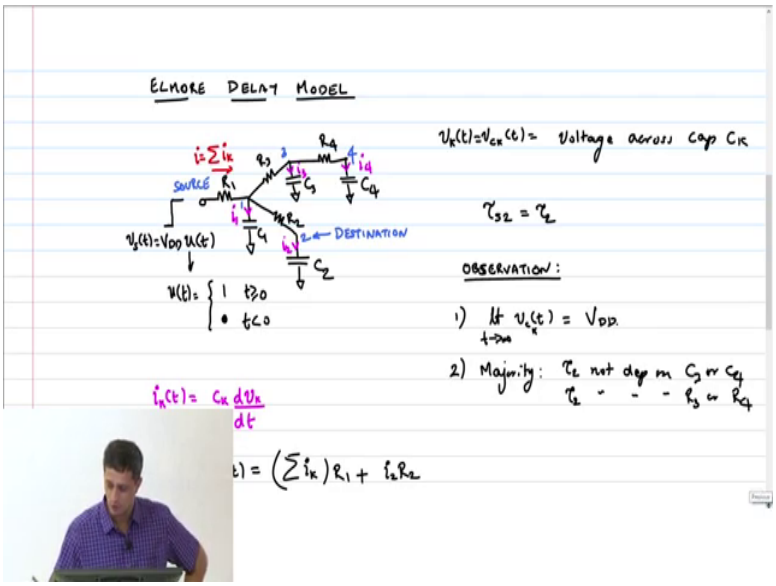

So, let us consider a simple not a simple network actually reasonably complex network. The same thing that I drew R 2 C 2 C 1, I have R 3 C 3 R 4 and C 4, ok. This is my source node and I am assuming that the input goes instantaneously from 0 to V DD; that means, V this is

my source, v s of t is V DD into u of t this is unit step function u of t equals 1 for t greater than equal to 0 and t less than 0, ok.

Now let us say that I pick node 2, ok. Let me put down the nodes in a different color node 1, node 2, node 3 and node 4 let us say I pick node 2 to be my destination node, and this is basically my source by the way. Now, I want to calculate the delay from the source to this particular destination ok. So, I want to calculate tau from source to node 2 or I will drop the source because it is redundant for all the nodes I will just call this as tau 2, ok.

So, before we start before we do any derivation let us try to intuitively understand what is going to happen here. Can you tell me what the steady state voltage will be on all the capacitors at t equal to infinity what will be the voltage on all the capacitors?

Student: (Refer Time: 08:49).

Exactly. So, first observation write 1 limit t tends to infinity of v c of v c k ok, because the and what is v c k? v c k of t is the voltage across cap C k this is equal to V DD, ok. Now, do you think the delay to node 2 will depend on C 3 or C 4, how many yes, how many no? Yes, it will depend on C 3, ok. So, majority seems to be let us majority tau 2 not dependent on C 3 or C 4, What about R 3 and R 4? So, the person who said it will depend you the it will depend on R 3 or R 4.

Student: (Refer Time: 10:27).

Yes, ok; tau 2 most others I think it will not depend on R 3 or R 4, ok. So, this we will try to resolve by the end of this derivation, ok. So, now, let us have we have put in some notation the current through each of these nodes I am going to call it as I 1, I 2, I 3, I 4, ok. So, the current I k of t, what is it in terms of v c k of t, I will simplify this drop the v c; I mean that C I will drop I will call it v k of t just because I do not need this capacitor in terms of v k of t what is it C k into d v k by d t, ok.

Now, it is a reasonable assumption to make that all these nodes are going to charge asymptotically to V DD, but they do not charge at the same rate each node is going to charge with its own time constant, ok.

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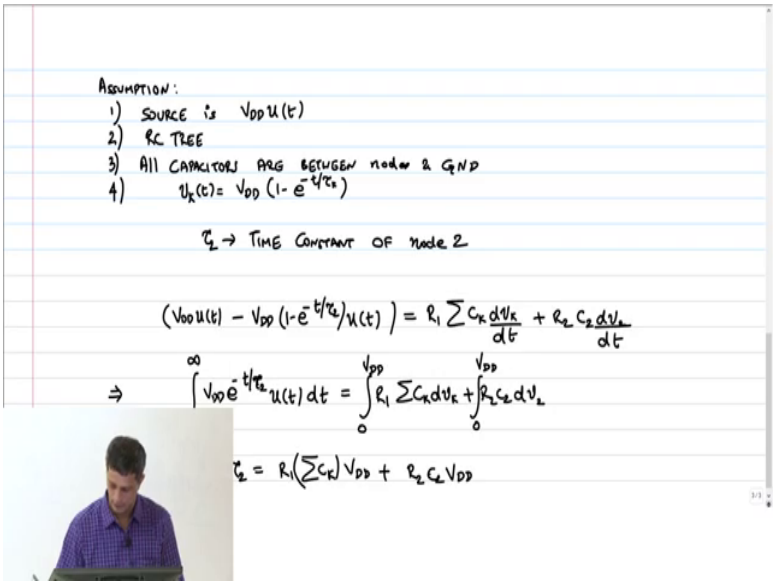

So, now we will write down the assumption, ok. 1 source is V DD into sorry no u of t which means it is an instantaneous voltage change, ok. 2, this is going to be an RC 3 what does an RC 3 mean, it means there are no loops. I do not put R and then take it back for example, from node 4 I do not put an R and bring it back to the source node or to node 1 there are no loops it is an R t R C 3 it just branches out.

And the third assumption is all caps are between nodes and ground; that means, there is no capacitor in series right they are only connected to resistors this is the necessary thing. Then we are also going to make the fourth assumption which is very reasonable to a first order that

v k of t is going to rise asymptotically with its own time constant minus t by tau k; node 2 will rise with a time constant tau 2 node 4 will rise with the time constant tau 4 ok. So, tau 2 is time constant of node 2 and that is our destination node now.

So, can we write kvl between the source node and the destination node? First of all what is the current that is flowing through R 1. Sorry.

Student: (Refer Time: 14:37).

Sum of all the currents, right; you apply kcl at node 1 basically all the currents are just going to add there and therefore, this current is i equals summation of i k. What is the current through R 2, I 2 right therefore, what is v s minus v 2, I can write now v s of t minus v 2 of t is basically a current through R 1 into R 1 the voltage drop across R 1 plus the voltage drop across R 2 which is summation i k into R 1 plus I 2 into R 2, right.

So, now we will go ahead and substitute all these things that we had v s of t is V DD into u of t, right; v 2 of t we said is V DD into 1 minus e power minus t by tau 2, t by tau 2 of course, into u of t again because this starts only at 0, right. This is equal to summation R 1 into summation of i k and what was i k each current it is just C k dvk by dt because the current is though that capacitor by definition c k dv k by dt plus R 2 into what C, ok.

So, now I am going to bring dt this side. So, this V DD vanishes it just becomes V DD into e power minus t by tau to u of t dt. We will put the limits later R 1 into summation C k dv k plus R 2 C 2 dv 2 of course, now I am going to integrate both sides. All the v ks are going to go from 0 to V DD in how much time? No, no they are going to go from 0 to V DD in how much time infinite time it is an asymptotic thing, right.

So, this is going from 0 to infinity 0 to V DD, ok. So, I you just integrate this you will get V DD into tau 2 equals R 1 summation C k into V DD plus R 2 C 2 into V DD, ok. Which implies tau 2 is R 1 into summation C k; k going from 1 to 4 plus R 2 C 2, any questions here, ok.

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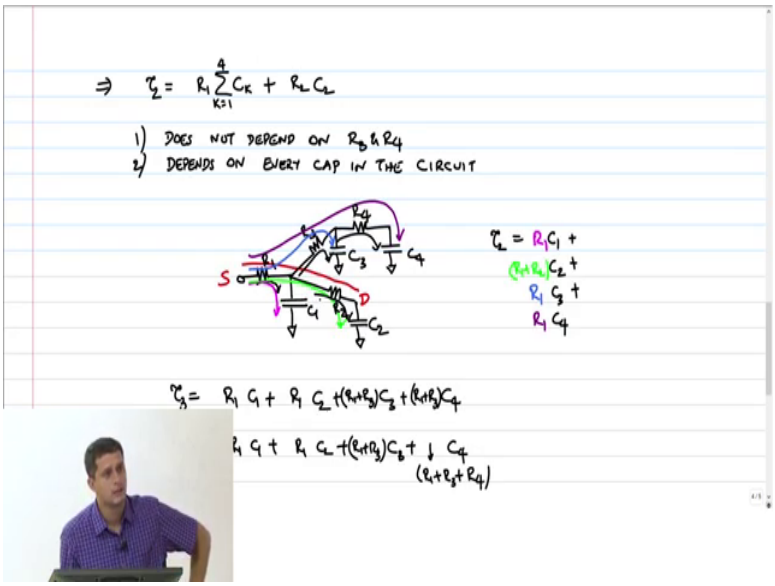

So, like yeah because to a first order we want the delay to be accurate in to the second order yes the delay may not exactly follow this, but what we want is a and first order estimate of the delay for back of the envelope calculations, right. Now, if you want the accurate number you have to do a simulation anyway ok, but this turns out that and it is true even intuitively all the capacitors do go like that asymptotically they do go to be ready right, they may not go exactly in that particular equation, but your first order its more than sufficient for us, yeah.

So, now let us go back to our observations, ok. 1; it does not depend on R 3 or R 4. R 4 2 it depends on every single capacitor in the circuit every cap in the circuit ok. So, let us just let me redraw that. So, that we get an intuition for what is happening and why it behaves like this. C 1, C 3, C 4, C 2 and R 2, R 1, R 3 and R four.

So, now, you look at what is going to happen? Suppose this node so, the current you turn on the source this first will try to charge this capacitor, the potential v 1 will go up slightly, but the moment v 1 goes up a little bit current will have to flow and start charging these caps as well, right. So, it is very intuitive that it has to depend on every single capacitor because the moment the source node raises current gets distributed to all the capacitors, ok.

Now, you can also do a limiting case suppose I make R 3 and R 4 0, what will happen to the capacitor C 3 and C 4? No, no what is the effect what is the net capacitance at node 1 there, yeah.

Student: (Refer Time: 22:02).

Yeah. So, that is one other check that you can do in that expression if I limit R 3 and R 4 to 0, it becomes a lump capacitor in which case of course, it is R 1 into C 1 plus C 2 plus C 3 or C 1 plus C 3 plus C 4 then R 2 C 2 is there, right. So, you can do these checks to intuitively figure out that it has to depend on every single capacitor, right. However, what is interesting is the delay depends only on the resistance that appear in the path from the source to destination, ok.

So, what is the path from source to destination I am starting from the source and going here; this is source, this is the destination. So, it depends only on the on path resistances, why is that because the current through R 1 happens to be the sum of all the currents right, but R 2 is basically just the current though C 2, right.

So, that is why you will see that; no, this is actually to tell you why it depends on all the capacitors anyway let us do that. So, if I want to write the delay tau 2 I will write it slightly different now. The right way to use this formula is because it depends on all the capacitors first you put down all the capacitors in the circuit, ok. I am going to so, this is plus. Now, I am going to put the resistance values before the C 1; now what should be the coefficient of C 1 here, R 1 plus R 2 you just look at this if I take the so, it is just R 1 C 1 yeah, correct no it is just R 1; what about C 2, R 1 plus R 2.

So, what you do is you go you put on all the capacitors go from the source to that particular node and C which resistances R matching with the destination node that you are considering, ok. So, what did we do first for C 1 we considered this path therefore, only this resistance came into picture let me color code it therefore, this is R 1.

Now I am going to go to node 2 capacitor 2. So, I go from source to node 2 like this and what are the resistances in the path R 1 plus R 2. Now, I am going to go to node C 3 right which I can do in blue. So, I am going to go like this, but my destination is to node 2. So, which is the resistance that is common to both that turns out to be only R 1 and therefore, this is R 1. Similarly for node 4 the same thing will happen I go all the way like this and the only resistance that is common is R 1 again, yeah.

Student: (Refer Time: 25:41).

Yeah.

Student: (Refer Time: 25:47).

Yeah.

Student: (Refer Time: 25:52).

So, it depends on what you mean by; so, I believe you should be able to neglect it, yes.

Student: (Refer Time: 26:11).

No, why do you say that? If I limit R 3 and R 4 to infinity, no the delay tau 2, tau if you look at tau 2 does not depend on R 3 and R 4. So, even if I limit them to infinity the number is the same.

Student: (Refer Time: 26:41).

No, what do you mean by limit; what do you mean by limiting R 3 and R 4 to infinity? You are going to increase the value to infinity in a sequence, but every number in their sequence is a finite resistance, correct that is what you mean by limit. So, if that happens for every finite resistance the delay is independent of R 3 and R 4 therefore, it does depend on C 2.

What you should check is maybe this first order approximation does not work at some very high limits that you should check through the simulation and that may break, ok. The first from the first order of approximation we are getting this that is for maybe there is a reasonable range of resistors and capacitors where this works that you have to go and double check in simulation if it worry checks, ok. So, any questions here, yeah.

Student: (Refer Time: 27:43).

. So, that is a very good question honestly I have not been able to give it I am not being able to get it as convincing an answer as I can tell you 4 capacitors. I am thinking about it I will get back to you sometime ok, it is got to do with the fact that the current through R 3 is just dependent on the capacitor charging that is all. This is my first order intuition that I have, but I do not have a conclusive answer yet for R 3 and R 4, why it does not depend on off paths resistances, ok.

So, I will think about this maybe the derivation should give you something. So, you also think about it, we will discuss it in the next class or hopefully I should have an answer by the next class or 2, yeah.

Student: (Refer Time: 28:39).

Yeah.

Student: (Refer Time: 28:42).

Correct.

Student: (Refer Time: 28:47).

True I know I know what you are saying. So, this is not a very trivial answer I do not have the right answer yet for this, ok; I will think about it you also think about it and we will discuss it maybe in the next class, ok. Intuitively, I do not have the answer yet for that through the derivation it is very evident because they just simply do not appear in the kvl equation that when I go from of this thing.

The other point to also check is in simulation if you try this is it really dependent on R 3 and R 4 is the question, right and again there is the range where that might break that we have to check, ok. So, the dependence on capacitance is very clear, the resistance is not that clear, yeah.

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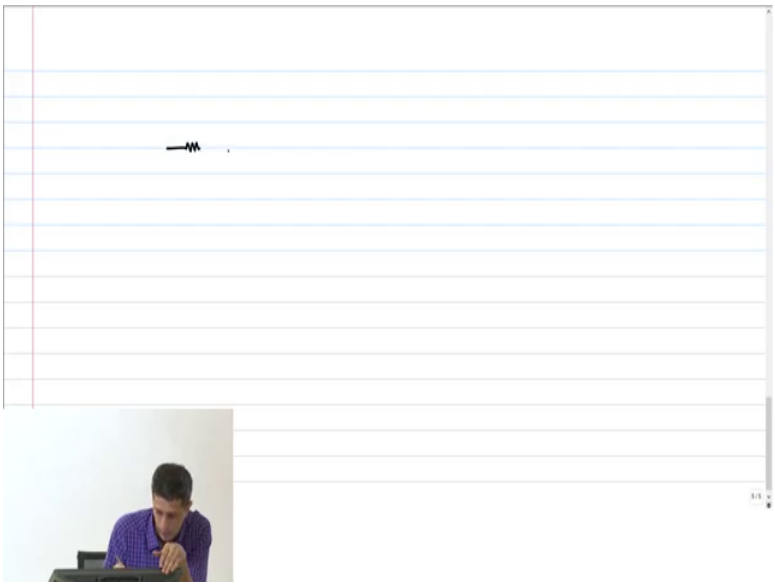

So, let us just maybe do one more example. So, that we get a feel for this or should I do a new circuit no, I do not have to do a new circuit, let us let us do tau 3 can you tell me what tau 3 should be in this circuit. So, what is the what are the steps that I told you, first you put down all the capacitors, right, then we will fill the coefficients of the capacitors ok, yeah. So, what should be the coefficient of C 1?

Student: R 1.

Yeah, R 1 C 2 yeah because I am now talking of node 3 the only resistance which comes in the intersection of source 2 node 2 and source 2 node 3 is R 1; what is it for C 3? R 1 plus R 3; what is it for C 4?

Student: (Refer Time: 30:52).

Yeah.

Student: R 1.

R 1 plus R 3, ok. Now, what is tau 4? Again, C 1 plus C 2 plus C 3 plus C 4.

Student: (Refer Time: 31:18).

Yeah, R 1; for C 2, R 1 yeah here.

Student: (Refer Time: 31:26).

Here? This is R 1 plus R 3 plus R 4, ok. So, this you will have to learn to apply very diligently correctly in various scenarios, ok.