Digital IC Design

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Lecture - 25
NMOS Transistor ON Resistance and Fall Delay

So, the idea is we have derived equations for the currents of the transistor, we know how the transistor behaves with various voltages and stuff like that that is fine. But, how are we going to use this transistor, invariably we are going to only use this transistor either to charge a capacitor or discharge a capacitor.

This entire course is all about that how fast you can charge the capacitor, how fast you can discharge the capacitor right. This capacitance can be because of its own parasitic capacitance like, I will discuss today or it can be because of a load capacitance right, so I have a capacitance discharging.

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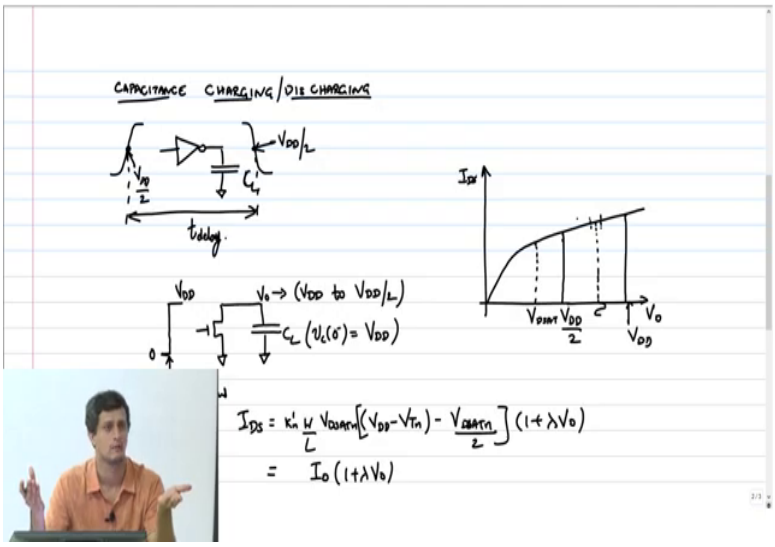

So, if I have an a logic inverter driving a load capacitance right this inverter is going to either charge this capacitor or discharge this capacitor, and the delay of the gate is determined by how fast this action can happen ok. So, I also told you that delay is defined as the time it takes for the input to go to 50 percent right from there till the time the output reaches 50 percent ok.

So, if this is my V DD by 2 and this also is V DD by 2, then the delay of the gate is defined exactly as this delay ok, this is the delay and we want to estimate this ok. So, the simplified picture is we have a capacitor CL and an n mos is going to discharge it, we will see why and n mos cannot charge the capacitor or a p mos cannot discharge a capacitor we look at it later ok.

But for now let us just look at this picture, the capacitor is charged v C of 0 minus equals V DD. So, this inverter is going to now discharge the capacitor through an n mos transistor ok. So, this voltage V naught is going to fall from V DD to V DD by 2, because of the delay

definition that is why V DD by 2 is a very sacrosanct number, I am not worried about taking it all the way to 0 ok.

Now, we have to make some assumptions to simplify our analysis otherwise it becomes very difficult. So, if for example, you the input is going to rise slowly like this, then that delay becomes a little hard to handle right. If it becomes a ramp function then I have to see when the delayed when the device turns on when it goes into linear, saturation all that it's it is very painful to do that. So, we have to make some approximations to get a first order number and then we will incorporate this input see also later on.

So, the assumption we are going to make is the input rises instantaneously to V DD ok, 0 to V DD instantaneous ok. So, if at 0 plus the gate is at V DD my v out is also at V DD right and 0 plus just after write down it on in what region of operation will my transistor be in saturation region or velocity saturation right. Because V GS is equal to V DD; obviously, V DS has to be greater than V GS minus V T you are removing some quantity from there therefore, the transistor is in saturation region ok.

So, the currents look like this I D and this is V naught, so right this is my points where it is V DD. This is V DD and somewhere here is V DD by 2, I am assuming V DD is large enough such that it is to the right V DD by 2 is to the right of V DD V D SAT ok. So, that I do not have to deal with a change in region of operation ok, so this is an assumption.

So, what is the equation of the current IDS? Let us say its velocity saturated it is K m prime W by L into V D SAT n into V. What is V GS? V DD right VDD minus V Tn minus V D SAT n by 2 into 1 plus lambda V naught. Suppose is a long channel device then this would be in saturation where this would just be Kn prime by 2 W L VGS minus VT V DD minus VT is the whole square ok.

So, let me not worry about all that I will just write this as I naught into 1 plus lambda V naught ok. Whether it is velocity saturated or not or it is in saturation I naught is independent of V naught that is the only thing I am worried about ok. So, now just look at the picture the

V naught is coming down, its being the capacitors discharging right V naught is just the voltage across the capacitor and the voltage is coming down.

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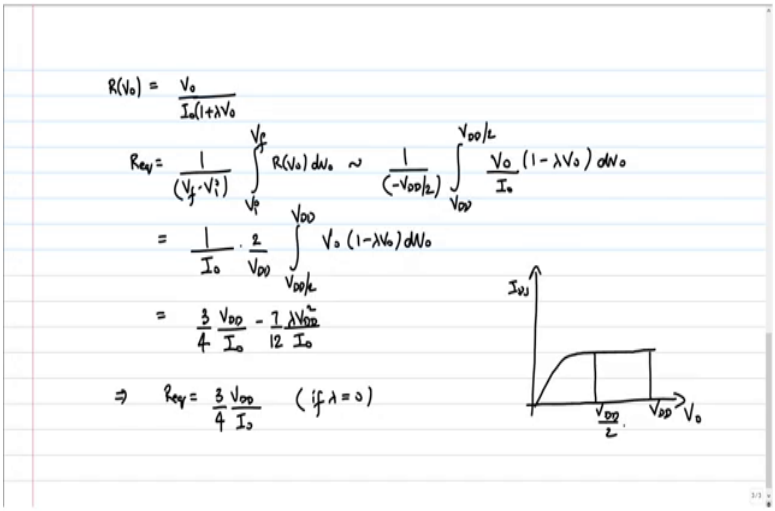

So, if you look at the resistance, it now becomes a function of V naught ok, so last class somebody asked me why do not you do a derivative out here. See in analog it is to do a derivative because, you fix your bias somewhere here and then you will do some sort of a small signal analysis over that bias point.

So, in some sense we have linearized this whole thing here, so when you do a Taylor series there you going to take a derivative and then you expand it in terms of the input variables. So, therefore, you take derivatives there, but here I am actually discharging it from V DD to V DD by 2 it such a large range right.

So, I cannot do that small signal also taking derivative here, I have to find some other way of finding the resistance average resistance, now which is a function of v naught right. So, R of V naught is simply what V naught by I naught into 1 plus lambda V naught. Now, I have a function f of x that is going from a to b, I want to find what is the average value, what do you do you just integrate and divide by the x 2 minus x 1 right that is all I am doing here.

So, I am saying that R equivalent is defined as V final minus V initial into V in initial to V final of R of V naught d V naught that is my that is what I am defining as the average resistance ok. So, this I will now write as minus V DD by 2, because V f is V DD by 2 V i is V DD. And, so I am going to write this as V DD to V DD by 2 into V naught by I naught write that 1 by 1 plus lambda v naught I am going to write as a Taylor series because lambda is very small ok. I can expand this approximately as 1 minus lambda V naught ok, maybe I should put an approximate here d V naught.

Of course, now I naught is a constant, so I will just write into 2 by V DD into V naught into 1 minus lambda V naught d V naught right. So, what did we get the answer here you solve the integration and you just get what 3 by 4 V DD by I naught minus 7 by 12 lambda into V DD squared by I naught right this is what we got fine.

So, if it is going to have channel length modulation then this is the only way you can do it, because there is a variation of resistance all through because of that 1 plus lambda V naught right. So, now, the interesting thing is if it is a long channel device, then lambda is equal to 0 ok.

So, implies R equivalent is 3 by 4 V DD by I naught is lambda equal to 0 ok. So, the point I was trying to make last time is we found an equivalent R right, why are we finding equivalent R? Because, I can now treat this as an RC discharge and I can evaluate delays in terms of the time constant of that RC network ok. But, if lambda equal to 0 then this is just like a constant current source discharging my capacitor, why is it a constant current source? Because, there is no dependence on V naught.

Now, if lambda equal to 0 the current basically just becomes a IDS versus V naught; this simply become the flat line and this is my region of operation from V DD to V DD by 2 ok. And of course, now I do not have to worry about V D sat, because this will always be in this thing you know you have to still worry about it.

You have to make sure the vt is above some number below some number for it to be in saturation region all through ok, so assume V DD is high enough there is no problem. So, this is now like a constant current source discharging the capacitor ok, so we did the same calculation in method 2.

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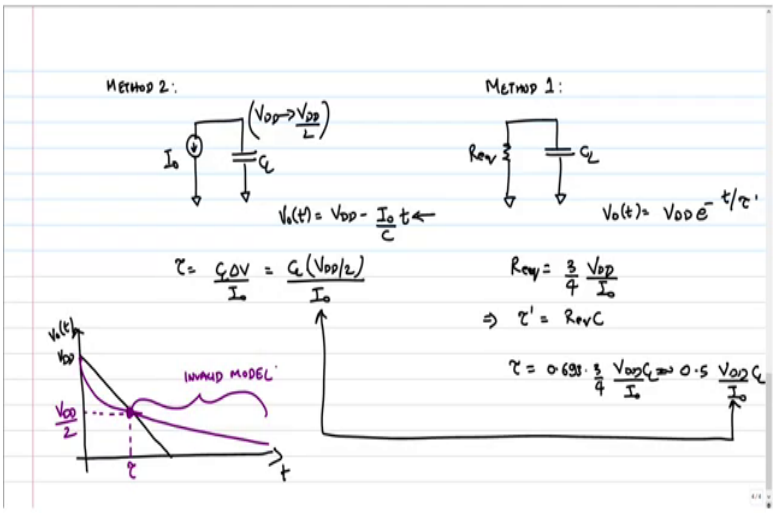

So, it is a constant current source discharging my capacitor; method 1 is you had a thing like this R equivalent into and C L. Now, what is the time it is going to take two and what is this current is I naught by the way if lambda equal to 0 this current is just I naught. What is the

time it is going to take to discharge from V DD to V DD by 2? If it is a constant current source discharge C delta V by I right.

So, the time is C delta V by I naught C L right, C L into V DD by 2 divided by I naught. Here the R equivalent was 3 by 4 V DD by I naught which implies that the time constant of this RC network right let me call it tau prime is R equivalent into C. Now, the delay of this thing to come from V DD to V DD by 2 is 0.693 times the time constant, so this is 0.693 into 3 by 4 V DD by I naught right.

So, this is approximately again we will get 0.5 1 or 5 2 or something like that, I naught into C L, now these two answers indeed do match right. Now; obviously, if lambda is 0 then the constant current source model is the right model, because the transistor is a current source ok. So, if you look at the model that we are using for delay ok. This guy is if you look at this V naught of t it will start from V DD and then go linearly right.

What is this? C d V by dt equal to I, so I naught by C into t whereas, this guy if you see V naught of t this V DD e power minus t by tau prime. So, the 2 models actually follow different equations with respect to time, but this one is more accurate ok. So, if you look at V naught of t versus t, you have a straight line like this for method 2, the method 1 is going to look like this asymptotically it will go down to this thing.

So, this is my delay tau and this is V DD by 2, so the two models give the same answer at that particular instant of time, any other instant the two models are different right. The delays are the same, question why do you why do we even want to do it to the resistance method? One is of course; if there is channel length modulation then this current source thing fails.

I have to now if you can of course; solve this from first principles by saying that I equal to minus C d V by dt. And use the equation of the you know make I dependent on V and solve the differential equation then its fine. Otherwise I need to do it through this resistance method which is a reasonable approximation; because all I am worried about is that delay act when it comes to V DD, this is the only point of interest in this model for me.

So, if you ask me which is better it does really does not matter right, and I also pointed out that beyond this both the models are actually not valid. Because when it drops below V DD by 2 and eventually goes below V D sat, the transistors goes into a linear region of operation right and there the equation itself changes.

So, when I do that resistance calculation it will go into a different region of operation altogether. So, that is not even worth sort of going through all the way down to 0 with that equation because it is not of interest to us ok. So, beyond this invalid model, the reason I am pointing this out is you will see that we use certain models in this course which are valid only in certain regions of operation.

Outside that region of operation if you ask me what the value of the model is I would say I do not care, because the model is not even meant to handle that region of operation that is the point I am trying to drive home here. Any questions? So, the other thing is of course, later when I start putting transistors in series or in parallel. Then I it is very easy for me to reduce that network using series parallel resistance combinations if I know R equivalent current source model I cannot do that. Any questions here? Ok.

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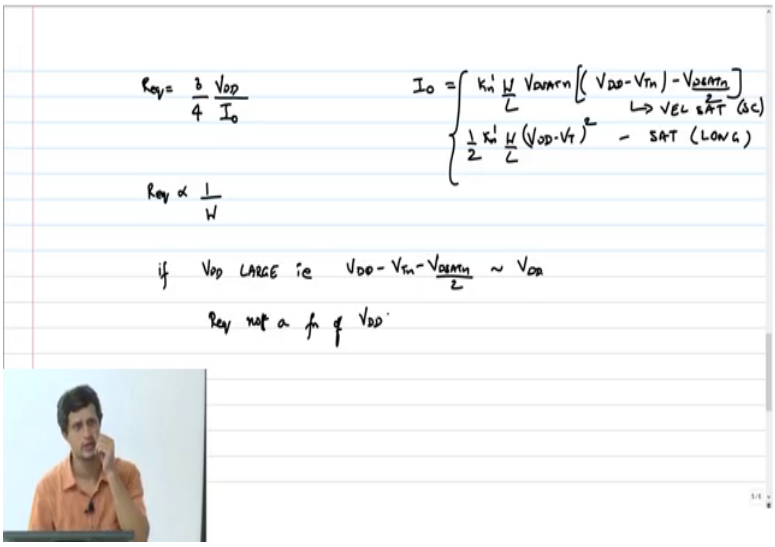

So, let us look at this equation a little more closely R equivalent is 3 by 4, I leave out this lambda parameter I naught ok. If it is velocity saturated then I naught is equal to K n prime W by L V D SAT n into V DD minus V Tn minus V D SAT n by 2 ok. If it is a long channel device and it enters saturation region then it is just K n prime W by L into V G V DD minus V T whole squared and half right.

This is saturation velocity saturation it does not matter, so this is a long device this is a short channel device ok. So, look at this equation of R equivalent now right, clearly it is going to be inversely proportional to W 1 over W, because I naught is sitting below right. So, therefore, if I double the width of a transistor then the resistance of the transistor drops by a factor of 2 right, or the resistance becomes 50; 50 percent of what it was earlier.

So, this is one key technique that we will use if you want to reduce your resistance then you up size the transistor and that is what this equation is also telling us right. Now, what happens if V DD is very large? Suppose V DD is very large such that V DD minus V Tn minus V D SAT n by 3 right or V DD is very large compared to V t then what will happen? Yeah? If its velocity saturated and V DD is very large what happens to the R equivalent as a function of V DD. Yeah?

But there is also an inverse dependence on 1 by V DD minus V Tn minus V S SAT n no. So, if we are V DD is large right, what does large mean? That is V DD minus V Tn minus V D SAT n by 2 is nearly V DD right. This is just a first order thing, this show you that R equivalent then is not a function of V DD.

So, if I have a 180 nanometer device and I operate it from one you know 1.8 volt down to 1.5 volt, then the R equivalent will not change much there ok. On the other hand if your V DD is very small, then of course; these things cannot be neglected and that has a more complicated relationship with V DD. In this course we are going to deal only with higher V DDs, we are not going to bring down the V DD close to suppress hold or even low voltage operations ok.