Digital IC Design
Prof. Janakiraman Viraraghavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture – 24
Pass Transistors

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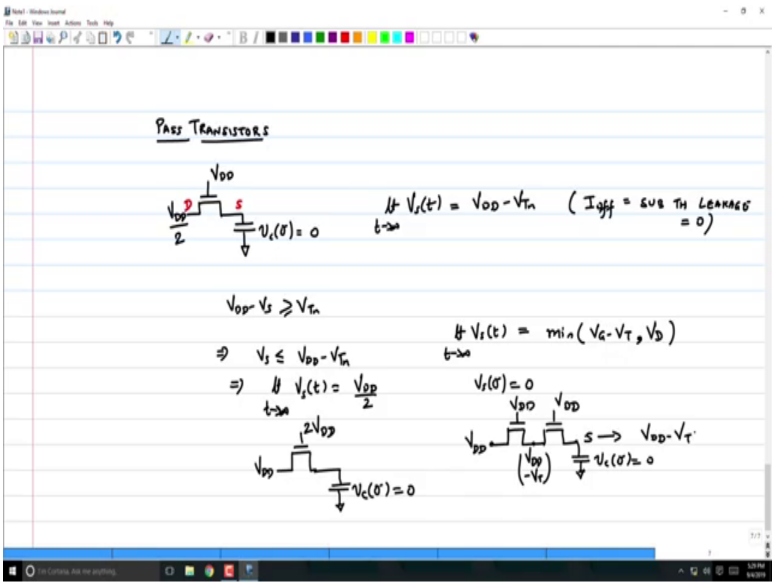

So, Pass Transistors, ok. We looked at this briefly you know in the initial part of this module when we wanted to figure out if you should put the NMOS on top or NMOS down, PMOS on top or PMOS down and all that, but we look at that in little more detail that. Now, I am going to connect this to V DD, I am going to connect this to V DD assume that this capacitor is discharged. So, what is the drain and source first? V DD is?

Student: Drain.

Drain source right; now, what happens to the source side, it will charge up to?

Student: V DD.

V DD?

Students: Minus.

Minus V T, ok. So, this V S of t maybe I should write here limit t tends to infinity V S of t is V DD minus V T, ok. And, this is assuming I off weight equal to sub threshold leakage equal to 0 because if I off is their then eventually it will charge to V DD, because there is some small current flowing of through, very small current very slowly it will go to V DD.

So, I cannot make the statement at limited t tends to infinity of V S of t is V DD minus V T, ok. If I off is 0 then yes it will go up V DD and V T and then cut off. Now, what happens if instead of V DD, I was trying to pass V DD by 2; what will V S of t, limit T tends to infinity b?

Student: V DD (Refer Time: 02:23).

V DD by 2, right. So, this this transistor can conduct as long as V DD minus V S is greater than or equal to V Tn, right implies that V S should be less than V DD minus V Tn. The key point is you should only be less than V DD, it only gives you a bound it cannot go beyond V DD minus V Tn.

But supports, the drain itself was a value which is less than V DD minus V Tn then; obviously, there can be no current flow any further after the sources has starts to the drain voltage, right. And therefore, it has to go only up to the drain voltage right, which implies for this condition limit t tends to infinity of V S of t will basically be V DD by 2 yeah, any question.

Student: (Refer Time: 03:28).

Student: Sir, (Refer Time: 03:31).

No, earlier I did not understand.

Student: Listen sir, (Refer Time: 03:55).

No.

Student: (Refer Time: 03:40).

You mean for V DD by 2 it will happen much before infinity.

Student: Yes sir.

No the nothing is again if you look at that current equation at some point this transistor will go into a linear mode right, where the current now depends on V GS. So, as V GS keeps dropping, but current also will give dropping. So, that also is basically an asymptotic behavior only, ok. So, this is a correct statement to make, ok. So, how do I combine these two statements that I just made now?

One is it can go up to V DD minus V T right the other is it can go up to whatever the drain voltages, right. Now, I will give you another case let us say that this transistor drain is that V DD, v cf 0 minus equal to 0, this thing is at 2 V DD then what will happen, it can go up to?

Student: V DD.

V DD again, right. So, how do you combine these two things? So, you can say that V S of T limit T tends to infinity assuming that V S of 0 minus equal to 0, ok. We will go to max of no max or min? Min V G minus V T comma V D. Here, I am not saying V GS minus V T, V g whatever the gate voltage is minus V T or it can go up to the drain voltage, right. So, what will happen if I do this V DD, V DD, this is also V DD this capacitor is discharged. So, what will the node S go to finally?

Student: (Refer Time: 05:53).

Student: V DD minus (Refer Time: 05:55).

V DD minus.

Student: 2 V T.

Why 2 V T?

Student: V T (Refer Time: 06:02).

Yeah.

Student: Behavior is not (Refer Time: 06:06).

It will basically go to V DD minus V T because this guy can go up to V DD minus V T. Now, this guy can go to min of V DD minus V T and V DD minus V T, drain is also at V DD minus V T assuming that these two are say have the same V T, right. So, therefore, this will eventually go to V DD minus V T. I leave it to you to figure out in what configuration will it actually go to V DD minus 2 V T, think about it, ok.

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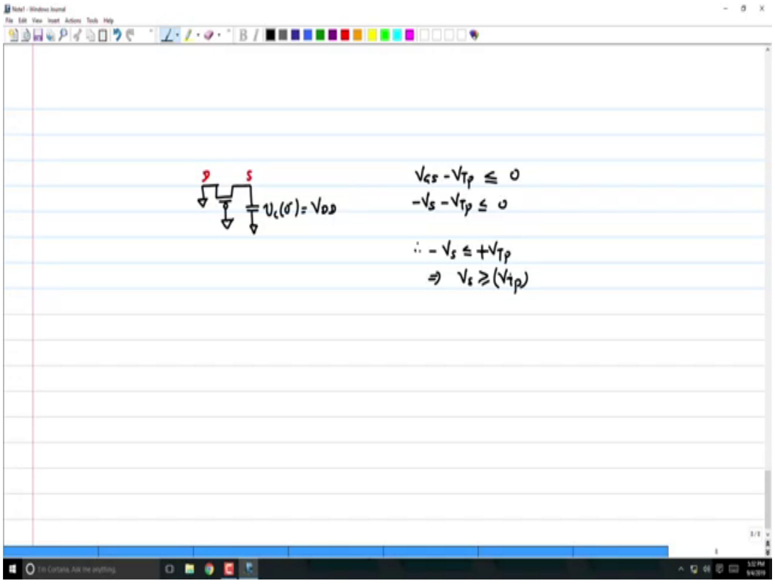

Similarly, what happens if I have a PMOS transistor like this, where I am going to do the following. I have v c of 0 minus into V DD, and this is going to come down to I am going to ground this guy and this also I will ground. What is the drain and source first?

Student: (Refer Time: 07:22).

Yeah.

Student: Drain is at (Refer Time: 07:24).

Drain is at.

Student: Ground (Refer Time: 07:28).

Drain is at ground, this is source so; obviously, this transistor initially has a high enough.

Student: V GS.

V GS right and therefore, or a high enough mode V GS and therefore, it turn on it will start discharging the capacitor, but it will can discharge a capacitor only until V GS minus V Tp is less than 0. What is V GS of this transistor?

Student: (Refer Time: 08:07).

Sorry.

Student: (Refer Time: 08:10).

It is basically minus V S because the grate is grounded minus V Tp should be less than or equal to 0. Therefore, V S minus V S should be less than or equal to minus V Tp implies V S, mod V S is this right.

Student: Plus V Tp sir.

Sorry.

Student: Plus V Tp.

Plus V Tp correct, implies V S should be greater than mod V Tp, right. So, how will you right this general condition, I have a gate voltage, I have some drain voltage, capacitors initially charged to V DD, right. I think this will be little hard to put down in a general thing because it depends on what the voltage is r, right. So, I think it is better you just apply this particular condition that identify drain and source first, V GS minus V Tp should be less than 0 and then you find out up to what it can go to, right.