Digital IC Design
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Lecture – 23
Noise Margin Analysis – Long Channel Device Inverter

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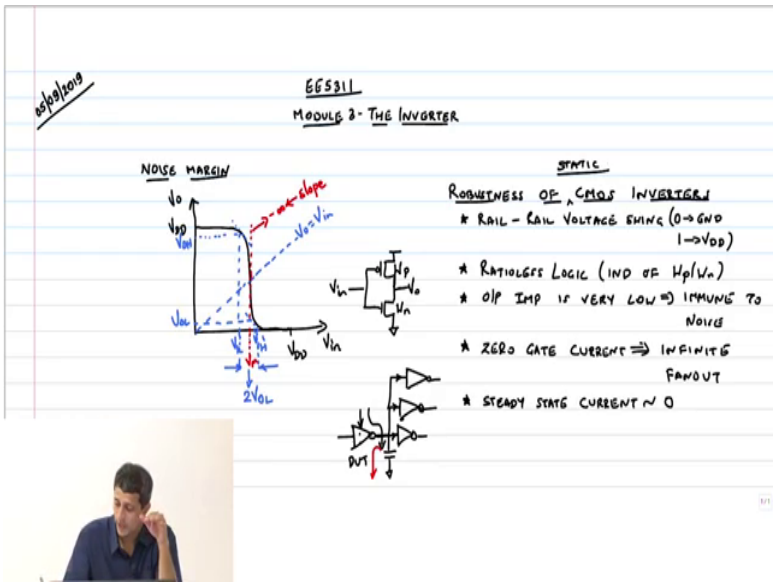

So, we derived from first principles the values for V IL and V IH for a long channel inverter right and we said we needed to make no approximation what so ever to handle this case. So, we got accurate expressions right. So, the key feature of a long channel inverter is at this point of V out equal to V in right and this is by the way V out versus V in and this is going all the way up to V DD.

The slope at this particular point was minus infinity right. And therefore, we went ahead and derived the exact expressions for the noise margins and V IL V IH and all that and we got.

So, this was V IL V IH. Sorry H corresponding values V OL V OH right. And in the process of deriving the whole thing we came up with this thing that in a long channel inverter this region of indeterminate input where the input is considered neither high nor low.

And will be governed by noise is actually a very small region and that width is 2 times V OL. Remember V OL is actually very close to 0. As you can see here also I have drawn a little exaggerated it is, but it is supposed to be 0, it is very close to 0. So, this region of indeterminate ray of where the input is indeterminate is just 2 V OL and this is not surprising because the slope at V in V out equal to V in is minus infinity.

So, this is the closest you can get to an ideal inverter or an ideal voltage transfer characteristic that we were looking for. We wanted the ideal characteristic to be somewhere on this red line right. We wanted this to be you know my V m and then that to be the region of transition from low to high, but this is the closest we can get ok.

So, let us just summarize our discussion on robustness; robustness of CMOS inverters; V in V out right. First key point logic voltage levels are rail to rail values right. So, rail to rail voltage swing. It means logic 0 is ground logic 1 is V DD ok, but for that small leakage current which is really negligible this is definitely true.

When the input is 0 output is V DD. When the out input is V DD output is 0 right. Second important point it is the ratio less which means it does not depend on what my value of W p and W n are; whatever the values the voltage swing is rail to rail. It is a ratio less logic which means it is independent of W p by W n. You will see why it is called ratio less because, later we will do ratioed logic where it will depend explicitly on this W p and W n value ok.

Third thing is output impedance is very low. In a sense the output is driven very strongly to either ground or V DD because when the NMOS turns on it is turned on very strongly and it pulls the output to logic low. When the PMOS is turned on and the NMOS is off it is pulled to logic high through a very very low resistance part and therefore, this implies it is immune to noise.

So, you know there is a glitch at the output it cannot like you know just go up and down or it will not go to some other value and settle. It come back to it is original value ok. Third thing not third fourth point what is the input current to that advent? Exactly. So, basically 0 gate current implies if you are not worried about delays this is infinite fan out.

What does this mean? If I have an inverter like this fan out is basically how many other gates it can drive what load it can drive ok. I want to drive 1, 2, 3 gates and so on. So, how much current is available for charging or discharging this capacitor is primarily dependent on the transistors in this inverter. Whatever that PMOS can provide that is a charging current whatever the NMOS can provide that is a discharging current.

Now if some small gate current had to be was needed in order to drive the other inverters then you are going to limit this current that is available for charging or discharging the capacitor right. Now, because this gate current is 0. Why is the gate current 0? Because, it is going to an insulator gate is an oxide silicon dioxide and therefore, or hafnium oxide and therefore, that is like an insulator and it can tolerate 0 current. A BJT for example, has a very very small base current. I cannot make this assumption for a BJT.

Now, therefore, any current that is available from this device under test right, DUT my device under test will be entirely used to actually charge this capacitor or to discharge this capacitor which means it has infinite fan out ok. So, these are the very very significant advantages of CMOS circuits and that is why it is dominated VLSI design since 1980 right. Somewhere around the first second or second microprocessor or so people switch to CMOS logic and it has been used left right and center right.

The first transistor was made somewhere in fifties or something right in a lab right. The demonstration of the first IC was made not transistor IC was done in sub 50 somewhere. By 80s it had reached mass production and since 80 still now it is simply dominating VLSI technology and it is very hard to displace this technology because of all these advantages that are there here right.

The kind of current, the kind of control ease of manufacture ability all of these make CMOS logic right very very attractive right. And, the one of the most important advantages is steady state equal to 0 which means is we put approximately C ok. It is very very low because if my NMOS is on right; that means, the PMOS is off right. So, there is really no conduction path from V DD to ground in steady state and that is where my clock will be for most of the time. It will make a transition then goes to sit in 1 or 0.

Every node in my circuit will go and sit at some logic level and whether it is logic 1 or logic 0. There is no conduction path from V DD to ground and therefore, it is almost 0. So, this current is actually leakage right. So, only now it has started to show up significantly late maybe last 2-3 generations makers current has started to show up significantly, but for a long time this leakage current was failing exist negligible ok.

So, this is the summary of the robustness of CMOS inverters and CMOS logic in general I should also maybe add another word here called static CMOS. This word static refers to the logic being driven to either power or ground through low resistance path ok. Later, I will talk about dynamic circuits where the output will go and sit on a capacitor and the capacitor is floating. There is nothing driving that.

So, capacitor has to hold that voltage and that becomes a dynamic node ok. So, here the static refers to being driven to supply or ground through a low resistance path which means that as long as power is on that logic state will remain forever. Of course, if you take the power off you lose it ok. So, with that we conclude the discussion on robustness noise margin and other aspects of the static CMOS inverter.