Digital IC Design
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Lecture - 22
Noise Margin Analysis- Long Channel Device Inverter

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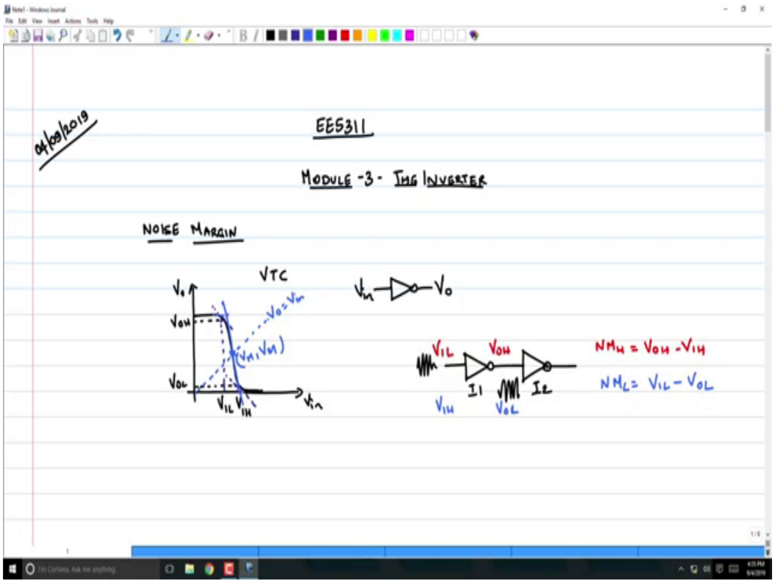

So, we were discussing Noise Margin last time right and what was the idea here? We basically had the Voltage Transfer Characteristics: VTC V out versus V in for an inverter like this V in V out ok. So, the VTC is like this and we said that the point at which the slope becomes minus 1 is of significance because before that right or outside that this signal gets attenuated or noise gets attenuated, within that region the noise gets amplified. And therefore, the region of importance is between the points at which the slope is minus 1, ok.

That is why minus 1 is a magic number here ok. So, we basically said that this was V IL this was V IH right, the corresponding y axis coordinates where defined to be V OL and this was defined to be V of H, ok. So, the idea of noise margin is if I have one inverter driving another inverter like this and I have noise fluctuating here right, then how does it go and get how does it affect.

You know if I have noise on each of these nodes, then how does the signal propagation get affected was the question right. So, for example if the input was V IL, then the output of the first inverter which is I 1 and this is I 2 output of the first inverter, I 1 would be V OH right, but for V OH to get recognized as a logic high for inverter 2 V OH has to be greater than V IH, right.

So, therefore, the noise margin high is V OH minus V IH. Similarly if you give V V IH here, then you would get V OL here. The output of the first inverter will give you V OL and for V OL to get recognize as the logic low on inverter I 2 V OL has to be less than V IL. Therefore, the noise margin low is V IL minus V OL.

Why noise margin? Because I have that much of margin for the noise to actually cause a fluctuation and not cause a change in the output right. That is the margin that I have and that is why it is called Noise Margin and of course, to derive this you know we had to make some assumptions. Earlier we said that we will take this point where V in is equal to V out, right. This is V out equal to V in and this point we would call it V M, V M that is both input and output are the trip point V M.

And, it would be said that we will just extrapolate this slope right and then whatever intersects here this is what we call V IL and this point we called as V IH right. This is what we did earlier. So, last class we stopped at the point when we started discussing Long Channel Inverter. Suppose we had a long channel device instead of a short channel device, then what would happen to this assumption is this model even valid right.

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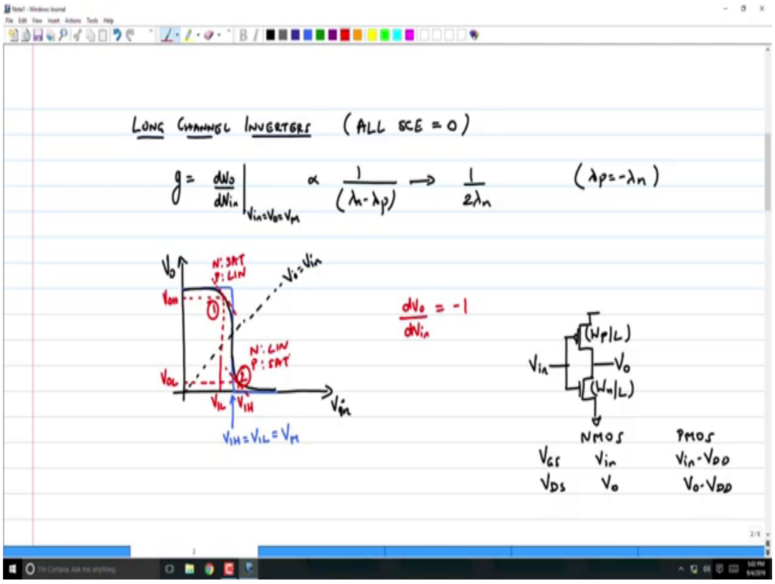

So, let us go back to long channel inverters which means that all short channel effects equal to 0. No channel length modulation, the velocity saturation voltage is very high right. So, therefore from linear it will only go into saturation right and all these things basically just vanish from our discussion ok. So, now if you remember the gain expression right equal to dV out by dV in at V in equal to V out equal to V m was proportional to 1 over lambda n minus lambda p, right.

And this is nothing, but if lambda p equals minus lambda n, then this would be 1 over 2 lambda n right. So, because of very small value of lambda n channel length modulation, this gain is very high and we got some expressions from that right, but of course in a long channel inverter, what is lambda n? 0. So, therefore if I use this particular model to derive the V IL and V IH of the inverter of a long channel inverter, what would happen is because at this point which is V in equal to V out, sorry without equal to V in, right.

At this point if I consider the gain, it is minus infinity right. It is not plus infinity because the curve will fall minus infinity and therefore, if I do the same extrapolation the curve will just extrapolate like this and both V IH V IH equal to V IL equal to V m, they will both simply collapse to this point though whatever I have shown here is not the V TC of a long channel inverter. This is the model, that we used where we extrapolated the slope at V in equal to V out equal to V m and pull that line all the way up that is the blue line the actual V TC is what is shown in black here, it will come like this. At this point, it will be minus infinity and then again it will be V it like this.

So, clearly this model that we used earlier works only for short channel device inverters where lambda n and lambda p are non-zero, right. So, now the question is how do I derive an expression for V IL and V IH for a long channel inverter, right. So, it turns out that the model was used in the first place because the expressions, current expressions for short channel inverters was very complicated. And therefore, actually solving for this point when the slope is actually minus 1 on both sides was very hard.

Because, you had velocity saturation, then you had channel length modulation, you had so many things, right. There is so many dependence on V in and V out, so solving for this point where dV out by dV in is minus 1 was very hard in a short channeling matter. Therefore, we use the approximation and the model and that is a reasonable model, right. Now it turns out here that you do not have to actually use that model at all. You can derive everything from first principles, right.

This is p i l V IH and this is V OH and this is V OL right. So, at 0.1 and this is 0.2 dV out by dV in equal to minus 1 that is a definition for the noise margin, right. So, in region one in which mode of operation is the NMOS which mode of operation is the PMOS yeah, ok. I need to this is something you should really get used to you know. So, maybe let us do it again.

So, that you this is V in V out, this is W p by l, this is W n by l in region one V OH is nearly V DD, very close to V DD, right. So, let us again write these expressions V GS V DS sorry V DS for NMOS and p mos. So, V GS is what for the NMOS in terms of V in and V out V in what about V DS V out PMOS V in minus V DD and V DS V out ok.

Now, V OH is nearly V DD right. Therefore V DS for the NMOS is what V DD nearly V DD, right. V in is what you can assume. It is just about threshold somewhere it is a very small value. So, in which region of operation is it V DS is greater than V GS minus V t and therefore, NMOS has to be in saturation. So, in region one NMOS is in saturation PMOS is in linear right, in region two NMOS in linear PMOS is in saturation. So, we will now use these expressions in order to solve for the points V IL and V IH.

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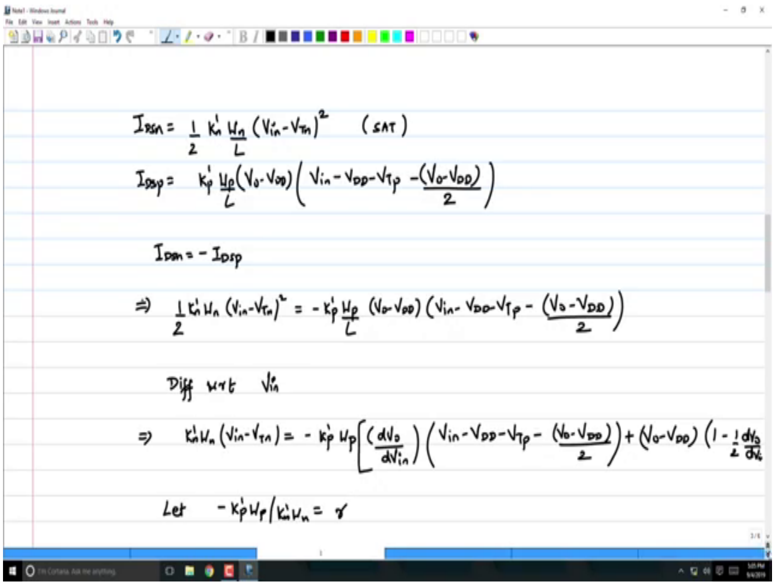

What is I DS n? What is the Saturation Current? Remember there is no velocity saturation. Now it is in it is a long channel inverter. So, directly it is going to go into saturation. So, what is I DS n half K n prime W n by l into V in minus V t n whole square, right. This is in saturation current. What about I DS p? Yeah K p prime W p by l into it is a linear current, right. So, it is V DS into V GS minus V t minus V DS by 2. What is V DS? V naught minus V naught minus V DD into V in minus V DD minus V TP minus V naught minus V DD by 2: right.

Now, again we impose our good old condition I DS n equals minus I DS p right two transistors in series one. Current is going up, one current is going down. They have to be the same and therefore, I DS n equal to minus I DS p which implies I can now write half into K n prime W n into V in minus V t n the whole squared equals minus K p prime W p by l into V naught minus V DD into V in minus V DD minus V TP minus I will just leave this as it is, ok.

I am not going to simplify that V DD term for now, right. So, now what do you do, differentiate both sides with respect to V in differentiate with respect to V in implies K n prime W n V in minus V tn equals minus K p prime W p into d V naught by d V in into V in minus V DD minus V TP minus V naught minus V d by 2 plus V naught minus V DD into 1 minus half d V naught by d V in, right. Now, let us let minus K p prime W p by K n prime W n equals r, right.

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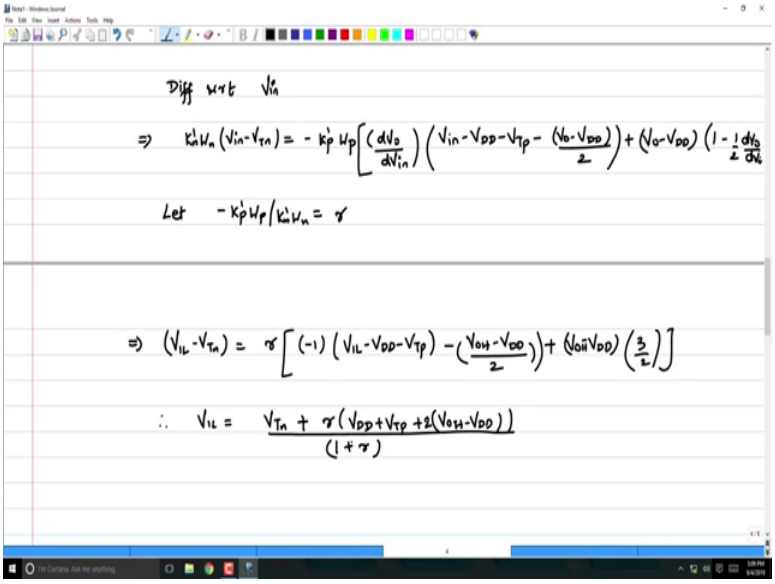

Then I can say implies V in minus V T n equals r times dV out by dV in. What is dV out by dV in? At that point minus 1 right; so, therefore I can write this as minus 1 and what is V in at that point V IL at that point when the slope is minus 1, there by definition it is V IL right into V IL minus V DD minus V TP minus V OH minus V DD by 2 right.

Correct plus p out minus V DD into 1 minus half of dV naught by dV in will just become 3 by 2. So, can you now simplify and get me an expression for V IL. Do not make any assumption right. V out by the way is what actually it is V OH, yeah. Can you now simplify this expression and get me the expression for V IL? Are you getting this expression? Are you getting this expression right ok.

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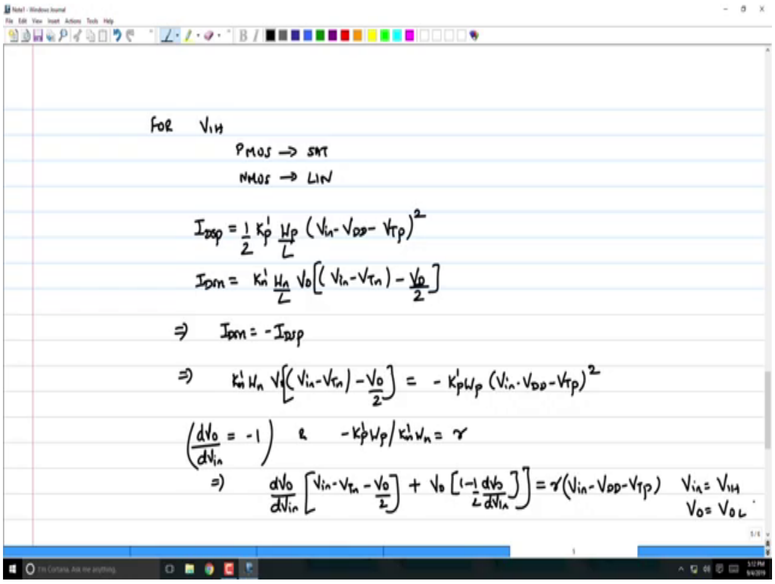

Now what about V OH V OH? You got to do the exact opposite right. For V IH PMOS is in which region? Saturation NMOS is in linear, ok. So, can we write the expressions of the currents ids p is K p prime half W p by l into V G s minus V T p the whole square right which is nothing, but V in minus V DD minus V TP whole squared and ID S n equals K n prime W n by l. What is V DS for the NMOS? Yeah V naught. What about V in minus V T n minus V naught by 2, right.

Again I go ahead and do the same thing if equals minus ID S p which implies K n prime W n into V naught into V in minus V T n minus V naught by 2 equals minus K p prime W p into V in minus V DD minus V TP the whole square. Again differentiate with respect to V in dV out by dV in equal to minus 1 right. Use this fact implies K n prime and minus K p prime W p by K n prime W n equals r which implies I can write dV out by dV in into V in minus V T n

V naught by 2 plus V naught into 1 minus dV out by V in half, right equals V in minus V DD minus V TP into r.

So, can you simplify this and tell me what you get for? Of course, here V in is nothing, but V IH V out is nothing, but V OL can you get me the expressions equal to dV naught.

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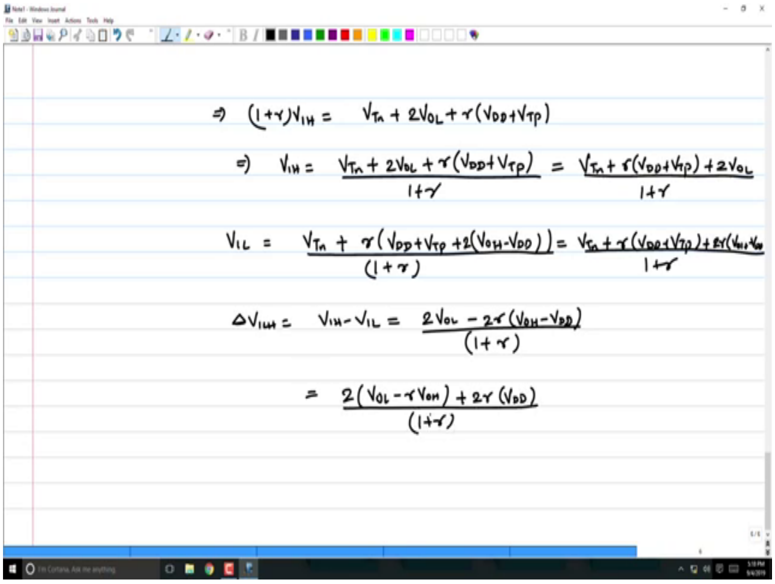

So, this is not. So, in this 3 by 2 V naught plus 2 V OL plus r into V IH is V Tn plus 2 V OL plus r into V D plus V TP by you get this yeah good. So, I just derived the whole thing, so that you are you get used to this kind of solving of you know these equations. So, now let us compare the earlier expression that we also had right what was our V? V IL is V T n plus r into this. So, can I copy this?

Yeah. So, V IL is this. So, can you compare these two expressions and see what do you get here. I am going to write this as V Tn plus r into V DD plus V TP plus 2 V OL by 1 plus r and this I am going to write as V T n plus r into V DD plus V TP plus 2 r correct V OH minus V DD by 1 plus r. So, what is this region between V IL and V IH? How thin is this region right?

Ideally you would want it to be 0. You know 0 indeterminate region right, you want the inverter characteristic to fall sharply like this, but inevitably there is a small region. So, what is this delta V IH right which I am going to call it as V IH minus V IL. Clearly you can see that this V Tn and r into V DD plus V TP is sort of gone, right. So, you basically have simply V IH minus V IL, right; so, 2 V OL minus 2 r into V OH minus V DD by 1 plus r, right.

So, I can write this as 2 into V OL minus r into V OH plus 2 r l to V DD by 1 plus r. Actually, that is not necessary, right. We do not need this. No this simplification is not necessary ok. So, what is V OL? It is a number which is very close to 0, V OH number which is very close to V DD, right. So, V OH minus V DD is a very very small negative number, V OL is a very very small positive number. So, if you see this difference it is actually extremely small number.

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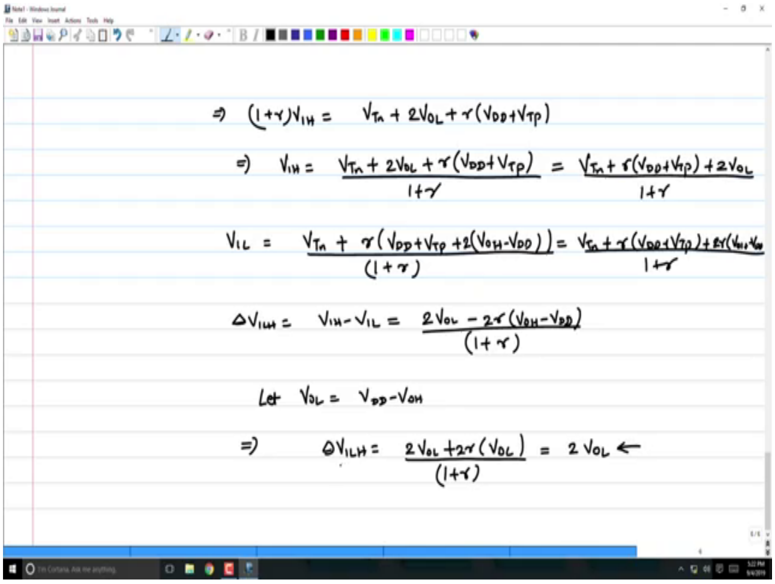

So, for example you could assume let right V OL equals V OH minus V DD or V DD minus V OH for symmetry, right. It is on either side. It is going by the same amount is what we are saying. So, if that is the case, then what does that thing simplify to V IH is 2 V OL minus plus 2 r into V OL, sorry right. What is it simplify to 1 plus r comes out and you have twice V OL.

So, what are we saying for a long channel inverter, this region in which this the input is an indeterminate input is actually simply twice V OL. It is such a small region it is almost like up to V DD by 2, everything is logic low after V DD by to everything is logic high, right. So, that is the reason I wanted to go through this long channel inversion inverted derivation because it allows me to show you exactly that this is true, clear.

So, that region in which because the slope is minus infinity at V in equal to V out equal to VM that region also has to be very, very, very small for a long channel inverter, clear. Of course, here I am assuming that V OL equal to V DD minus V OH it is the fair thing actually because V OH is supposed to be V DD, V OL is supposed to be ground ideally.

Any questions here? So, two things one short channel transistor, the equations are very complex because just think about this now in each of these terms if I add a 1 plus lambda V naught, just think about how you will do this differentiation and get the accurate answer. It is not possible. It is not even tractable and it is not even useful. The end of the day I do not even get a result like this where I can intuitively understand something from it, right.

It just makes it very complex and therefore, we resort to that approximation where we extrapolate that line act V in equal to V out equal to VM with that same slope. And then, extrapolate those points as V IH and V IL right, but for the long channel device it is possible to derive these expressions very accurately clear. And, if you make the assumption that V OL is equal to 0 and V OH is V DD, then you will find then this region delta V IH is basically 0.

So, that is also not true it. So, somewhere it is because V OH and V OL are not exactly V DD and ground respectively. That is when this small indeterminate region actually comes into picture, ok. Here we have made no approximations whatsoever. All expressions are accurate here.