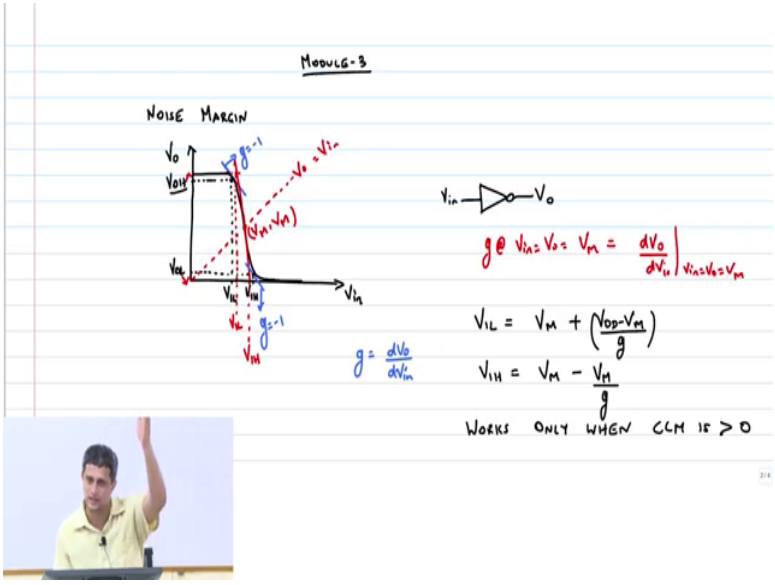
Digital IC Design
Prof. Janakiraman Viraraghavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 21
Noise Margin Analysis-3

(Refer Slide Time: 00:14)



So, yesterday we started doing analysis on Noise Margin. We did not complete it, but we derived expressions for the V IL and V IH, ok. What is V IL and V IH, we look at it now. V out versus V in, this is my transfer characteristics V in V out right. So, we said that the point at which the slope right becomes minus 1 is a point of interest because to the left of it on the lower side, the gain is less than 1 which means any noise will get killed, will get attenuated and the output will be robust and stable at that particular value, right.

So, therefore the point where the gain becomes minus 1 is of importance g equal to minus 1, right and what is g? d V naught by d B in the gain, right. So, we need to identify these points. So, the point where this is V IL V IH corresponding y axis value is V OH for V IL because this is an inverter and V OL, right.

So, we wanted to find these points in a short channel transistor because it has channel like modulation. All that the expression is quite complex. Therefore, we made an approximation and said that we will sign the point when V in equal V out equal to V M the trip point, right. V in V out equal to V in equal to line and this point is V M, V M.

Then we said that we will take the slope out here and just extrapolate with that slope right and see where it intersects my V OH. So, the first point is V OH is actually nearly V DD and V OL is nearly ground. This is true whether it is a real transistor or the ideal case or the real case, it does not matter right.

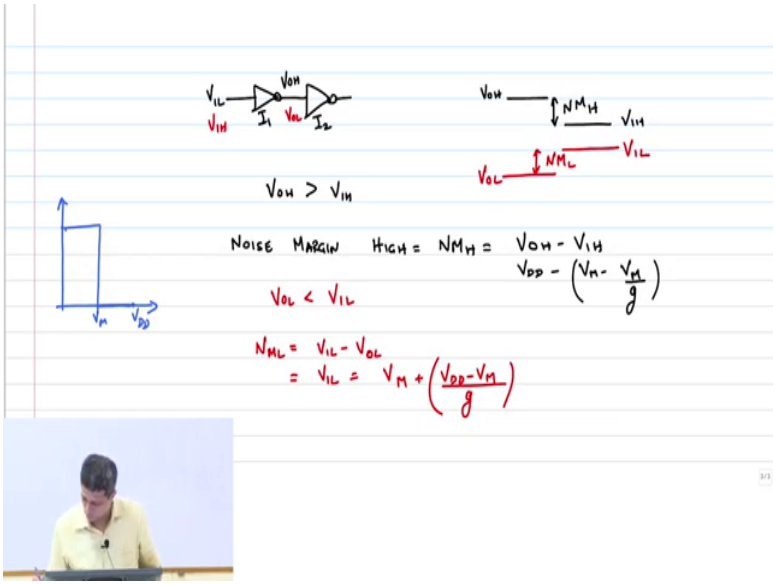
So, V OH if you are going to approximate is V DD is not a big problem. So, we can take the intersection and this point we said we would call as V IL. Similarly this particular point we would call as V IH. Of course there will be slight error, but it is a very reasonable error within 5 percent or so. We get the answer right.

This is the basic idea because the expressions are complex, ok. You can always try to derive it, but it is just going to get very cumbersome, ok. So, then we said that you can calculate the gain at, so you calculate the gain at V in equal to V out equal to V M, right. How do you do this? You have to basically do d V out by d V in right at V in equal to V out equal to V M. Of course, both n mos and p mos are going to be assumed to be in velocity saturation region in this particular at this particular point V M. We already did this calculation in earlier right.

Using this we were able to calculate the levels V IL and V IH. So, what was V IL? It was V M, right. What was that plus term can you remind me huh? V M plus V M by g is it V IL V DD minus V M by g and V IH minus V M by g z yeah make sense because g is a negative gain. Minus minus will become plus. So, V IH is to the right of V M and V IL will be to the

left of right. So, this is the expression that we got now. Still this does not tell us anything about the noise margin. That is what our discussion started with.

(Refer Slide Time: 05:30)



So, let us now see what these values what is V IL. It is the threshold voltage, right. Not to be confused with transistor threshold, it is that particular threshold voltage below which everything will be treated as a logic 0. V IH is the threshold voltage above which everything will be treated as a logic one, ok. That is the most important thing. So, now let us assume in the limiting case that I am applying V IL here, what will be the output of this inverter?

No no go back to this curve. Ah if the input is V IL, then the corresponding output is V OH by definition because that is the y axis value, right. Therefore, this has to be V OH right. Now I want this output to be recognized as a logic I. What is the condition on the second inverter?

This is I 1 I 2. What is the condition on the second inverter? For this V OH to be recognized this logic I, correct.

V OH should be greater than V IH which means that if there is a noise plus up to this magnitude, the difference of V OH and V IH, it should be fine. My V OH is here right. My V OH is somewhere here; my V IH is somewhere here, right. This is V OH, this is V IH. V OH is above V IH as long as that is done taken care of. It is a logic high, no problem. That means, I have this much room for noise do actually you know cause this voltage to come down. That much I can tolerate.

Naturally this is called the Noise Margin of the High Side. So, noise margin high is N MH is V OH minus V IH. Now, if this is V IH, what will the output of the inverter be? I 1 V O, V O l. What is the condition for V OL to be recognized as a logic low for on inverter 2 V OL? It should be less than V IL, correct. So, this is my V IL and somewhere here is my V OL. Therefore, on the lower side I can tolerate a positive noise pulse as long as it is below V IL I am fine. So, this much is my Noise Margin on the Low Side.

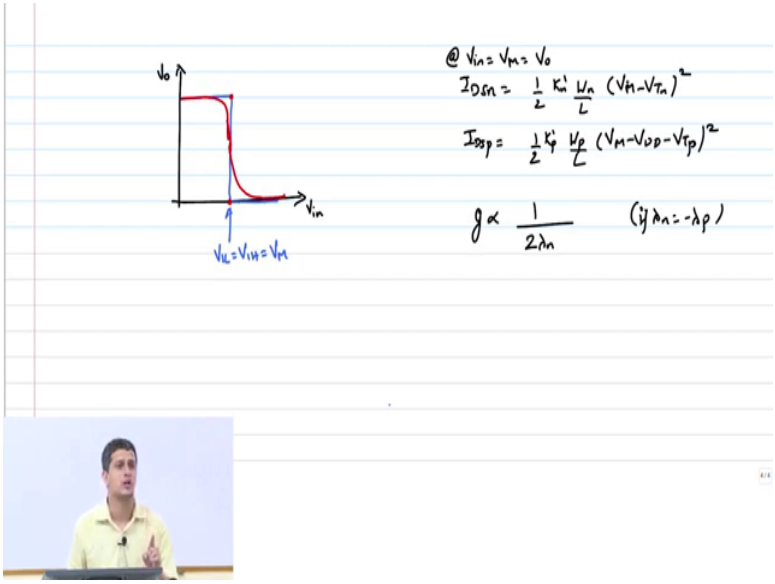
So, N ML is V IL minus V OL, ok. So, now can you substitute these values? Of course, V OH is very close to V DD, correct. So, we can make the substitution that V OH is merely V DD. So, this is in black color right. So, this is V DD minus V IH. What does that value V M minus V M by g? Right. Similarly what is Noise Margin Low V? V OL is what yeah 0. So, this is just V IL. So, this is what we derived again V M plus V DD minus V M by g V D, sorry V M plus V DD minus V M by g.

Now, sanity check ideal inverter what is g yeah infinity? What should the Noise Margin be on the High Side? V DD minus V M right because for the ideal inverter, for the ideal inverter the V TC is going to look like this right. It starts appropriately V M, it will fall, this is V DD, V M. The noise margin on the high side is going to be V DD minus V M, on the low side it is just going to be V M as long as I have that much room and that is exactly what we get when we substitute g equal to infinity.

So, the expressions we have got are in alignment with our intuition as well ok. Any questions here? Yeah because they are actually very very close to V DD ground. I mean you can calculate the exact value, but then we really close that is true your approximation method does that, but even otherwise V OH and V OL will be very close. You do a simulation and see for example, find out where the slope goes to minus 1 and see what V IL and V OL are? V OL and V OH should be very very close to infinity, right. For reasonably high V DD, this will be true yeah.

So, now let me see how far this approximation that we have made how far can I take it? Can I apply the same logic to a long channel device? Think about the approximation that we did. Tell me if I can make this approximation for a long channel device? How would this approximation look for a long challenge device?

(Refer Slide Time: 12:55)



First of all how will the V d V t of this long channel device look like rather what will be the slope at the trip point huh? What is the slope g at the trip point? More than? No no I need an I need a number huh. So, we derived this yesterday. Suppose it was a long channel device right at V N equal to V M equal to V out I D s n is what half of K n prime W n by L into V M minus V T n the whole square. I D s p is what half of K p prime W p by L. Both are in saturation V M minus V DD minus V T n V T p whole square.

Do any of these currents depend on V out? No. So, what will it be the slope? There is no lambda. That is whole point, right. So, we derived an expression for the gain right. If you remember yesterday and we said it is 1 by 2 lambda n assuming that lambda n equal to minus lambda p.

If now lambda n is 0 what happens to the gain goes to minus infinity, right. Basically all it to goes to plus infinity. Why do you think minus infinity there is a minus yeah right? Anyway it basically becomes a vertical line and that point this does not mean that the voltage characteristics of a long channel device inverter is an ideal case.

It does not mean that long channel V D c is like this. That is not true. What actually happens is this guy is like this. It comes now at this V in equal to V out, ok. Here it will be a straight vertical line, your slope will be infinity ok, then this again go out like that.

So, the conclusion is if I do this same analysis and approximation for the long channel device, I will get this blue curve and my V IH and V IL will both collapse to V M. If I make the approximation right, then here yeah V IL equal to V IH equal to V M. Clearly this is not true right. So, the approximation that we did work is only for a short challenge device when there is non-zero channel length modulation.

That is the limitation of the approximation that we have made earlier. So, this guy here works only when CLM is greater than 0. This is the limitation that you should understand when CLM is there. It is a reasonable approximation because you get a slope at that point you extrapolate and it works reasonably well, but you cannot do this for a long channel device, ok.

So, now question is how do I evaluate this noise margins for a long channel inverter. Luckily it turns out the expressions for current are themselves not so complex as it is for a short channel device and therefore, we can do it from first principles, ok.