**Digital IC Design**
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**Lecture – 20**
**Noise Margin Analysis -2**

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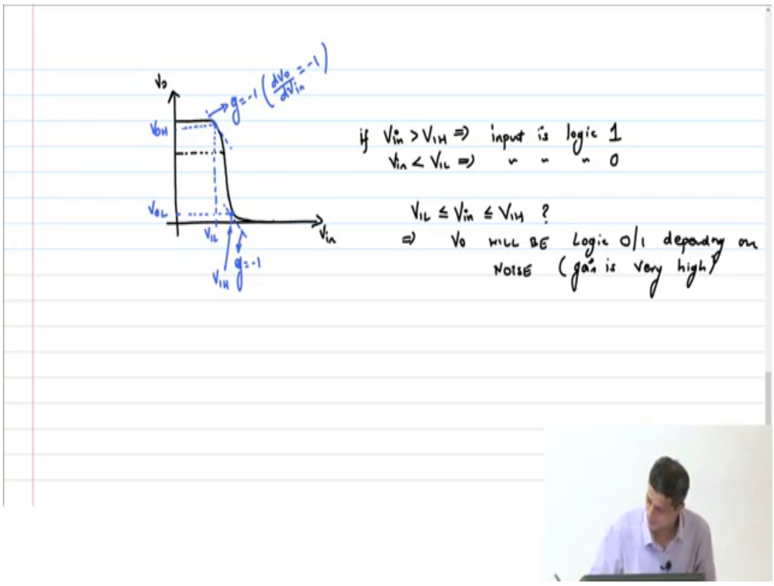


So, now our aim is to find out these two points V IL and V IH and then the corresponding V OL and V OH. So, how do I go about doing that? Suppose, I want to find these two points of intersection; what should I do? What region of operation is my N MOS and P MOS? Let us take V O; V IL, N MOS will be in? Saturation, P MOS in? Linear. Now, you write these equation out; then you have to differentiate it and equate the gain to minus 1; that is what we are trying to doing here right. We are finding the point at which the gain is minus 1 that is dV out by dV in equal to minus 1.

Now, the issue is that is a quadratic equation and you know tough layer; it becomes very cumbersome to derive it; it is possible to do it with some approximation. So, I would recommend you go back and just try it once ok, it is very much possible, but you have to just do it very carefully. Instead of doing all these cumbersome thing, there is another way where we can with some approximation obtain this expression pretty easily ok; I will tell you what that approximation is right now.

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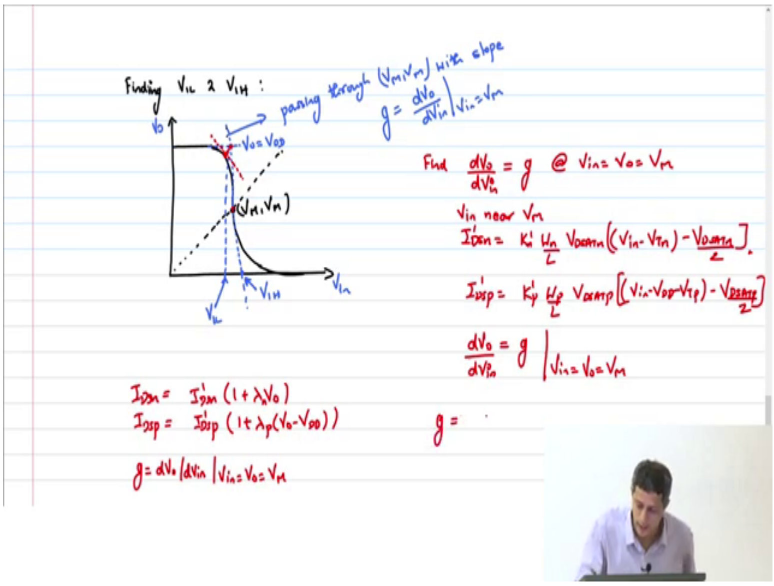


So, finding V IL and V IH ok; let me draw a slightly exaggerated ok. The gain this is my V in equal to V out line and this is my V M comma V M. Now, if I find this straight line at this point at V M comma V M and I extrapolated dots ok; this is the line passing through V M comma V M and the gain with slope; with slope g which is equal to dV out by dV in; at V in equal to V M.

I am taking the line at V in equal to V out finding the slope there and extrapolating the same thing the same straight line with that slope ok. This will come and now meet by x V out equal to V DD line V out; this is V in this is V out equal to V DD; this I am defining as V IL ok.

Similarly, on the other end this comes here, remember I have drawn this little exaggerated just to find out. So, if you look at this I am calling this as V IL and this as V IH. Actually, that point is going to be somewhere here because the line equal to slope of minus 1 will happens somewhere here. You have this much error; no doubt about it, but that error actually very small ok. It is an approximation, but the error happens to be very small and therefore, it is possible to use this approximation quite well.

Any questions on the approximation? We are not doing it with the accurate expression because that is a quadratic equation become very complex; no, this is somebody has just found out and told you that it works pretty well; so we are just using that that is all yeah. But it is like within like 5 percent apparently of the actual value right. So, now, what do I need to do? I have to find dV out by dV in right; this is my gain at V in equal to V out equal to V M ok. So, now what do I do? I have to go back and do the same story I DSN equal to IDSP right.

So, I am going to say that the current I DSN is let me not; let me use a short channel device for now right ah. So, this be K n prime Wn by L into VDSATn into V in minus V Tn minus VDSATn by 2 right. This is V in near V M; IDSP is what? K p prime W p by L VDSATp into V in minus; no, this will not V in; this is V in minus V DD minus V Tp minus VDSATp by 2 ok. I want to equate these two and then find dV naught by dV in. What is the problem in this? I equate these two currents by doing I DSN equal to minus IDSP, then I have to find dV naught by dV in and that is going to be minus 1. I mean that is not minus 1; I am sorry that is basically the gain that I want.

This is the gain that I want; gain at V in equal to V out equal to V M, correct? I am trying to find that slope of the V Tc at V in equal to V out equal to V M; that is what I am trying to do. What is the problem in this equation? Can you find the slope here? Look at the current equation, how do you do dV out by dV in here? Yeah, what is the issue? There is no V out; there is no V out in this right.

And therefore, if you do not consider the channel length modulation; you cannot get this exact expression ok. So, we will come to what happens then there is no channel length modulation later ok. So, therefore, what I am going to do is; I am going to; I am going to say that I DSN is whatever this expression I DSN prime into 1 plus lambda V naught; IDSP equals IDSP prime into 1 plus lambda no; lambda n lambda p; V out minus V DD, agree with me here?

So, now you can go head and find dV out by dV in; the gain is at this point, at V in equal to V out equals V M ok. So, I am not going spend my time deriving that here because algebra is it is; it is easy, but it just cumbersome it turns out that you can derive it to be exactly like this.

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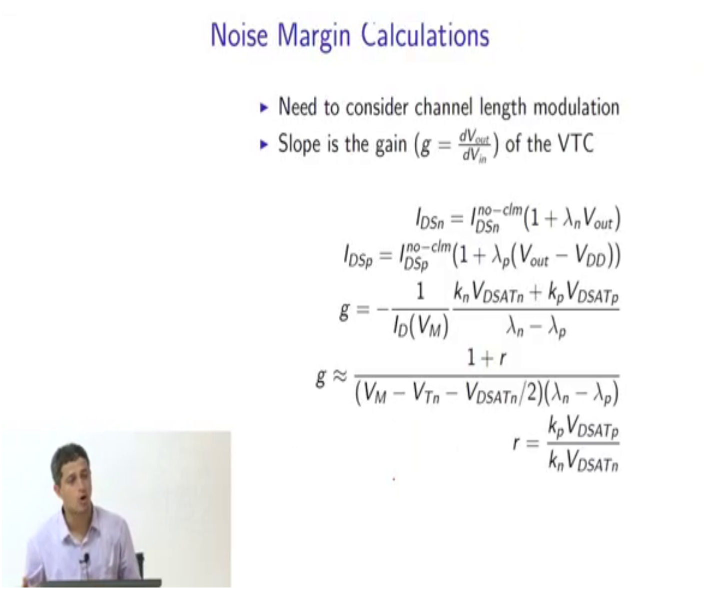

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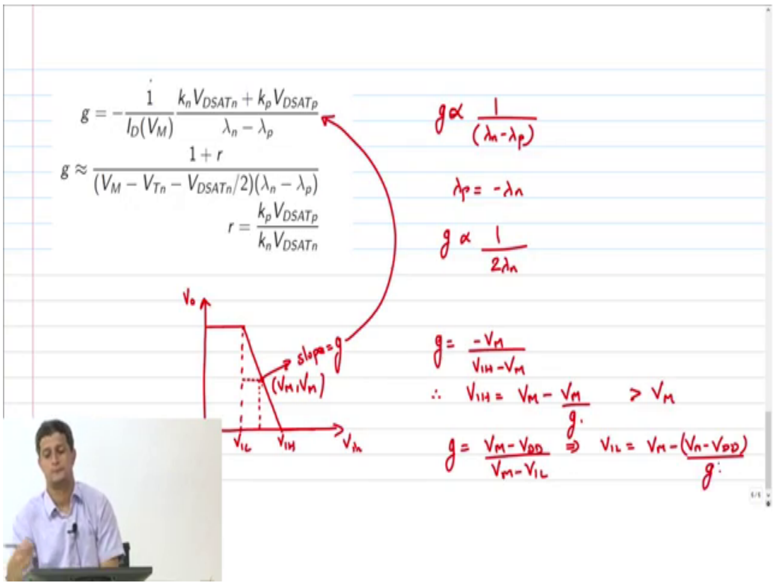


The gain ok; I will just write that here it turns out the gain gives maybe I can use the turns out the gain is as follows ok. You can derive this later; it is there in the tutorial for you to derive this expression ok; I tried it out, it comes out correctly you just have to do it carefully; I am just not wasting my class time for this. So, the gain is if you look at it; is you know basically proportional to 1 by lambda n minus lambda p. So, if the technology is symmetric and all P MOS parameters are negative of N MOS parameters; what will be the gain?

That is what you should be very careful about; lambda p is also a negative number. So, this does not mean that if lambda n and lambda p are minus of each other. So, if lambda p is minus lambda n; then gain is actually proportional to 1 by 2 lambda n. So, the fact that the gain is very high comes from the point that channel length modulation parameter itself is very small. And therefore, the gain will be very high it not because lambda n minus lambda p is almost 0, clear ok.

So, with this expression can you now tell me what V IH and V IL should be ok? It is let us just go back and redraw this thing V out; V in. So, what we have said is now the approximated VTC is going to be like this; it is a straight line. This is V IL; this is V IH, this line has a slope of g; equal to g which is given by this expression ok. And the line also passes through V M comma V M ok. Now, it is just a question of slope; can you find out V IH and V IL from this? Please do it.

Do you get this? Right g is positive or negative? Negative slope; the large negative number; so V M minus; so the point is V IH should be to the right of V M correct. It should be V M plus some number; does that happen? Yeah V M minus V M by g; g is a negative number. So, that actually becomes a greater than V M. So, I think we are right ok; what about V IL? V IL equals V M minus V DD by g yeah.

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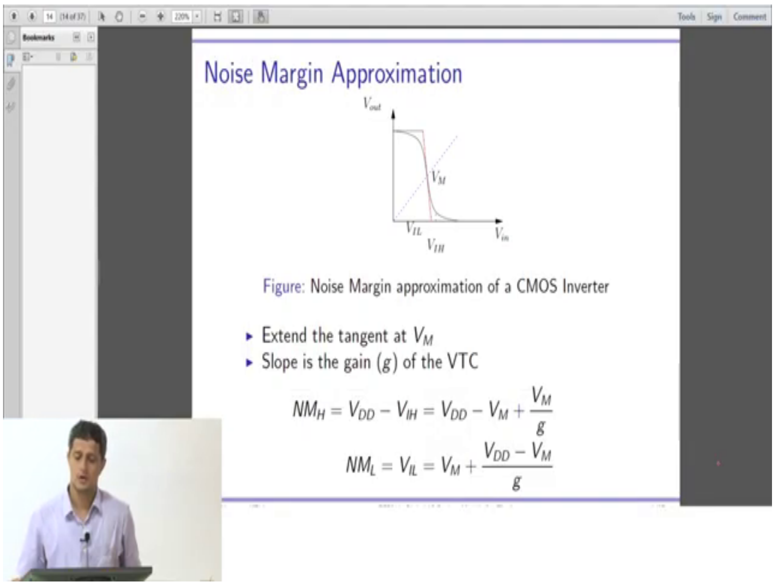


V M into V M plus V DD minus V M by g and we will; we will come back to that. So, are you able to get this? First point, suppose g were infinity; what will happen to V IL and V IH? Both of them will just collapse to V M; that is the ideal case.

If the gain is such a sharp transition right where V out and the VTC becomes the straight line at the trip point; then both V IL and V im will simply collapse and come down to V M. So, anything greater than V M is logic high; anything less than V M is logic low ok.

So, with this we will actually proceed in the next class to do the noise margin analysis. Now, we want to figure out if my input is at V IL; then how much noise can it tolerate before it goes into some determinate region or the output will switch? So, how much noise can we tolerate for both logic level is what we are going to look at in the next class and that is the noise margin that I spoke about in the beginning of the class ok.