

Digital IC Design
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Lecture – 02
PN Junction

So, then let us jump straight into the first module and do not worry I will be teaching of the tablet here ok. I am not going to teach of the slides like I did now because it is a reintroduction, I just went a little quick there. So, the transistor is basically the fundamental building block of all these circuits right. And, as a designer you need to understand what the transistor does at least at some level of abstraction right.

So, the transistor can be studied as a separate course in a device you know semiconductor devices course. We are not go into go into that level of detail, I need a certain abstraction that will help me make my decisions in digital circuit design very well, with respect to that I will teach what is necessary about the transistor right. How do you; how do you get the expression for the current? What effects the current? What are the model parameters that one a designer should know about, you know these kind of questions we will answer in this module.

(Refer Slide Time: 01:25)

Learning Objectives

- ▶ Explain short channel effects(SCE) like Drain Induced Barrier Lowering, Gate Induced Drain Leakage, Sub-threshold leakage, Channel length modulation
- ▶ Derive the equation for ON current of a CMOS transistor with first order SCE
- ▶ Estimate various capacitance values for a transistor
- ▶ Estimate the equivalent ON resistance of a transistor




What are the learning objectives? Ok. Again once you are done with this module, you should be able to explain shorts Short Channel Effects, it is called SCE right. So, when I bring the channel may when I when I bring the diffusions very close right, the channel becomes very small that introduces some non-idealities. So, that is something you should be able to explain like brain induced barrier lowering, gate induced drain leakage, sub threshold leakage, channel length modulation and so on right.

Then you should be able to derive the equation for the on current of a CMOS transistor with first order short channel effects ok, we will do all of these. Then the most important thing is you should be able to estimate various capacitance and resistance components of a transistor because ultimately going forward I want to measure delay. And, not surprisingly delay of a

transistor is just given by r into c ; I need to be able to estimate these components and figure out how the transistor behaves with respect to resistance and capacitance.

(Refer Slide Time: 02:37)



Outline

- ▶ Silicon and Doping
- ▶ P-N Junction
- ▶ CMOS Transistor
 - ▶ Threshold Voltage
 - ▶ ON Current (I_{ON})
 - ▶ Channel length modulation
 - ▶ Velocity saturation
 - ▶ Sub-threshold leakage
 - ▶ Drain Induced Barrier Leakage
 - ▶ Gate Induced Drain leakage
 - ▶ (Reverse) Short Channel Effect
 - ▶ Other leakage mechanisms
 - ▶ Capacitance
 - ▶ Resistance

Janakiraman, IITM EES511: Digital IC Design, Module 1 - The Transistor 3/43

So, the outline this I am going to just briefly tell you about silicon and doping and the P-N junction only with respect to what we need for the CMOS transistor. I am not going to go in to deriving the current equation for a P-N junction and all that is for a different course. Very quickly I will jump into the CMOS transistor and define what threshold voltage is, how what the on current is, we will derive what the on current is.

Channel length modulation, velocity saturations, sub threshold leakage you know a host of other short channel effects. So, what you see here right basically from here, channel length modulation on till reverse short channel effect. Those are all the effect of bringing the diffusions very close by. So, I will do all of that and some leakage mechanisms also right, that

a digital designer should be worried about and then we will do the capacitance and resistance estimation ok.

(Refer Slide Time: 02:39)

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MODULE - 1

THE TRANSISTOR

Diagram of a silicon atom (Si) with four valence electrons. One electron is shown as a "free e^- " after "DOPING".

Si density: $10^{23}/\text{cm}^3$

@ Room Temp (27°C) $= n_i = p_i = 10^{10}/\text{cm}^3$

$n = N_D = \text{Doping Conc} \sim 10^{15}/\text{cm}^3$

So, with that let us just quickly jump into the transistor and of course, the semiconductor that is used is silicon. Why is silicon? Because it has good mobility, but it also has a very fantastic thing called a silicon dioxide which can serve as the oxide, insulator and forming this silicon dioxide is very easy. So, the interface is nothing, you just oxidize the silicon you get a good silicon dioxide there. So, that makes the transistor manufacturing relatively much easier compared to if you try to do it with other semiconductors right.

So, what is silicon? Basically, it has 4 valence electrons right which means that in a lattice it is going to sit like this right. And, you have covalent bonds which are connected like this ok. And, as I increase the temperature from 0 Kelvin onwards some electrons can break free from

this bond and be made available for conduction. This can result in a free electron ok. What is now the quickly the order of magnitude again? The silicon density is what? Yeah. 10^{22} per centimeter cube ok, in 1 cm cube you have 10^{22} atoms.

Now, at room temperature right which is what about 27 Kelvin 27 degree centigrade 300 Kelvin. The number of free electrons that are available is basically called n_i . Why? Because, its intrinsic silicon it has nothing else, number of free electrons is equal to number of holes. Absence of an electron can be treated as a hole for this course number of electrons; obviously, is equal to number of holes because I have to maintain charge balance right. And, that is what order of magnitude again I do not want 10^{10} per centimeter cube ok. Clearly, this number is not high enough for me to achieve the conduction that I need right.

So, therefore, what you do is you go ahead and replace this silicon atom by let us say phosphorous ok. Phosphorous now has how many valence electrons? 5. So therefore, the phosphorous has 4 electrons that it forms the covalent bond with right. And, this electron can easily be released above 0 Kelvin, not at 0 Kelvin. If we increase the temperature much easier it gets released and is available for conduction ok. This act of replacing the silicon atom in the lattice with another atom like phosphorous or boron which is trivalent is called doping ok. This process is called doping.

Now, once this free electron is released from phosphorous what happens to the charge of that phosphorous atom? Yeah. So, this will become positive right, the phosphorous atom the electron is now free available for conduction, the phosphorous atom is a positive charge. But, it is immobile because it is in the lattice its stuck in the lattice, it does not contribute to any current or current flow in general. So, now the question is at room temperature how many such free electrons will I have? Ok. It turns out that if your doping is high enough then at room temperature all the atoms are ionized, phosphorous atoms get ionized.

And therefore, the number of electrons at room temperature is just the doping concentration right and this is the phosphorous atom is giving an electron. So, it is called a donor right and

the concentration of phosphorous is N_D , the doping concentration right. This is doping concentration, typically it is about 10^{15} per centimeter cube ok.

Note it is that it is 5 orders of magnitude higher than the intrinsic silicon free electron concentration. So, there that is why I am not worried about what happens to this free electrons that come from some of the silicon atoms that also happens, but that number is so, small I can neglect it right. So, effectively I have like number of free electrons at room temperature is 10^{15} per centimeter cube right. Now, how many holes are there in this doped semiconductor?

(Refer Slide Time: 09:19)

LAW OF MASS ACTION:

$$np = n_i^2$$

$$n = N_D$$

$$p = \frac{n_i^2}{N_D}$$
$$\frac{n_1}{n_L} = e^{\psi_{12}/(kT/q)}$$

$$\frac{kT}{q} @ RT = 25 \text{ mV}$$

So, it turns out that there is a law of mass action that determines that; law of law of mass action ok. What is this say? It says that the intrinsic the concentration of electrons in to holes

is a constant and that is basically n_i^2 ok. So, therefore, if n equal to N_D what is p ? n_i^2 squared by N_D ok.

Now, there is also an other equation called the Maxwell-Boltzmann equation which just tells you that if I have two points in a semiconductor ok. This is my let us say silicon here, some reason I have; I have caused a charge imbalance not an it does not violate conservation of charge. But, there is more concentration of electrons here n_1 and n_2 and let us say n_1 and n_2 are different. Then it turns out that there will be a potential difference between these two points which is basically $\psi_1 - \psi_2$.

And, the relation is given by n_1 by n_2 is e power $\psi_1 - \psi_2$ by kT by q ; k is the Boltzmann constant, T is the temperature, q is the charge of the electron ok. And, this is important to know kT by q at room temperature is approximately 25 millivolt.

Hey you can work it out, just substitute T equal to 300 Kelvin; work out the constants and you will get this ok. So, you should know this number 25 millivolt is an important number for a digital designer right.

(Refer Slide Time: 11:43)

Device Physics Abstraction

1. Law of Mass Action - Product of concentrations remains constant

$$np = n_i^2$$

Where

- ▶ n/p = Electron/ hole concentration after doping
- ▶ n_i = Intrinsic electron/ hole concentration

2. Maxwell Boltzmann Equation -

$$\frac{n_1}{n_2} = e^{\frac{\psi_{12}}{kT/q}}$$

Where

- ▶ kT/q - Thermal voltage = 26mV @ 300K
- ▶ n_1, n_2 - Charge concentration across a potential ψ_{12}



So, this is basically called the it is called Boltzmann yeah, it is called the Maxwell-Boltzmann equation, not just the Boltzmann equation ok. Now, what happens? So, what I have done is with this equation here I have completely bypassed this theory of Fermi levels and other things. I abstracted out all that I need for my for this course right and in fact, you can even go ahead and do lot of device derivations using this just this assumption ok. The book called (Refer Time: 12:15) actually does it like this, MOS the MOS transistor it works exactly like this. So, this abstraction is very very useful not just for digital design engineers, it is also good for device guys.

(Refer Slide Time: 12:29)

Build in potential = V_{bi}

N_D n-type Donant = P

N_A p-type

Area = A

SPACE CHARGE REGION (Depletion region)

W_n W_p

$n_i = e^{\frac{qV_{bi}}{kT}}$

$n_1 = N_D$

$p_1 = N_A$

$\Rightarrow n_2 = \frac{n_i}{N_A}$

$qN_DW_nA = qN_APW_pA$

$\Rightarrow W_nN_D = W_pN_A$

if $N_D \gg N_A$

$\Rightarrow W_p \gg W_n$

$\therefore \frac{N_DN_A}{n_i^2} = e^{\frac{qV_{bi}}{kT}}$

$\therefore V_{bi} = \frac{kT}{q} \ln \left(\frac{N_AN_D}{n_i^2} \right)$

Now, what do I do? I cannot do much with just a n type semi conduction right. So, that is the donor semiconductor is called n type semiconductor, because I have more electrons than holes right. I can take two semiconductor blocks which are doped differently and connect them together like this ok. So, the let us say this is N D this is N A. So, instead of phosphorous if I put boron, boron is trivalent; there is going to be one electron absent and therefore, it is like a hole that is available ok, that is the abstraction that we need. So, I have an n type semiconductor here, I have a p type semiconductor here right.

So, I can even may be say that dopant equals phosphorus and here it is boron. So, now what happens? You basically have excess electrons on the n side and excess of holes on the p side. So therefore, they will now start diffusing right. So, the free electron from this side will go here, the free hole from this side will come here.

Remember that once the electron comes this side what happens to the atom from which that electron was released? It is a positive charge. So, what happens is effectively on the n side you will have immobile positive charges like this. And, on the p side you will have immobile negative charges that are formed ok.

So, ultimately there will be a region like this here and a region here, this is called space charge region. Space charge region basically it says that there is no free electron or hole that is available for conduction there because moment you have a positive charge on the n side and a negative charge, you will have an electric field coming from the n to p right; you have an electric field here. So, if any free electron enters that region, it will be driven the other way. If a hole enters it will be driven in the direction of the field to the other side. So, this is basically devoid of any charges and you will have what is known as a built in potential across this region space charge region ok.

So, now let us you know calculate how far this has to go on both sides. Let us say that this went up to a distance of W_n and this went up to a distance of W_p ok. On the p side the distance of the depletion region it is also called a depletion region by the way, this is also called depletion region ok. How do I relate W_n and W_p ? Yeah, basically charge neutrality right. So, therefore, if the concentration of electrons right on this side is N_D ; I mean concentration of dopant atoms is N_D right, then the number of positive charges is what? q times N_D into W_n into the area.

Let us say the cross section is like this and this is the area A right, then into A is the total volume W_n into A is the total volume, this is the total charge, this has to be q times W_p into N_A into area. So, W_n into N_D is W_p into N_A . So, what is this basically say? It says that W_n into n is a constant. So, the main takeaway for us here is if N_D is much much greater than N_A let us say, it implies that W_p will be much much greater than W_n correct clear. So, now we have a relation between W_p and W_n , but what about W_p plus W_n ? How far will that go?

So, that will go only as far as I am now what do I have? I have two in a; in a semiconductor I have two points. Point 1 is here, this is point 2; there is an electron concentration at point 1, there is an electron concentration which is different at point 2 right. And therefore, they have to be related by the Maxwell-Boltzmann relation right. So, they which basically says n_1 by n_2 is e power q times built in potential V_{bi} by kT right, this let me call it V_{bi} . Now, what is the electron concentration at point 1? n yeah; so, n_1 equal to N_D . What is the whole concentration at point 2? Yeah.

So, the p_2 is N_A which means n_2 is how much? Yeah, n_i square by N_A therefore, I can now divide this as N_D by n_i square into N_A equals e power q V_{bi} by kT . Therefore, built in potential is kT by q \ln of $N_A N_D$ by n_i square ok. This is all we need from the semiconductor device physics for us to go ahead and understand all of MOS transistors for digital design. At least first order short channel effects all that we can handle with this ok. So, I will stop here, we will meet again tomorrow at 9 am.

Thank you.