Digital IC Design
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Lecture – 19
Noise Margin Analysis - 1

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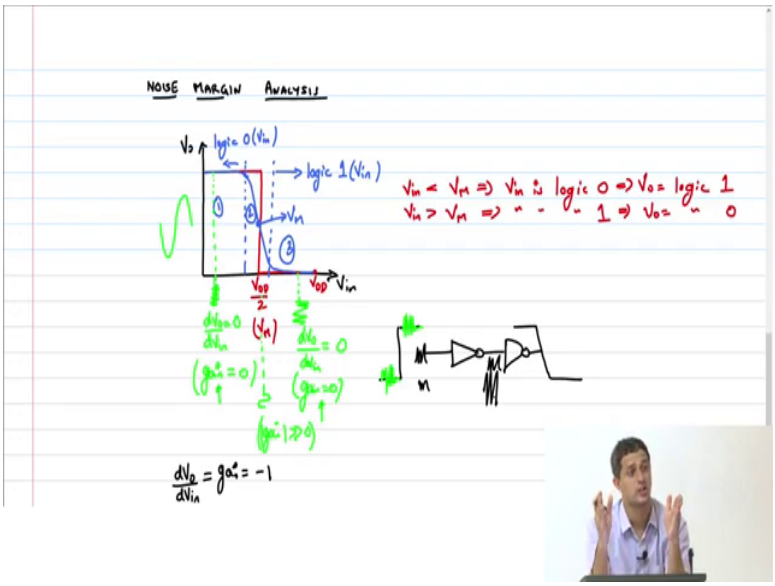

So, with that let us now go on to the Noise Margin Analysis. So, the ideal voltage transfer characteristic was like this right, very sharp thing at around V D D by 2; not necessary I can actually move that little bit here there depending on my threshold that I need right. The trip point would be at V D D by 2, ok. So, this is V D D. So, it is very clear that V in if it is less than let me call this as the trip point V M; V in less than V M implies V in is logic 0, implies V out is logic 1. If V in is greater than V M right implies V in is logic 1 and this implies V out is logic 0; no problem here in the ideal case.

Now I want to see how does this analysis work for the real inverter because there is a deviation from this ideality. So, if you consider the V T C of the real inverter; it could be slightly exaggerated I am showing, but this is my V M, right. Clearly this definition does not hold here; if V in is greater than V M, it does not mean that it is a logic 1.

Neither is it true is that if V in is less than V M in the real inverter that the input can be treated as a logic 0, ok. So, there is some region before V M, somewhere I do not know where this is; we are going to pin it down in this discussion today, right. Anything to the right of this line can be treated as logic 1 for input for the V in; anything to the left of this line can be treated as logic 0 for V in, ok. And of course, this is V out versus V in, ok. So, now, let us go back to the, I am just going to draw the inverter like with a schematic symbol like this, fine.

So, I have an input like this, the output will also go something like this right and maybe if I have to draw it there is a delay and all that, so it could be like this, fine. So, in steady state my input is fixed at either 0 or logic 1, ok. In reality, in a chip it is not true that the signal will be so idea, ok. So, therefore, I am going to constantly have some noise perturbation around this, ok.

And a robust inverter is one which is immune to this noise in steady state; of course, in the transient region that is a different case. You know anyway there is a transition some noise here there we cannot do, we cannot do too much there; but in steady state any noise the inverter must be immune to it, which means that the noise must get killed ok. So, what does it mean to say that the noise must get killed?

So, let us look at three regions ok; region 1, 2 and 3. To the right of some point I am going to analyze what happens if there is noise ok. So, this will determine where our boundary should be, where this region 1 to region 2 transition happen and 2 to 3 transition will happen. Suppose there is noise now, if my input is very close to 0 here.

Let us say I have a noise like this, what will happen to this noise at the output? Why? Sorry?

Student: (Refer Slide Time: 05:46).

What does that statement mean? More precisely, more mathematically; what does that statement; you are right whatever you do we are getting the same output. What does that mean again? Mathematically what does it mean? V out; so delta V out by delta V in is is zero; that means, the derivative is zero which means the gain at that point is basically zero, right. So, if you look at this point here d V out by d V in is 0, right; which means that the gain is 0. So, what it means is that; if there is noise the noise is getting killed, because it does not getting amplified, in fact it is getting attenuated and it is all gone. So, the noise fluctuation at the input cannot percolate to the output, right.

Similarly in region 3 I can do the same analysis; I have a noise perturbation, very clearly here also d V out by d V in is 0. Again the gain is, ok. Now what happens if I do the same thing in region 2, here? I am going to do the same thing here, I will pull this thing here, I have a noise, ok. Or let me just maybe make it like a sinusoid; what will happen to the output here around V M? Sorry?

Student: Amplified.

Amplified, because the gain in this region is extremely high; it is actually it should be a vertical line. Gain should be infinity there, but since there is a deviation it is slightly this thing it has a very large gain in this region; which means the output will actually get inverted and it will appear like this, right. But of course, it is not like you know it can be a sinusoidal like this, because as I move away the gain is changing and all that. So, effectively it will be a distorted you know sine wave, right.

So, the point is as I am moving from left to right, my gain is going through some changes, right. And if you adopt this definition that noise should just get killed in order for the inverter to be robust; then the region of transition were below some level it is treated as logic 0 and above some level it is treated as logic 1, what should be the transition value for the gain when I go from region 1 to 2, 2 to 3? What do you think this magic number for the gain should be?

Here gain is 0, here gain is 0, here gain is very high and it is a negative number; it is gain mod gain is actually much greater than 0, ok. So, what do you think should be this magic transition value for the gain, for me to determine these regions? Noise should not get amplified; that means the region, the point at which the gain actually hits minus 1 is the point to the left of which gain noise gets attenuated to the right of which noise gets amplified, sort of coming for the low level. For the high level right of that noise gets attenuated left of it, noise gets amplified.

Therefore the region of importance is really when gain equal to minus 1 that is d V out by d V in equal to minus 1, right. Because any small value, any if the gain goes slightly above that; then the noise is getting amplified. The least or the limiting cases noise does not get amplified, it just goes through as it is at least. You are still ok, because assuming that the noise is of reasonable value; it goes through to the output fine, it is not going to affect the next inverter too much. But if it gets amplified then you have a problem, ok.

Any questions here; yeah correct. So, by when we say noise it means that, it is a reasonably small signal; if you have like V D D noise, then that is not noise that signal, right. So, it does depend on the magnitude, but the assumption is it is reasonably small, ok. And that can sort of it is if it goes through an amplified or attenuated; no problem, ok. Why? Why because now if I have another inverter here, I have noise from here it goes unamplified here; then the same thing will continue in this cascading thing.

Now, if the noise comes here and then gets amplified, then the following stages will get will have a problem; that is why we are saying that as long as it is does not get amplified or gets attenuated, there is really no problem. That is my region that I am really going to be worried about and that is what is going to define; what is can be treated as a logic 0 for sure, what can be treated as a logic 1 for sure, ok.

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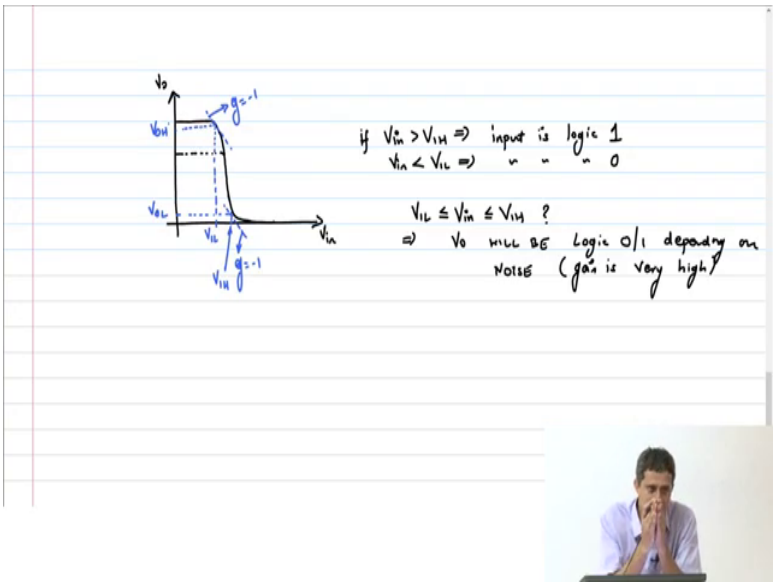

So, now let me just go ahead that is redraw this, so that it becomes easy to. So, there is some point where the slope is basically minus 1 g equals minus 1, ok. Now I extrapolate this onto both axis and find the intercepts; the first point I am going to call V I L, this is V out versus V in. This point I am going to call as V I H, ok. So, what does this mean now; if V in is greater than V I H, implies input is logic 0, I mean logic 1, ok. Now V in is less than V I L implies input is logic 0, right.

Now, what happens if V in is between V I L and V I H? So, if the input lands up in this region, it does not mean that the output will be stuck. For example, if the input is here, does not mean that the output will be stuck here; because at all times in your chip, there is noise there is some noise which is perturbing in all wires, some small noise that will get amplified.

And eventually depending on the polarity of the noise, the logic will switch to 0 or 1; there is no question about that, it will never remain there ok. Because the gain remember is extremely high in this region, even a small perturbation can switch it to logic high or logic low. The problem is it depends on the polarity of the noise. So, sometimes it can go to logic 1, sometimes it can go to logic 0; and therefore, this is an indeterminate region. If my input lands up here, implies V out will be logic 0 or 1 depending on noise ok; because the gain is very high, clear ok.

So, keep this in mind I only about V I H it makes sense, below V I L it makes sense, ok. So, these corresponding y intercepts right are my output V O L and V O H, ok. So, V O L is actually very close to 0, V O H is very close to V D D, ok. But V I L and V I H are not rare; that is actually very close to V D D by 2, somewhere around V D D by 2 this change is going to happen, right.