Digital IC Design

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Lecture – 18
Trip Point for Long Channel Device Inverter

So, good morning and let us continue with discussion in module 3. So, in the last class we look at the load line analysis of how to obtain the output voltage for a given input voltage by freeing the constraint variable. V out was made a free variable and then we plotted the current for the NMOS, PMOS transistors on the same axis and then found the intersection where I DSn is equal to minus I DSp, right.

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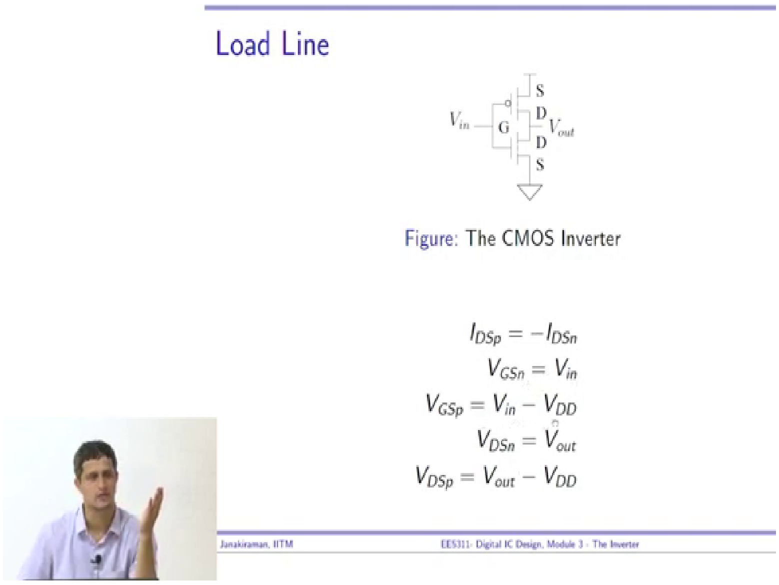

Then of course, the conditions V GSn is equal to V in, V GSp is V in minus V DD and so on have to be applied in order to find out various things.

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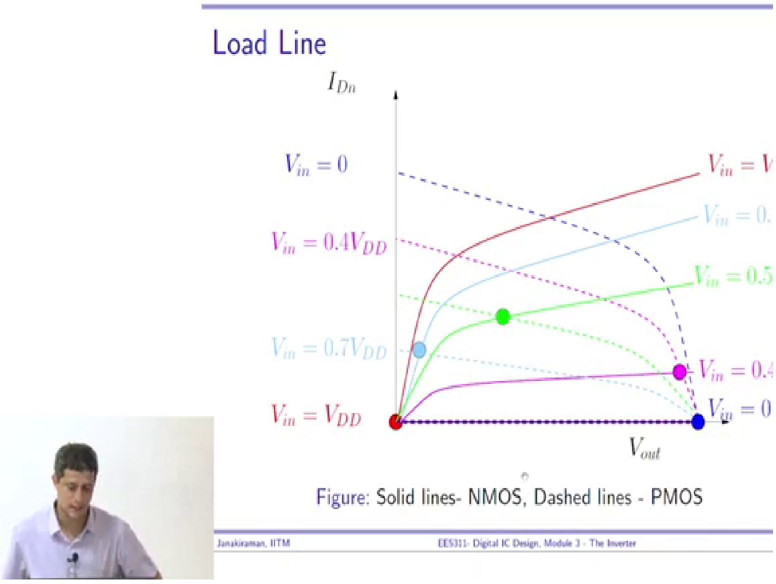

So, the conclusion was this that you take for V in equal to 0 the NMOS current is essentially 0 along the x axis. PMOS current after mirroring about the x axis and moving to the right, right you will get a curve like this which is the dotted blue line, ok. Yesterday, I showed both of them in solid lines, but this one is slightly better because it differentiates PMOS currents with a dotted line, right.

So, the point of intersection is this big blue dot, and therefore, the output has to be V DD, V out equal to V DD when V in equal to 0 that is the only point of intersection that is possible, ok. I also pointed out that there are many other points of intersection with the other curves like the blue dotted line intersects the magenta line, green line, light blue and red line, but those intersections have no meaning because they are actually for different V ins and therefore, do not get put off or confused by those points of intersection. You have to consider only the curves for the same V in and that point of intersection will be your final output, ok.

So, basically when I now move by V in slightly above V t n, all rights 0.4 V DD for example, I am assuming that is above V t n, then the magenta point of inter section will tell me very clearly that the NMOS is in saturation region because the solid line is clearly intersecting in the saturation region with the PMOS which is in the linear region, right.

The green one of course is both of them are in saturation somewhere in between it happens, then the NMOS comes to linear PMOS is in saturation the blue dotted line is in saturation. Finally, PMOS is what is going to happen is you are if V in is going to be V DD then NMOS will be turned on in linear region PMOS will be cut off, right and therefore, the point of intersection is this red dot which is V in equal to V DD V out equal to 0, ok.

So, as I told you if there is leakage current then this exact 0 and V DD will not happen. There has to be some current through the NMOS transistor. So, the PMOS will adjust the V DS, so that that amount of current is allowed through the NMOS transistor when V in equal to 0, right. So, then it will be slightly above 0, but it will be negligibly above 0, ok.

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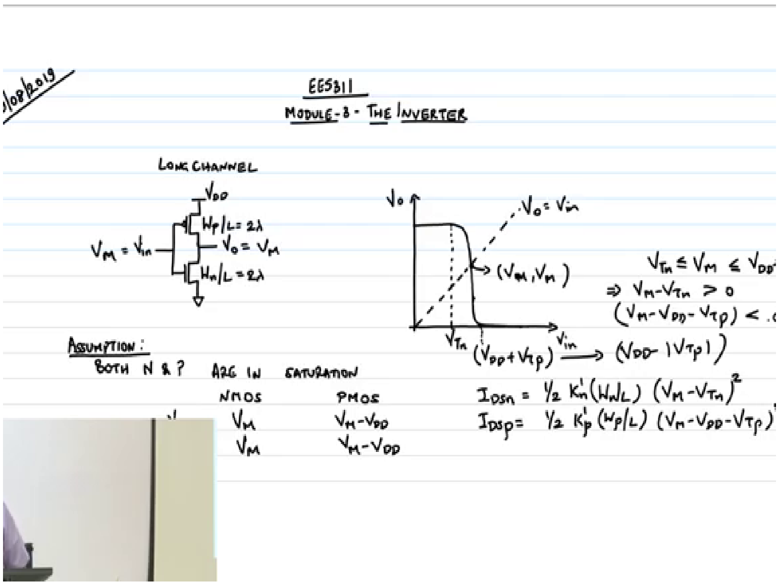

So, yeah. So, then we started discussing this switching threshold or the trip point, right. We were doing this analysis and then I after the class I realize that some of them were not very convinced with the argument I gave for why you should take the negative root, when I when we considered the case of long channel devices. So, what I will do is just for the benefit of doubt I will go through the long channel derivation once more because that was done towards the end and maybe it was done in a slight hurry, ok.

So, let us just consider a long channel device V DD, V in, V out and this is a long channel, ok. The width of the PMOS is W p length is L, W n and length is L, of course, length is always going to be 2 lambda width can be something else, ok. So, now, how do you find the switching threshold or the trip point? You basically plot V in versus V out and then this is the V tc, right V out versus V in and then you plot V in equal to V out curve here. This point of intersection is, so this is V in equal to V out, right or maybe I should call it (Refer Time: 05:33) its y axis is V out V out equal to V in.

Therefore this point of intersection is V m comma V m we want to find this point, right. And therefore, we are obviously, these two devices now are in saturation region because the V m is somewhere close to V DD by 2, both devices are in saturation, right, ok. This is only an assumption by the way. It needs to be verified after you get the answers with numerical values to be sure that the assumption is correct, ok. Let me reiterate that point.

So, now what is our various things? Right. V GS, V DS for NMOS and PMOS; V in equal to V out. So, this is also equal to V m, this is also equal to V m. So, what is V GS for the NMOS transistor? V m. V DS; V DS is what? No, no V naught, but here in this case V naught equal to V in equal to V m this also is V m. For a PMOS V m minus and this one, ok.

So, now, I DSn for a long channel device is half of K n prime W p by L sorry W n by L I am sorry into V m minus V Tn the whole square. I DSp is half of K p prime W p by L into V m minus V DD minus V Tp the whole square, ok. On this curve, can you tell me this guy somewhere here is where V Tn is? Somewhere here is V DD plus V Tp, right. Or if you want me to be very careful and you know indicate that it is a negative value I will say V DD minus mod V Tp, just to be just to show that it is a negative number there, ok.

So, V m is between these two values, ok. V m is necessarily greater than V Tn otherwise the NMOS will not turn on, right and it will also less than V DD plus V Tn, ok. This is the key point to note here which means V m minus V Tn is a positive number, but V m minus V DD minus V Tp is a negative number, ok. This is the main thing. So, this implies V m minus V Tm is greater than 0, V m minus V DD minus V Tp is less than 0, clear. Because this is the key data that point that we need to find out the sign after we take the square root, ok.

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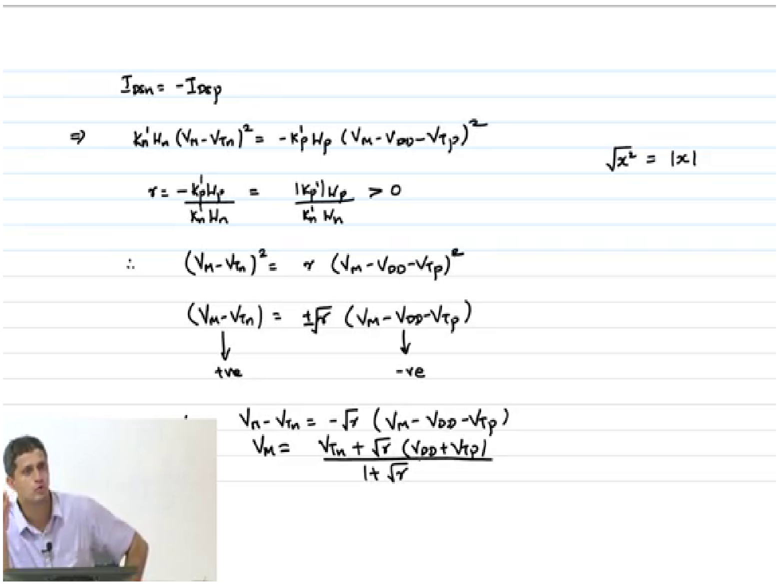

So, now what do we do? We go ahead and equate the two currents minus I DSp, right, implies K n prime W n into V m minus V Tn the whole square equals minus K p prime W p into V DD minus V T n V T, no, no V T D minus, no. V m minus V DD minus V Tp whole square.

Yesterday, I defined that the you know the I do not know what I defined as r in this case, but let me now define K p prime W p, right by K n prime W n itself as r. K p prime is a negative number, so this is actually equal to mod of K p prime W p by K n prime W n. So, it is a positive number, ok. So, therefore, I can say V m minus V Tn whole squared is r times V m minus V DD minus V Tp whole square. Now, I am going to go ahead and take the square root. So, V m minus V Tn equals plus or minus r into V root r into V m minus V DD minus V Tp.

Now, this is a positive number, this is a negative number. How can these two be equal? Only if you take the negative root. So, what this is basically saying is square root of x square, the positive root is what? Mod x. What if x is a negative number? Right. So, therefore, it is square root of x square, the positive root is always plus I mean mod x and that is what this is minus of that negative number is nothing, but modulus of that number, right. That is what we are using here.

Therefore, V m minus V Tn equals minus root r into V m minus V DD minus V Tp implies V m equals V tm plus root r into V DD plus V Tp by, ok. This r and the r that we used for velocity saturation is different, that that also as you sort of consumes the V Dsat parameter, ok.