Digital IC Design
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Lecture – 17
Trip Point for Short Channel Device Inverter

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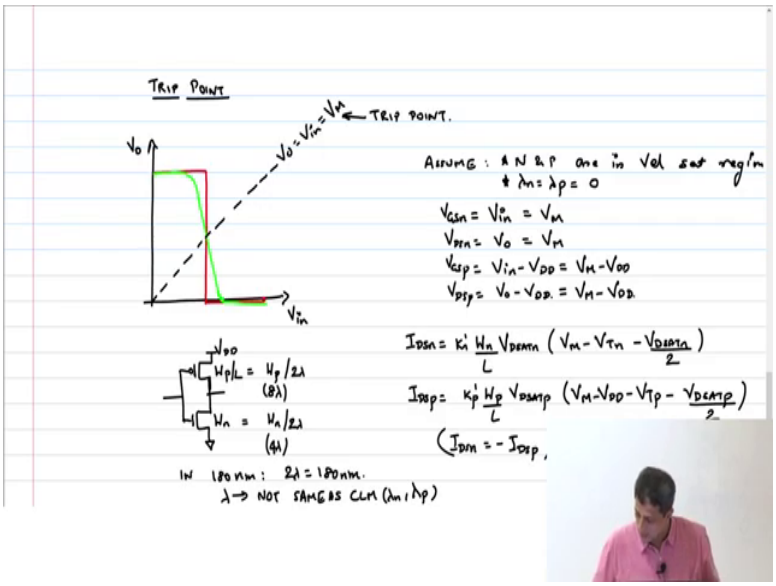

So, now let us look at this idea of a Trip Point, V out versus V in and we said that the ideal curve for this inverter should be like this right. At maybe V DD by 2 there is a sharp transition right of course, in reality that is not the case we have something like this ok. So, it is quite reasonable to assume if this region is quite sharp, this transition region is quite sharp then if I just plot V in equal to V out curve V out equal to V in that is sorry. The point at which it intersects my voltage transfer characteristic I can define to be my trip point. Ideally x if the characteristics were perfect and that point the inverter should have tripped, right.

So, the point at which V out is equal to V in is what we define as the trip point of the inverter. So, it may even think that well the inverter trips as long as you cross V TN right, but for other reasons it is better to define it somewhere in between ok; I will tell you why. So, this is going to be called V M, this point I am going to call it as V M, this is my trip point.

So now, I want to calculate the value of this trip point, ok. First of all approximately tell me in which region of operation will be transistor be in?

Student: (Refer Time: 02:34).

Saturation or velocity saturation, it really depends on whether it is a long channel or short channel. For now we will assume it is both transistors are short channel and therefore, it is in the velocity saturated region. We can also do a derivation for the saturation region, right. So, assume N and P are in velocity saturation region, ok.

So, what is V GSn at this point? Let me write it out explicitly again, this is V in V DS n equal to V out V GSp equals V in minus V DD. Please get used to this, we will use this again and again V DSp is V out minus V DD. So, when V in equal to V out equal to V M, this will simply become V M, right. This will be what? V M minus V DD; V M minus V DD, ok.

We will make one more assumption just to not complicate our derivation lambda n equal to lambda p equal to 0; no channel length modulation. You can put that in, you will just get some random quadratic equation to solve and it will give you no insight into what, how it actually controls you know various things, ok. So, now, what is the current through my NMOS transistor at this point?

Yeah.

Student: (Refer Time: 04:41).

K n prime W n, ok; now at this point I am introducing the bits of the NMOS and PMOS transistor. We have not really worried about it till now, the length of both NMOS and PMOS will be the same L ok, but the width can be quite different; I am going to call it W n and W p, ok. So, let me clarify that here explicitly I have the PMOS transistor V DD; this is W p and W n. I am not writing L because, both of them are minimum channel length and in the tutorial you would have seen that they use this technology parameter called lambda, ok.

So, typically the dimensions of the transistors are written as a function of this lambda ok. So, W by L will be maybe for example, L will be 2 lambda always. This is different from the channel length modulation lambda parameter, this is a technology parameter. So, if you are in a particular technology 180 nanometer; that means, the channel length is 180 nanometer 2 lambda is equal to 180 nanometer. So, for 180 nanometer technology lambda is 90 nanometer, for 90 nanometer lambda is 45 nanometer, ok.

The reason is this scaling sort of work very well in older technologies, ok; everything was represented just in terms of this technology length parameter. All designed rules everything that work well that time it does not work anymore, but for historic reasons you have just need to be aware of this, ok.

So, length is 2 lambda W p is something I do not know, I will have will have to fix it; this is W n. Typically, this will be 4 lambda and this will be 8 lambda and in 180 nanometer technology 2 lambda equal to 180 nanometer. And, also let me write lambda not same as channel length modulation lambda n comma lambda p; do not confuse it with that, ok.

Now, let us come back to the equation I DSn is K n prime W n by L into V DSATn right. What is V GSn? V M, V M minus V Tn minus V DSATn by 2, that 1 plus lambda V out I am leaving, because lambda n equal lambda equal to 0. I DSp is K p prime. What? W p by L V DSAT p into; sorry, V M minus V DD minus V Tp minus V DSATp by 2, ok when V in equal to V out equal to V M, these are my current equations assuming both devices are velocity saturated. This it might be it might surprise you is a big assumption ok. When you

actually solve a numerical and you will see in the tutorial, you solve with the assumption you solve the equations you get some values.

Now, you go back and plug these values into these conditions and see you will find that it may not be true. For example, one of them might be in linear region, ok. So, be aware that unfortunately unless you give me numerical numbers, I cannot verify this for you right. So, right now we are that is why I am saying this is an assumption it is not cast in stone, keep this in mind; in the tutorial you will see an example of this, ok.

So now, what do I do? I have to go back to my old condition I DSn is equal to minus I DSp right therefore, I DSn equals minus I DSp because it is not in place.

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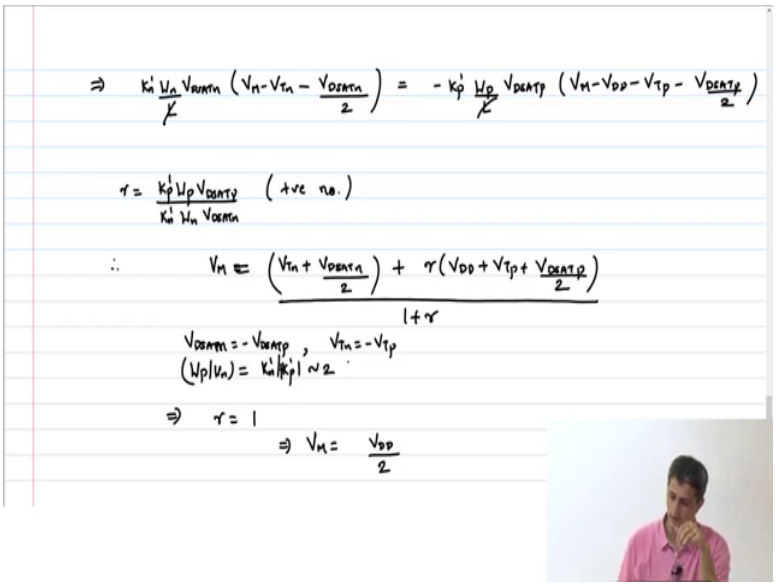

I go and equate this right which implies K n prime W n by L into V DSATn into what? V M minus V Tn minus V DSATn by 2 equals minus K p prime W p by L into V DSATp into V M minus V DD minus V Tp minus V DSATp by 2, clear. So, of course, all of this goes away, ok. Now, let me define K p prime W p into V DSATp by K n prime W n V DSATn equals r, ok; quick sanity check, this r a positive number or a negative number, ok.

Student: (Refer Time: 11:34).

K p prime is a negative number, V DSAT p is also negative number. So, negative-negative positive, r is a positive number ok. Now, can you go ahead and derive the expression for V M in terms of r and the remaining technology parameters? Of course, V DD is also there; are you getting this answer? Yeah. Ok, very good.

So now, let us look at some let us see how to interpret this alright, I mean first of all there are too many terms in this, ok. So, let us make some assumptions that V DSATn equals minus V DSATp and K p prime; I have no control over that. Because, that is approximately 2 is to 1 right, mobility or 1 1 by 2.

Let us assume that W p by W n equals K n prime by K p prime rather by mode I would say. So, what does this condition give us? What is r? 1 clear implies r is equal to 1, ok. Now, apply the same condition out here V DSATn equal to minus V DSATp. Where will V M land up? Yeah, V DD by 2 right because this is now and of course, I am also assuming V Tn equals minus V Tp, technology is symmetric is what I am assuming. This implies V M will simply be V DD by 2, ok. So, if you are of course, K n prime by K p prime is usually approximately 2 mu and C ox, if you take that ratio this is approximately 2. So, if W p by W n is 2 then V M would land up at V DD by 2 approximately ok, but even otherwise this would be somewhere around that V DD mark, ok.

Now, what happens if my W p goes up? Yeah, sorry V M will decrease actually that is not very obvious from this equation because, there is a r on top, there is an r below and all that. So, therefore, this may not be so obvious to understand, ok.

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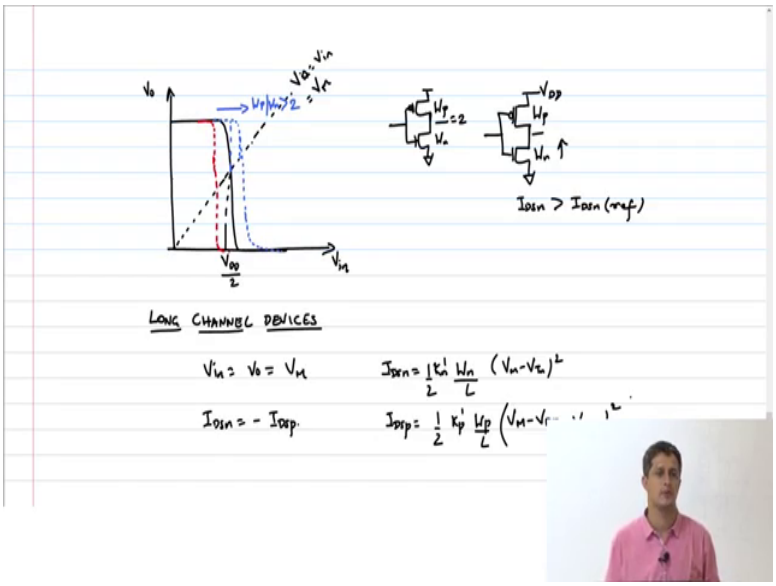

So, let us see if we can first get this intuitively ok, then we will go back to that; V out versus V in this is somewhere here is my V DD by 2. This is V in V out equal to V in equal to V M, ok. Now, if I increase my W p by W n I want to know how this curve will shift, it will shift to the right side, let us see why ok. So, he is saying the following, why do you think it should happen? Yeah.

Student: (Refer Time: 17:56).

So, basically the PMOS gets stronger that is the width of the PMOS is going up; that means, the PMOS current is stronger for the same V in as I would have had for the earlier case, right. So, if that is the case then where should V naught land up? No, why that is what I am asking.

So, for the same V in right you are saying that the PMOS now has a higher current right. So, how will V out adjust itself to accommodate this higher current?

So, if my width goes up, I am able to accommodate more current in the PMOS transistor just because of the width; that means, my V DS can come down, right. I do not need higher V DS to get the same current. So, therefore, the V DS has to drop; that means, the V out will go closer to V DD, right and that is what we are seeing here; you should look at it. For the same this thing, for the same input the output is closer to V DD for the case when W p is higher than W n, ok. So, this is W p by W n is greater than 2.

So, if the PMOS transistor becomes stronger then the curve shifts to the right, ok; similarly, if the NMOS transistor becomes stronger you can apply the same argument, ok. Let us maybe do this thing very clearly; so, that maybe some of you did not follow my argument here. V DD, now my W n has gone up ok; earlier my reference device was W p by W n equal to 2 ok. This was my reference device W p W n by equal to 2, now W n has gone up; that means, the NMOS is a stronger device compared to this.

So, for the same V in what should happen, the NMOS current is going to be higher in this case; here I DSn is of this guy is greater than I DSn of reference. Now, if that happens then my V out which is basically the V DS of my NMOS transistor can drop because the width is giving me more current. I do not need the V DS for me to give me the current there. Therefore, the V out can now drop and that is the basic idea where we say that if you do this right, for the same input voltage the output will be now lower when NMOS is actually strong.

Are you all following me here? This is just the intuitive picture right, you can go back maybe simulate this and see how it actually goes with r, right. You can simulate this V TC, change your W p by W n and all that stuff and check what happens, ok. You will see it, I am just giving you the intuitive picture here clear. Any questions? Ok.

So now, I am just going to give you a quick hint for what happens if the devices are long channel image which means there is no velocity saturation, this guy will go into saturation, ok. So, I want to do long channel device, same thing we are going to do V out V in equal to V

out equal to V out equal to V M, I DSn should be equal to minus I DSp of course, at all times, ok.

What is my long channel saturation current now? I DSn is K n prime W n by L into V in that is V M, V M minus V Tn the whole square; whole square I have half. I DS p is half K p prime W p by L into what? V M minus V DD right, V Tp the whole square. So, what is V M now? What is V M? Can you derive it? What is the condition? I DSn equal to minus I DSp, right.

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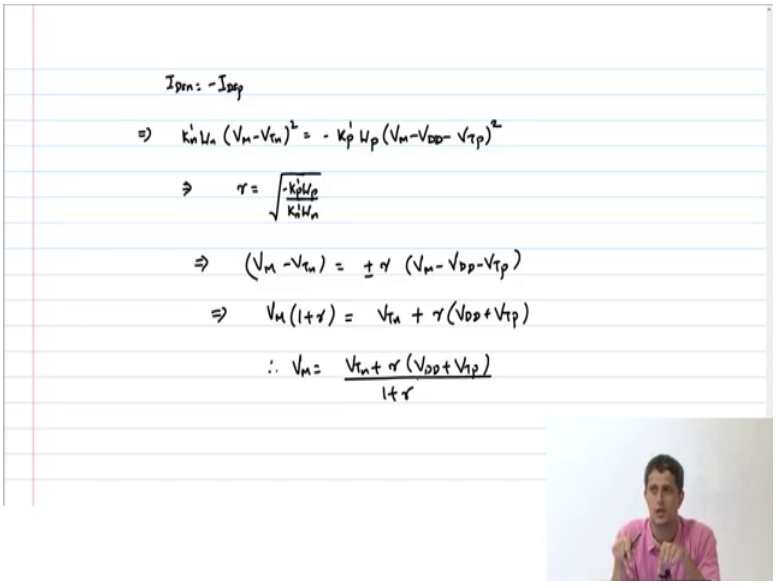

Implies K n prime W n into V M minus V Tn the whole squared equal to minus K p prime W p into V M minus V DD minus V Tp whole squared. So, now, there is a small trick of course, I have a square; so, that minus sign you should be careful about, but that is not the real issue because minus K p frame is a positive number, right.

So, if I define r as root of minus K p prime by K n prime W p by W n. K p is prime is a negative number minus K p prime is a positive number therefore, r square root no problem, clear. When I take square root how do I decide if it is plus or minus? You get my problem right, now this is V M minus V Tn equals plus or minus r into V M minus V DD minus V Tp.

Student: (Refer Time: 26:00).

Correct; so, therefore.

Student: (Refer Time: 26:11).

No, but; so, let us go with his argument first if V M minus V Tn has to be positive, then if I take plus r into V M minus V DD minus V Tp will that guarantee that this is always positive? So, therefore, the minus sign has to be taken there correct implies V M into 1 plus r right equals V Tn plus r into V DD plus V Tp, V M equals V Tn plus r into V DD plus V Tp by 1 plus r, ok.

So, it is very likely you might think that I am doing this plus minus because K p prime is a negative number that is not the case. K p prime negative is already negated by the I DSn equal to minus I DSp that is taken care of when you take square root, there is a plus or minus that has to be resolved appropriately.