Digital IC Design
Prof. Janakiraman Viraraghavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 16
Load Line Analysis

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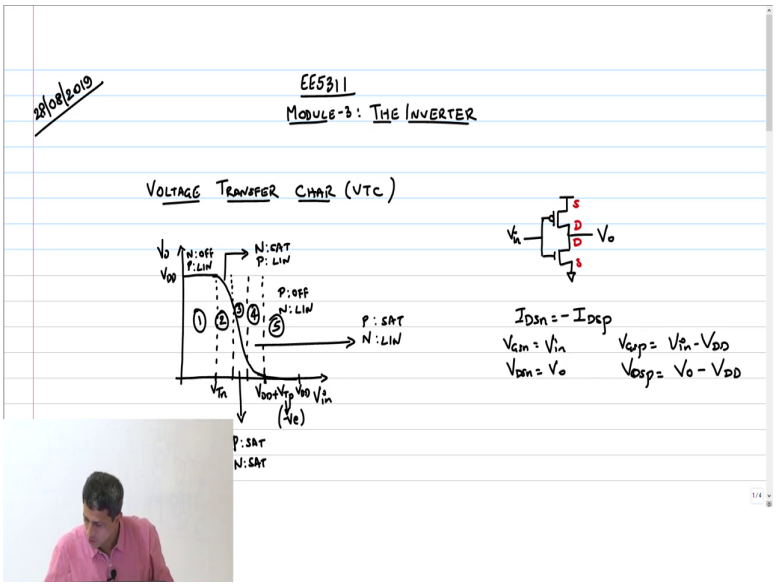

So, last class we were discussing the voltage transfer characteristics right. Characteristics it is called VTC, the abbreviation and just to remind you this is my inverter that I constructed last time. We looked at various combinations of charging a capacitor and discharging a capacitor with NMOS PMOS, we looked at all four combinations and then concluded that PMOS can be used only to charge a capacitor, NMOS can be used only to discharge a capacitor.

So, that the output voltage swing is actually rail to rail. And therefore, our CMOS inverter complementary metal oxide semiconductor inverter is made of both NMOS and PMOS ok.

There are alternate ways of making these inverters which you will see in the tutorial. For example, I can replace the PMOS with a resistor even then you will get an inverter right. Voltage swing may not be rail to rail and all that, but you can analyze that as part of the tutorials based on what I am going to teach today ok.

So, V in and V out and we said that you intuitively we were able to arrive at this VTC right. So, if I sweep V in right and plot my V out and I sweep V in from 0 to V DD it goes through certain transition points. The first transition point happens to be at VT n because until then the NMOS transistor is not turned on and if the transistors are considered to be ideal it means that there is 0 leakage current. And therefore, V Tn is the first point when V in crosses V Tn some nonzero current can flow through the NMOS transistor right.

And then we had another condition which is basically V DD plus V T p. Remember that again let me keep reminding you V T p is a negative number whereas, V T n is a positive number. Both of these invariably will be the same in magnitude, but it will be opposite in sign plus 0.5 volt minus 0.5 volt alright. So, V DD plus V T p is actually less than V DD and this point is of course, V DD ok.

So, if I look at this thing here output will start at V DD, perfectly at V DD if the NMOS current is 0 before V T f, which is true if it's an ideal transistor and there is no leakage current. So, it will be perfectly a V DD and remember what is our constraint; I DSn is equal to minus I DSp. This is the constraint this is not an artificial constraint that we are imposing, it happens because the two transistors are in series and therefore, the series currents have to be the same which means V out will adjust itself so, that these two currents are always the same at all for all input combinations this is true right.

And again to remind you this is the drain for the NMOS, this is a brain for the PMOS sources fixed at V DD and we also evaluated V GSM equals V in, V DSn equal to V out, V GS p equals V in minus V DD then V DSp, V out minus V these are the 5 equations that we used ok. So, the voltage transfer characteristic starts off at V DD, once you cross V Tn there is some nonzero current.

So, V out will now start dropping from V DD right, because some nonzero current has to flow through the NMOS transistor; that means, there has to be some V Ds across it right and V Ds of the NMOS transistor is V naught. So, the V out will sort of start dropping a little bit right for the PMOS that is I am sorry ok, this will drop like this and again after V DD plus V T p it will come back to 0 output, output will be perfectly 0 ok.

There are, so if you look at the region of operation we said NMOS is off, PMOS in linear. Here PMOS is off NMOS is in linear right then we introduced we had one more region somewhere in between it goes through where in this region NMOS's is going to be in saturation. So, the moment we in crosses V T n the NMOS turns on in saturation; PMOS will turn on in of course, PMOS continues to be in linear region. In this region both n and p will be in saturation or velocity saturation depends on whether it is a long channel or short channel device.

This region is going to be; what is N and P?

Student: (Refer Time: 06:19).

Yeah.

Student: (Refer Time: 06:21).

No no.

Student: (Refer Time: 06:24).

Yeah. NMOS linear PMOS saturation; so, it is exactly a dual ok. So, this is what we derived last class, the regions where 1 2 3 4 and 5 ok. So, intuitively we came up with this picture ok. Now, the question is how do you actually arrive at these exact numbers and that is what we are going to look at in this class ok.

Especially when you are trying to do for example, the PMOS is not, if the PMOS instead of PMOS I put a resistor then what do you do there.

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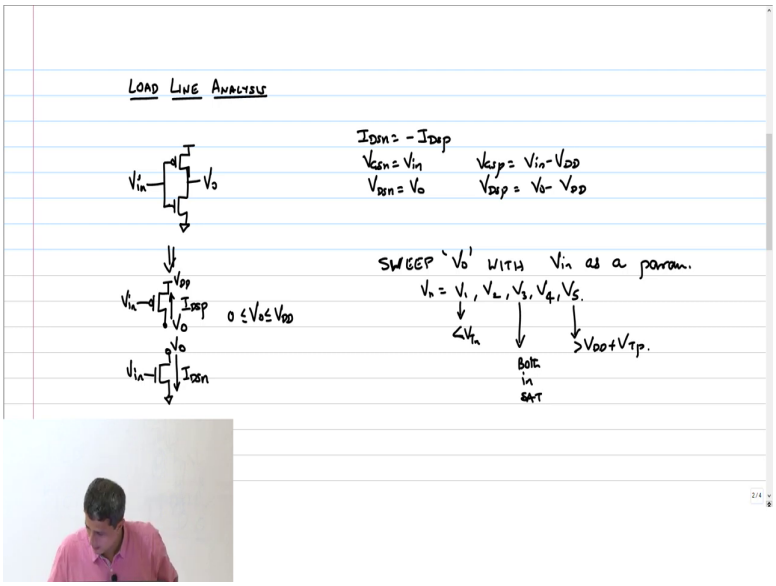

So, in that case we resort to something known as a load line analysis; you load line analysis is the following. I have the inverter like this, I have two devices who each of which has its own current equation right and it has a constraint that is being imposed because of the way in which you have connected these devices at the two currents have to be the same right. So, if you look at this V in is here V out and the currents are sort of, in some sense constraint it can't take any arbitrary values right.

If I tell you that by V in is so and so then to satisfy both n and p constraints V out will settle to some particular value appropriately right. So, what you do is to analyze this, you free this constraint variable. So, you make V naught as a free variable and then you sweep V naught

from 0 to V DD and then you look at the currents, for both n and p as a free variable you do this. And then you impose the constraint that these two currents have to be the same, then you find out where these two meet that will be your actual V naught that it will settle to ok.

So, we look at that particular example let me just write the five equations again, I DSn equals minus I DSp then we have V GSn equal to V in V DSn equal to V out V GSp equal to V in minus V DD V DSp equal to V out minus V DD ok. So, what I am going to do is I am going to free this variable V naught ok, I am going to basically make it like this V in this is V DD then I have V naught here ok. I am going to have a current which is going to flow from drain to source like this, I DSp V naught will be swept from 0 to V DD clear.

I am also going to free my V naught for the NMOS transistor V in this here current will flow like this I DSn and this is my V naught ok. I am going to now free this variable sweep it, find out what the currents are and then I will equate these two in the end and then find out what the V naught should be clear. So, in order to do this I am going to now plot it for various values of V n ok. So, obvious very natural now, that we looked at some five regions of operation right.

So, I look at five different values of V in ok, point is sweep V naught with sorry with V in as a parameter ok. So, I want to consider V in equal to V 1, V 2, V 3, V 4 and V 5; V 1 will be less than VT n right, the first region of operation this I am going to say is V 1 is less than V Tn, this will be greater than V DD plus V Tp, V 3 is some value I am going to choose so that both transistors sort of operate in saturation region ok.

So, both saturation region V 2 and V 4 will be chosen such that one is linear other saturation and vice versa ok. I just need to actually I should do this for a continuum of V Gs so that you can see what, but since we have only limited plots that we can do I am choosing this very specifically clear yeah.

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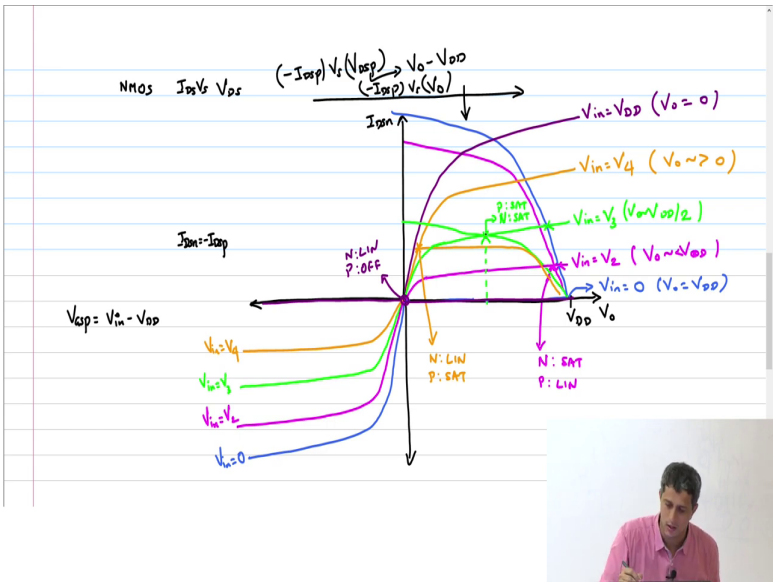

So, now what I want to first do is to plot by NMOS current ok; NMOS id versus V out right, I will say ids versus V DS actually what is V DS for the NMOS it is V out. So, there is no big thing there I DSm verses V out I am going to sleep V out from 0 to V DD what is the current through the NMOS transistor when V in equal to V 1 as I told you I mean V 1 as defined here below V T n 0 ok.

So, now I will use some special colors. So, that we do not confuse things. So, the current through this guy with respect to what your V out is whatever the V Ds is current has to be 0 through this well transistor is not turned on and here is my V DD fine. Now I take my V in slightly above V Tn, so what will be current through this and how will this plot look like? It is basically going to go through our earlier equation. So, it will be something like this, correct this is for V in equal to V 2.

Now, I am going to take V in equal to V 3 which is obviously, higher. So, therefore, this again will go from here and it will look like this, you for simplicity let me assume that this is just V in equal to 0 volt. Actually it is from 0 to VT n it is just the same thing ok.

Then I am going to assume another color I need now. So, let me take this, V n equal to V 4, V 4 and of course, when V in equal to V DD I will have the highest possible current through my NMOS transistor and therefore, for that I will use maybe blue is over ok, equals we 5 right or I will just call this V DD because that is now V in equal to 0 ok.

Yes.

Student: (Refer Time: 15:44).

Yeah, it can get saturated. So, let us not go into that detail for now. So, let us assume that this is a long channel device I have just shown non 0 channel link modulation for now, but let us assume that its the velocity saturation does not occur here yeah.

Now, I want to first plot I D sp versus V DSp for the PMOS transistor, I am not looking at V naught nothing for various values of V n I DSp versus V DSp, which quadrant will it like? This is the third quadrant right. So, therefore, I need to look at the plot now in the third quadrant here, you just one constraint we are going to introduce now which is basically V GSp is V in minus. What is V GSp? V in minus V DD ok.

So, now for V DD equal to 0 V DSp is how much minus V DD right. So, if I now sweep my V DSp from 0 to minus V DD I will have the highest possible current through the transistor right. So, the key thing to note first is the corresponding blue curve here which is the same current for V in equal to 0, is actually going to be the highest.

This is for V in equal to 0 ok. Now what happens when V in equal to V 2? Slightly higher the V GSp is now dropping, mod V GSp is dropping from V DD to slightly lower. So, the curves will actually be an inverted version of that. Lowest current there corresponds to highest

current here because I am now looking at it for the same V in, I am not looking at this for V GSp it is for the same V in because now V GSp is V in minus V DD that I have already incorporated ok.

So, therefore, the curves if I color code correctly the magenta will basically come out like this, V in equal to V 2, then the green they will come out like this right then orange will come V 4. There will be curve for being equal to V DD be 0 right, because now V G sp has gone mod V G sp has gone below mod V T p correct. So, therefore, this final curve is going to sit on this x axis like this.

Now, these are complete free variables we have not imposed any of our constraints. We will now impose the first constraint which is I am going to say I DSn equals minus ID sp. What will this do? It will mirror it about the x axis right. So, therefore, the first curve will just remain as it is and this is 1, then and. Yeah approximately not greatly drawn, but fine ok. Now, I want to superimpose this on my I Dsn versus V out itself remember.

Now, this curve is id minus of I DSp versus V DSp, this axis whatever curve we have drawn is these curves here are all I DSp minus of I DSp versus V DSp. But what is V DSp this is nothing, but V naught minus V DD right. Therefore, if f of x is there, how does f of x minus x naught looks like move to the right, correct whole thing just shifts. So, x equal to 0 will happen at x equal to V DD right because it is V out minus V DD.

So, now we are going to redraw these curves quite carefully and I am going to make this transformation of going from here to here, I am going to make this minus I D s p versus p out minus V DD right or rather it is going to be with respect to V out.

Student: (Refer Time: 21:50).

Yeah? Correct, correct sorry this will be with respect to V out you are right correct ok. So, now, all we have to do is make the plot wherever I DSn's and minus I DSp meet that will be the operating point. Your V out will settle to that particular value finally, ok. So, let us go

ahead and draw these curves for V in equal to 0, how is the curve want to look you it is this curve right that is going to shift all the way there correct oh sorry.

I can actually move it wow I did not know this brilliant ok, have to mirror that also right anyway. What is the point of intersection, at V DD right the two curves blue curves meet only when the current is actually 0, the key thing that you have to notice is there are many points of intersection here which make absolutely no sense because they are for different means. In a textbook when you take it especially Indian edition because it is in black and white you cannot make out this.

So, that is why it is important to color code this or by the foreign edition you will see the colors there, it sort of makes it easy for you ok. So, now, let me yeah similarly I am going to move this curve right. So, it is going to start from here yeah. So, now, where do these two curves meet? Yeah? Here right this is my point of intersection correct.

Now, let me ask you a question in which region is the NMOS transistor, which region is the PMOS transistor? NMOS is in because if you just look at it you will know the current is in saturation region where is the PMOS current is in linear region right. So, this point corresponds to NMOS being in saturation, PMOS being in linear region.

Similarly, I can now move this guy. What is this maybe this alone I will just rewrite for V in equal to V 3; obviously, this is my point of intersection very evidently n and p are in saturation period and again this I can sorry, yeah; this two. So, this point of intersection is here. What is the region of operation for n and p?

Student: (Refer Time: 26:46).

NMOS is in linear PMOS is in saturation right. So, this is N in linear, PMOS in saturation region ok. And of course, now the final one is for the V in equal to V phi which happens to be 0 along the x axis point of intersection is origin ok.

So, this guy is again what? NMOS in cutoff, PMOS in what? Linear region, is the previous one yeah PMOS sorry sorry PMOS is cutoff yeah PMOS is cut off and NMOS in linear ok.

Now, from here it is also very easy to find out what d corresponding V out is right, when V in equal to 0 it has to be V DD ok, this guy here V out is equal to V DD. Exactly equal to V DD when there is no leakage current. And this guy is how much? maybe I should use the same color V out is equal to V DD ok.

This one is somewhat close to V DD right, less than V DD, but close to V DD. So, this is V out is approximately close to V DD maybe approximately, but less than I will just add that symbol ok. This is clearly you can see V out is somebody here, halfway somewhere here right; V DD by 2 approximately V out. What about this? P out is approximately greater than 0, but very close to 0 fine and here of course, V out is exactly 0 ok.

Now, I can ask you the question. In which of these regions is a current going to be maximum?

Student: (Refer Time: 29:45).

The third region right, basically that is where this particular the green intersection is when the current is also maximum because this is the maximum current that is allowed to flow, when the input goes from 0 to V DD.