Digital IC Design
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Lecture - 15
Voltaage Transfer Characteristic

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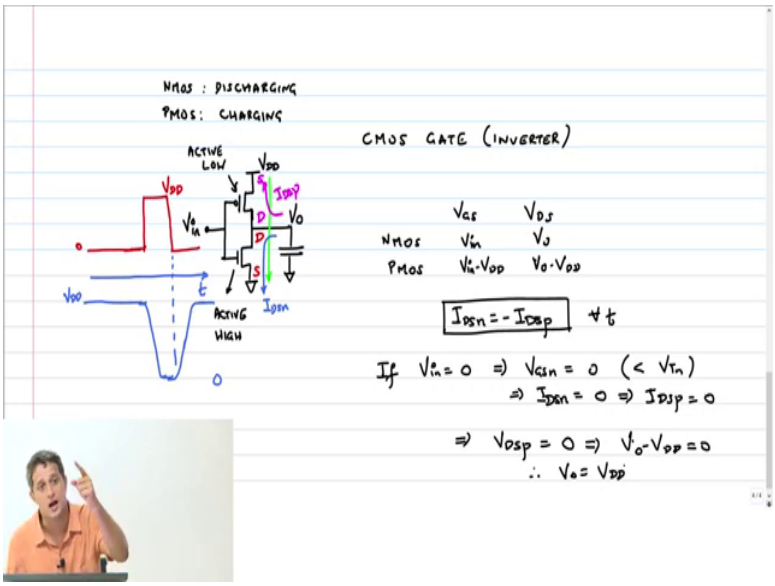

So, let us put down what the drain source and all that is what is the drain for the NMOS transistor. V naught right sources crown PMOS transistor drain is, yeah. Basically, the source has to be fixed should not change any input is changing right only then you are gate overdrive will always be as good as it can be, right. So, therefore, the source for the PMOS has to be V DD source for the NMOS has to be ground ok.

So, this you know this logic gate has some constraints when this input goes from 0 to V DD and the output falls like this, there is one constraint that is always maintained in this logic

gate, what is that constrain? Ok. So, let us now list now let us list out these conditions and then you will I think you'll get it after that.

So, let us look at V GS and V DS for the NMOS and PMOS ok, the input to the gates are V in the output at the drain of both this transistor this V ou.t ok. So, what is V GS of V NMOS transistor, it is V in V DS V out. What about PMOS V in minus V DD, V DS is be careful it is V out minus V DD, V DS.

Now, there is some V GS some V DS on the NMOS some V GS V DS on the PMOS what should happen to these 2 currents, at all times they both have to be equal in magnitude, ok. Remember that the current in always will flow from supply to ground like this when the current can flow that is assuming that one transistors allowing conduction, right. For example, if the NMOS is off and can allow no current then there can be no current in the PMOS as well right, it is series.

So, the constraint that is going to be imposed is I DSn NMOS current, remember the direction for I DSn is like this; I DSN, what is the direction for the PMOS current? No, no, no, I D S direction it has to go from here like this is I DSp. So, therefore, I DSn should be equal to minus I DSp, this will hold at all times for all,.

So, now, assuming that the transistor is ideal, suppose the input were 0 what is I DSn, it is an ideal transistor input is 0, what is I DSn 0, right therefore, the current to the PMOS also has to be 0 right which means that the drain voltage will adjust itself. So, that you get this 0 current happening appropriately ok. So, let us look at that suppose if V in equals 0 implies V GSn is how much, V GSn is 0 this implies I DSn equals 0 because it is less than V in, ok.

Now, what is the V DS on the PMOS such that the drain current to the PMOS can also be 0 you get my point right if because of this constraint my V DS on the PMOS transistor should adjust itself. So, that the current is 0, V DS equal to exactly. This implies V DSp should also be 0 right now, this implies I DSp should be 0 right therefore, V DSp should be 0.

So, if V DSp should be 0 it implies V in minus V DD equal to 0 and I mean V out I am sorry, V out equals V DD, clear. This is a more rigorous analysis of the same thing that we just discussed where the input is low, output will be high because these currents have to match.

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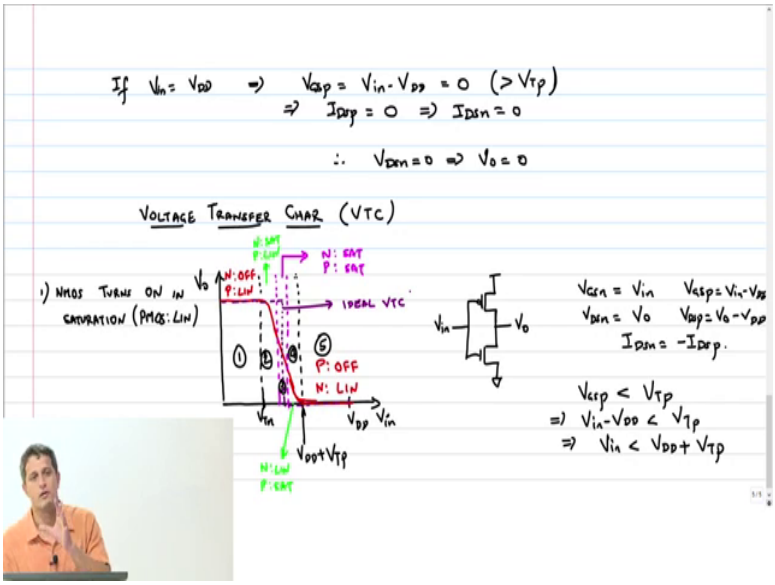

Similarly, if V in equals V DD implies what is V GSp what is this V in minus V DD right equals 0 right and; obviously, this is greater than V Tp. Remember, V Tp is a negative number it should be less negative than that only then it can happen or it is bit more negative than that only then it can conduct. Therefore, I DSp should be equal to 0 which implies that I DSn also has to be 0 and therefore, what is the only way this can happen, the drain source voltage of the NMOS transistor should be 0, ok.

So, therefore, V out I will write that step V DSn equal to 0 implies V out is 0 any questions here, ok. So, this are the extremes that we analyzed ok. The idea of doing a voltage transfer

characteristic is to sweep V in from 0 to V DD and then analyze what will happen to V out in the process by applying exactly these constraints. What will happen is as you sweep V in from 0 to V DD for each value of V in right V out will adjust itself. So, the. So, that the current in both NMOS and PMOS will be the same, ok. So, that leads us much time (Refer Time: 08:13) yeah, I have rub that Voltage Transfer Characteristics, VTC ok.

So, first we will look at this intuitively and figure out what should happen and then we will look at the more rigorous way of identifying these points on the VTC ok, first we look at the intuition. So, we are going to plot V out versus V in for my CMOS inverter V in V out right, and of course the constrains are simple V GSn equal to V in, V DSn equal V out V GSp equals V in minus V GD. V DS equals v out minus V DD and I DSn equals minus I DSp ok. So, what we are going to now is to sweep V in from 0 to V DD.

In the process there going to be some transition points, right. So, when we sweep V in from 0 to V DD what do you think the first point of transition will be. So, V in equal to 0 what is the state of the NMOS transistor off at what point of course, if I increase the gate voltage to V DD NMOS will turn on. So, somewhere in between it is turning on what is that point? V Tn it has to turn on, right.

So, therefore, this is going to be my V DD, the first point of interest is V Tn. For an ideal transistor where leakage current is 0, output has to be what until I reach V Tn has to be V DD because the V DS of that PMOS has to be 0 and therefore, the thing has to be V DD, right. If there is some finite amount of leakage current; however, small it is then V DS has to allow that much current to flow through PMOS transistor.

So, V DS will be slightly lower than V DD right, this is the ideal case, but for now let us look at the real case ok. So, I am going to consider this output will start at V DD now, the NMOS transistor is turning on as soon as I cross that V Tn it is turning on in what region of operation will my NMOS transistor be. Saturation you agree why because, V GS is how much, V GS is just very just slightly above V Tn. So, V GS minus V Tn is a very small number, but V out is nearly V DD.

So, therefore, the NMOS will turn on in saturation, this is the first point that we have to consider. NMOS turns on in saturation, ok. Now, what about the PMOS transistor in that region, why linear. Actually tell me even before suppose V in is less than V Tn which region of operation will PMOS transistor be it will be in the linear region (Refer Time: 12:58) because it has to depend on V DS, V DS has to be 0 right

So, therefore, it is in that linear region, also the PMOS will turn on at the same time PMOS is linear region right, and of course, now current is going to flow because both NMOS and PMOS are going are on, right; one in saturation other in linear respectively therefore, the V out will adjust itself slightly lower than V DD, right. So, the V out will now start falling. At some point the PMOS transistor will come out of this linear region and get into saturation or the velocity saturation, you agree with me why is that, what is happening to the V DS of the PMOS transistor over a period or what is happening to mod V DS? It is it is increasing right and therefore, the V DS at some point VDSp mod, V DSp will exceed VGS minus V T of the PMOS and therefore, that will get into the saturation region at some point and this will happen somewhere near V DD by 2, ok.

So, there will be one point in which both NMOS and PMOS transistor will be in saturation region, ok. So, this will continue to happen now at what point will my PMOS go off. So, for that what is my V GS, V GSp. So, V GSp should be less than V Tp; I mean, less than V Tp only then it can turn on V Dp is a negative number. Again, let me remind you again and again which implies V in minus V DD should be less than V Tp, right. Only then it can turn on which implies when V in should be less than V DD plus V Tp.

So, this point is not V DD minus V Tp or if you want to say V DD minus there is a V DD minus mod V Tp. So, this point is going to be where the PMOS transistor turns off is V DD plus V Tp, ok. And we will come all the way down here and of course, the output will be absolutely 0, after that why because now it is an ideal transistor PMOS transistor cannot tolerate any more current therefore, what should happen to the V D S of the NMOS transistor 0, ok. Now, in this region when the PMOS is off what region of operation is my NMOS is it is in linear region.

So, here PMOS is off, NMOS is linear out here NMOS is off, PMOS is what linear. Now, like I said there is one small region where both here both N and P will be in saturation, ok. Saturation or velocity saturation depends on whether you are talking of a long channel device or a short channel device. The reason before that here what will be my NMOS state, PMOS state. Again, N is saturation, PMOS in linear and the exact opposite will happen in this region where NMOS is in linear PMOS is in saturation, ok.

So, there are like how many regions; region 1, 2, 3, 4 and 5. There are five regions that the voltage transfer characteristic goes through and you should be able to explain each one of them correctly, ok.

So, we will look at primarily this region 3 will be of very much of importance to us because that is where the sort of the trip point that I spoke about occurs ok. So, this is the V in, V out versus V in of our actual inverter. What was the V Tc that we wanted of an ideal inverter sharp line right, we wanted the ideal V Tc to be something like this; basically, up to this point it will be V DD and then it will just drop, ok. So, this was ideal V Tc, ok.

So, clearly right here you see that there is a region or a range of input values which are treated as logic loop which means the output will be logic high, right. Similarly, the range of input which will be treated as logic high, the output will be logic low no problem, but there is an indeterminate region in between which is neither logic 0 nor logic high. I will tell you why it is you know you, I will show you why that happens and this is of primary importance to us.

Because, this is where the input should not go in line if it does line then the output becomes a random value dependent on noise, ok. We will we will come to this later, but for now I am just giving you the intuitive picture of how the voltage transfer characteristic is different from the ideal V Tc that we wanted, ok.