Digital IC Design
Prof. Janakiraman Viraraghavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 14
CMOS Inverter Construction

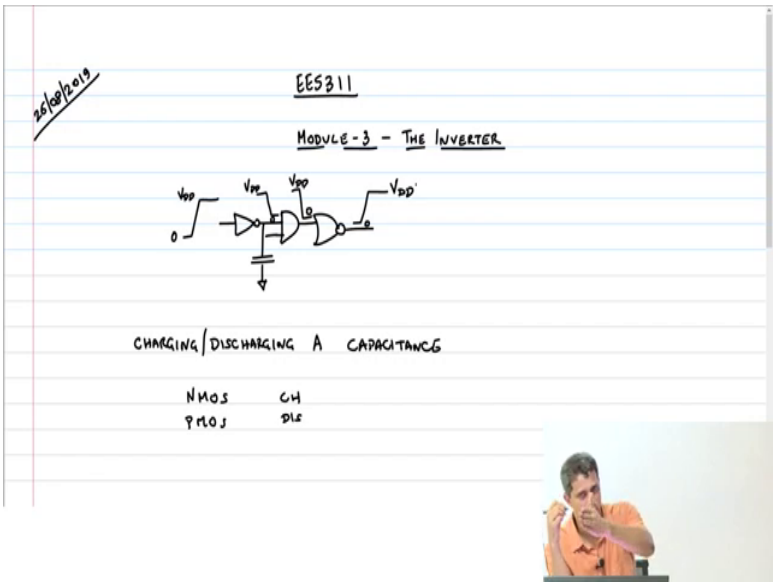
Good afternoon and welcome back. So, last module we completed the module on interconnects right, it is a very short module we just mainly focused on the Elmore delay derivation right, for an RC tree, ok. And, in the process you should have been you should be able to now estimate wire parasitics given the sheet resistance right that r square that I spoke about is basically call also called sheet resistance and the capacitance per unit length, right.

Then, you should be able to derive the Elmore delay for a given RC tree right, any arbitrary RC tree you should be able to derive it not just apply the formula, right. Like, I showed you may making those assumptions and stuff like that you should be able to derive the time constant with which each capacitor in the tree will charge up or discharge, ok. When you discharge the assumption will be slightly different it has to be a discharging equation rather than a charging equation, ok.

Then, you should also be able to estimate the wire RC delay by applying the Elmore delay to a distributed RC network. So, this we saw that you overestimate the RC delay by about a 100 percent, right. If you by 50 percent sorry, actually or it depends on how which one is your reference if you choose a distributed versus the lump RC model, right.

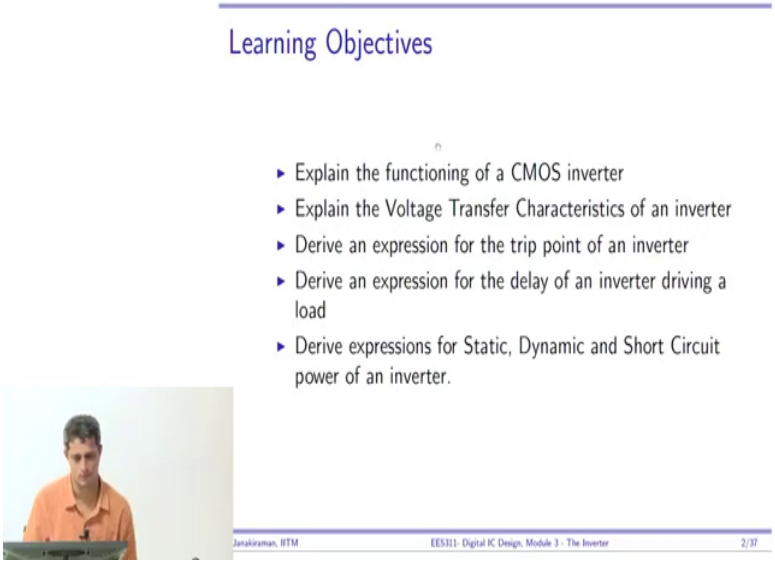
Remember, the main takeaway you can neglect the resistance of the interconnect, but at no time can you neglect the capacitance that has to because that adds to the load, right. Suppose, it is a if it is a very small wire then you can neglect that thing, but otherwise usually the capacitance you can add, but wire cant resistance can still be neglected in some cases as I derived in the module, ok.

(Refer Slide Time: 02:14)



So, let me take this off. So, with that we move into module 3 and probably this is one of the most critical modules of this course ok, because this is where we actually take our learnings from the transistor and apply to build logic gates, ok.

(Refer Slide Time: 02:34)



So, this is the inverter is actually studied in reasonable detail in this course because many of these results can then be carried over to the other logic gates as well that we will see in module 4, ok. So, what are the learning objectives of this module, module 3 the inverter, you should be able to explain the functioning of a CMOS inverter right, which means that if there is a transient input signal going from low to high or high to low you should be able to tell me how the output signal of the inverter will go.

Explain the voltage transfer characteristics of an inverter which means basically the V out versus V in when I sweep V in from 0 to V DD. You should be able to tell me what will happen to V out right, what regions of operation each transistor will go through what are the points of transition and so on.

You should be able to derive an expression for the trip point of an inverter, this is again a very very key point that you need to know. Ideally, there are you know there should be a very sharp transition when I go from 0 to V DD, maybe above V DD by two you want all signals to be recognized as logic high, below V DD by two you want everything to be recognized as logic low, right.

Unfortunately, this and that is what that trip point is signifies V DD by 2 is that sharp trip point. Unfortunately, in reality there is also a transition zone where there is an indeterminate region right which we will come to, but this trip point is a very key characteristic of this inverter, ok. If it is too close to V DD then you know need to take a long time to switch the logic high, if it is too close to ground and it will take a long time to switch to logic low and so on.

Then, you should be able to derive an expression for the delay of an inverter driving a particular load, then you should be able to derive expressions for static dynamic and short circuit power of an inverter with regard to power this is the only thing that we will be doing in the entire course. I will tell you what the short circuit power is, what dynamic power and what leakage power are. Same thing will apply to other logic gates, but beyond this we will not deal with power in this particular course, ok.

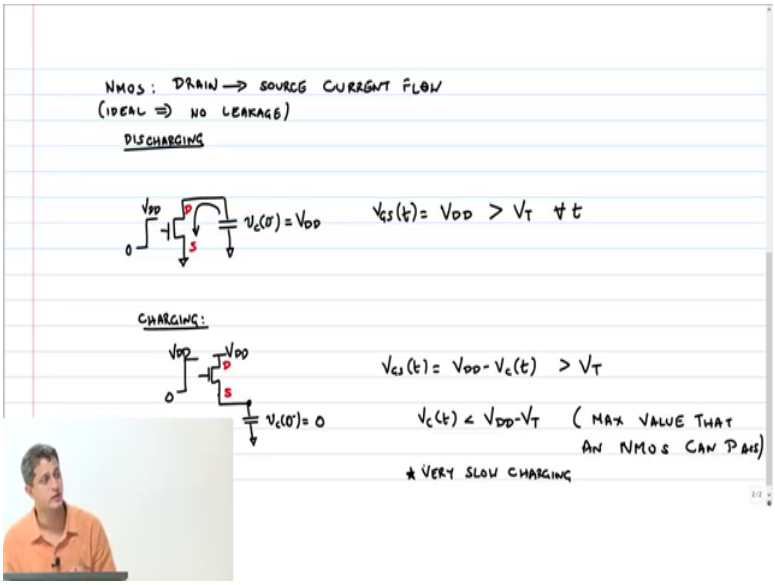
So, let us now get going logic gate as we know right for example, if I have an inverter driving an AND right, driving a OR and so on; I mean, these gates we are already familiar with, right. So, what happens is each gate right as you have seen now the input right to a transistor is basically to the gate right which means that you will see some capacitance at that node; in fact, there are capacitances in all nodes.

So, effectively this will have some load capacitance right, plus it is own capacitance right coming from the drain source and all that we will look at the origin of these capacitances. But, if I now want to propagate a signal like this through this circuit, this signal then has to fall, then this signal will also fall because the AND is non-inverting and then this is going to

sort of invert, right. All through, what you see is a capacitor is either being charged by the previous gate or a capacitor is being discharged by the previous gate.

So, we will first study in detail these two operations and figure out which transistor has to be used for which operation and the reasons for why we need to use them in that particular way, right. So, we will look at ok. So, now, let us just look at it very common it orally we have two types of transistors NMOS, PMOS and we have two types of operations charge, discharge. So, we have to look at all four combinations and figure out which is going to work for what, ok.

(Refer Slide Time: 07:00)



So, let us start with the NMOS transistor ok, I am going to first look at discharging because this we already looked at. What is the direction of current flow in an NMOS transistor? Drain to source current flow, ok. So, what do I have here, I have a capacitor which is initially

charged to V DD and then I am going to apply an instantaneous gate voltage to turn on my transistor, this we already studied ok, but I am just refreshing your memory in that with that. So, if I turn on this transistor then; obviously, this capacitor is now going to discharge, ok.

Now, here when we looked at this right, we were treating these our logic signals; so, this is actually 0, V DD, V DD, 0, right. So, when we propagate a logic signal through some logic gates we want the logic signal to swing all the way rail to rail from 0 to V DD, right. So, now, which means that when a capacitor is being discharged by the NMOS transistor, the hope is that it can discharge it all the way to ground, right.

So, let us see if that will happen here, ok. Of course, for delay purposes remember we looked at only discharging from V DD to V DD by 2 right, but for logic purposes I need to take the signal all the way down to 0, right. The delay is characterized by only by that point where the current was in saturation and all that stuff which is fine, but ultimately I need to discharge this capacitor all the way to ground, ok. So, let us see if that will happen.

So, before I now start tell me which is the drain, which is the source; top is drain, this is the source. Therefore, what is V GS of this transistor at all times, V DD; after it is turned on it is at V DD all through; right. Now, therefore, this capacitor can obviously, discharge all the way to ground right, why is that because as long as V GS is greater than V T, this transistor will be turned on and it will continue to discharge all the way together. Of course, this is also be asymptotic because after you come out of the saturation region transistor will enter the linear region which means now it depends on V DS.

So, as the capacitor is discharging V DS keeps coming down which means a current also will keep coming down and asymptotically it will come down, right. So, it will take some time to go, but eventually it will happen, ok; so, this is greater than V T for all times, this is the key thing, ok. Now, if I were to use the same NMOS transistor to charge a capacitor, I want to see what happens here, ok.

So, let us look at charging of a capacitor with an NMOS transistor. What is V C of 0 minus, 0 it is been capacitor has been discharged now, I am trying to charge this all the way to V DD,

right. So, therefore, this is V DD what should I apply on this gate again same thing right pulse going from 0 to be V DD instantaneously.

Now, what is the drain? What is the source? Which is higher potential? V DD will always be higher potential therefore, that has to be the drain this has to be the source. So, therefore, V GS of t is what? V DD minus V C of t, right. So, what happens is this capacitor keeps charging all the way and of course, current assume now this is an ideal transistor it means that there is no leakage current which means the moment I go below V T, the transistor just cuts off completely and there is no current to charge this any further.

So, let us assume there is no leakage for ok, this may with ideal transistor implies low leakage. Does not mean that this cannot be short channel and all that, I am just saying ideal means there is no leakage current, right. V GS less than V T means current is 0, ok. So, this as long as it is greater than V T, it will conduct. So, what is the maximum value of capacitor voltage that this can reach right, it has to be V DD minus V T.

So, if I use an NMOS transistor to charge a capacitor at most I can charge it up to V DD minus V T, ok. Now of course, if there is leakage current this will continue to charge, but that will charge. So, slowly that that is not going to be useful for me, it needs to happen quickly in the on current it needs to charge the capacitor to V DD forming, right. So, this is the maximum value that an NMOS can pass.

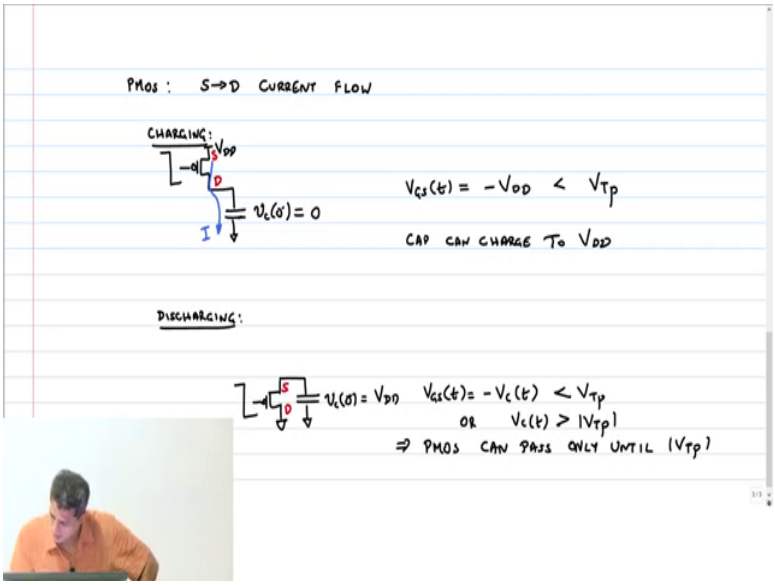
So, this guy is a switch that is trying to pass a high voltage unfortunately it can pass only V DD minus V T, right of course, if it is discharging then it can discharge all the way to ground. The key difference is in the discharging case the source was fixed at ground, V GS did not depend on the capacitor voltage. On the other hand when I am charging the capacitor V GS is depending on the voltage that is being charged, right.

Now, this is not just a problem of the you know this rail to rail swing right, it does not go to V DD minus V T; I mean, it does not go to V DD it stops at V DD minus V T. Apart from this look at the gate overdrive also as this capacitor is charging V GS minus V T is dropping which means that current is now even in that saturation region and all that my current is

actually dropping because it depends on V GS minus V T. So, the charging process is also ridiculously slow.

So, not only is it a logical problem I do not have rail to rail swing charging is also extremely slow, very slow charge, ok; any questions here. So, I did not define the drain and source is the most key thing that you have to do in this analysis, ok.

(Refer Slide Time: 15:27)



Similarly, let us now move to the PMOS transistor; current flows from source to drain ok. So, now, let us look at the same case I am going to look at charging first. So, this is going to be connected to V DD; so, PMOS transistor I am going to connect it to a capacitor like this and V C of 0 minus is 0. Now, what should happen to the input, ha you should go from V DD to ground, ok.

So, first before we start as usual which is a drain, which is a source? V DD is source and this is drain. So, which means that V GS of t is what minus V DD which; obviously, is less than the V T of this transistor, let me call it V Tp; V Tp is negative number right which is; obviously, lesser than that and therefore, it will be turned on always, ok. And therefore, this guy can now simply charge up in this particular way using this correct. So, PMOS charging no problem it can go rail to rail all the way to V DD, right.

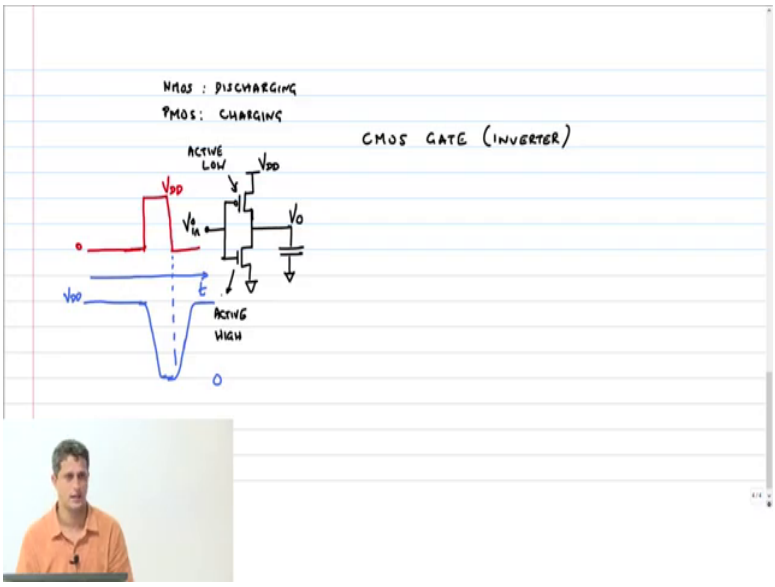
So, cap can charge to V DD, what about discharging? V c of 0 minus is what V DD and I am now going to connect this to a PMOS transistor of course, this is going to go to ground. Again what is the source what is the drain, top is the source the capacitor voltage is now the source, this is the drain. So, what is V GS of t? No what is the input where is it gone, it gone from high to low gate voltage is what? So, it is minus of V C of t as long as minus V C of t is as long as this V GS of t is less than V Tp this will turn all this will be on, right.

The moment that goes you are gone. So, minus V C of t should be less than V Tp or if I remove the minus sign from both sides what should happen to the inequality it will. So, V C of t should be greater than mod V Tp ok, because V Tp is a negative number which means that a PMOS can discharge a capacitor only up to mod V Tp.

So, the NMOS cannot take cannot charge a capacitor to V DD it stops at V DD minus V Tn, a PMOS cannot discharge a capacitor it will stop at mod V Tp, right. So, this implies PMOS can pass only until mod V Tp when you are trying to pass a logic 0 you cannot pass you can pass only up to mod V Tp. So, we will use this later in something known as a pass transistor, ok. Any questions here, clear? Great.

Now, what is the conclusion we have to discharge with NMOS transistors and we have to charge only with PMOS transistors. Any other combination is just leading to a either no rail to rail swing and also that will be very slow. Even in the case of PMOS remember, the V GS keeps diminishing with time and therefore, it becomes weaker and weaker and therefore, the delay is also going to be ridiculously bad, right.

(Refer Slide Time: 20:57)



So, what can we do with NMOS discharging and PMOS charging. So, I am going to construct my first logic gate in this course in the following way, ok. V DD this is my load capacitor that I want to charge or discharge, ok. Now, it turns out that I can just short these two guys and connect the same input to both of them, right. And other important observation note that an NMOS transistor is an active high switch. In this configuration and my input goes high to V DD, the switch will turn on and will allow discharging to happen right, on the other hand a PMOS is an active low switch, ok.

This is active high, this is active low because of this natural thing of you know I have to put an active high element in the discharge path and an active low element in the charging path, the CMOS gates are always inverting in nature, right because when this turns high this the output will discharge. The NMOS turns the input to the NMOS goes high, the NMOS

actually discharges the capacitor which means if the input goes high the output will fall and vice versa.

So, this is called a CMOS gate, right and of course, this is an inverter; why CMOS? It is complementary MOS you have NMOS and PMOS gates, ok. So, you will see in your tutorial that there are you know few other combinations which are not robust inverting gates, but they are also inverters in some sense clear, ok.

So, now let us look at you know I apply a signal which is like this or let me apply an ideal signals for now input is going from 0 to V DD instantaneously, ok. So, let us assume analyze both these cases. So, if my input is 0 right, let us assume that the input was 0 for long enough. So, what will which of the two transistor would have been on, PMOS should have been on and therefore, we charging circuit would have been on for long enough and therefore, the output should be exactly. So, this will be V DD, ok.

Now, I am turning on the input and switching it from 0 to V DD. So, what happens to the PMOS transistor, off right; what happens to the NMOS transistor turns on and therefore, it will now discharge it to that equivalent RC model that we discussed, right. So, there is going to be some sort of a delay here and it will come down like this ok, this axis is by the way time is V DD 0, 0 and V DD, right.

Now, exactly the opposite will happen if now the input happens to fall again here, right. This will now rise up further let me destroy it more accurately right and then at this point, this will again rise with some delay, right. Clearly when the input is 0 the output is V DD, when the input is V DD the output is 0 and therefore, this is very naturally a CMOS inverter, right. In fact, all CMOS gates are naturally inverting gate. So, you do not think of AND, OR gates, you think of NAND, NOR kind of logic in CMOS it is, ok.