Digital IC Design
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Lecture - 11
The PMOS Transistor

So, now we will move on to the PMOS Transistor.

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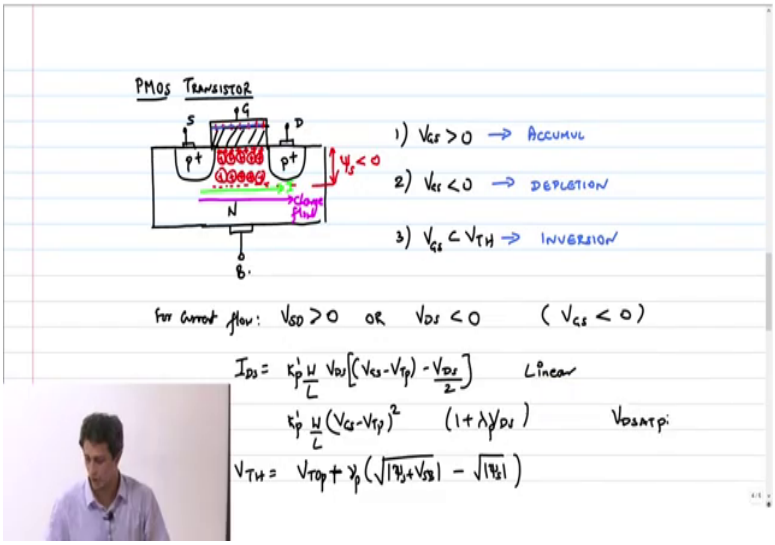

So, the PMOS transistor the structure is exactly the dual of your NMOS transistor, where I have diffusions which are P plus ok. These is my again my metal and oxide, the thickness will be the same for an NMOS transistor and a PMOS transistor right and this substrate is going to be N ok. So now, I could have gate, source and drain and this is my body. So now, let us

analyze the three cases; what happens when V DS is greater than 0 case 1, 2 V GS is less than 0 and 3 we will come to that. So, what happens when V GS is greater than 0? Yeah.

You will; you will attract positive charges here right and therefore, you will get negative charges out here right. Enough number of electrons and so on, you get negative charges there and which is again not very useful. And therefore, this region is what you are basically accumulating more electrons at the surface then what is there is the bulk. And therefore, this region now is called accumulation ok. So, the interesting region of operation is when all these positive charges become negative where, V GS is going to be negative.

And therefore, I start depleting the channel which means I am going to drive away electrons and leave behind immobile right; I am going to leave behind immobile positive charges like this. So, this will happen until the surface potential gets pinned right just like the NMOS transistor. So, you will have a surface potential that develops across this psi s; obviously, V GS is less than 0 so, psi s will also be a negative number right. In fact, if for psi is 0.25 volt for an NMOS transistor, typically this will be minus 0.25 volt for a PMOS transistor ok.

This is the convention that we are following right, you keep doing this at some point you are going to attract enough number of free holes at the surface and then invert the channel. What does inversion means? Strong inversion means that the concentration of holes at the surface is as much as electrons in the bulk right. And, then you apply your same derivation and you will get your current equation very nicely. The only important thing to note is holes are your charge carriers in PMOS transistors, while electrons with the charge carriers in NMOS transistors.

So, because holes are the charge carriers current direction and charge direction is the same ok. Charges always flow from the source to the drain, that does not change. Its only a direction of current that changes between an NMOS and PMOS transistor ok. So, my charge direction is from source to drain and current direction is also from source to drain. I will just say I and this is my magenta is charge flow ok.

So, if you look at this now compared to the source what should be the nature of the voltage I apply on the drain side? Should be a negative voltage because again current can flow only from high potential to low potential that does not change; NMOS transistor, all PMOS transistor that does not change.

If current has to flow from high potential to low potential and the charge and current flow from source to drain then; obviously, the source should be at a higher potential compared to the drain right. So, this for current flow V SD should be greater than 0 or V DS should be less than 0 ok. And, by the way just like the NMOS transistor V GS less than 0 is depletion region, depletion mode and V V GS less than V T. You keep reducing the gate voltage at some point you would have inverted the channel, that point is known as the threshold voltage.

If you go further then you are going to get more and more electrons at the surface, that can constitute I mean holes at the surface that can constitute current right. This is what is this mode of operation? Inversion and the convention here is already with sorry V GS, V GS should be less than 0. So, clearly you are seeing a trend here that all quantities are becoming negative ok, yeah no. So, the like I told you earlier even for the NMOS transistor, if I give you just the device and ask you what is the source, what is the drain I have no idea; you have to tell me what potential you apply.

Once you apply the potential in a PMOS transistor the higher side is the source because that is sourcing the charges and the drain is draining out the charges. Its just a convention and a definition; by definition of course, if you I can reverse this potential and apply higher there, by definition that will become the source that is all ok. Yeah.

So, the it turns out that the drain current equation does not change ok, my ID I DS will be K p prime W by L into V DS into V GS minus V T, I will call it V TP if you want minus V DS by 2 this is for linear ok. And, saturation will be K p prime W by L V GS minus V TP the whole square ok.

Similarly, the equation for threshold voltage will also not change, it will just be V T naught p right plus gamma times root of this is where the mod is important, because psi S becomes negative you have to put root of mod of that ok. Psi S plus V SB again it does not change minus root of mod psi S ok. And of course, if I go ahead and now you incorporate all the short channel effects then this guy will become into 1 plus lambda V DS lambda p into V DS right and then there is a gamma p also here ok. How many parameters do we have? Right.

And, similarly I cannot just keep increasing my keep reducing my V DS negatively and achieve more and more current. You have a saturation velocity there as well and therefore, you have a V D sat p even in that case ok.

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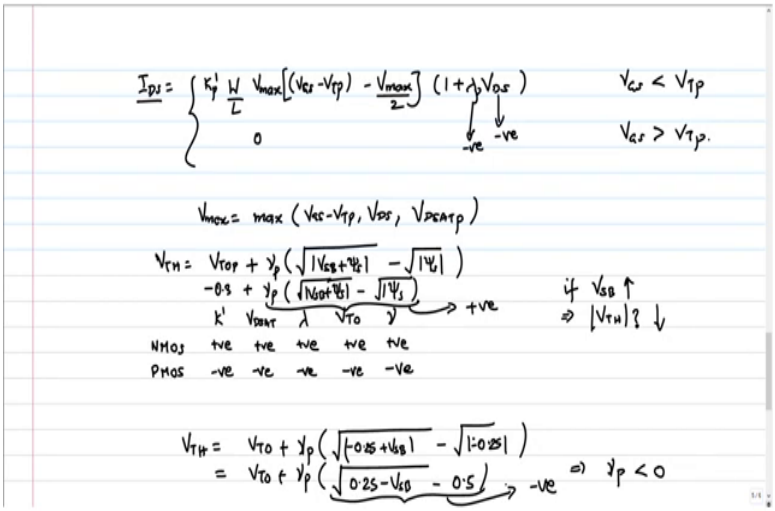

So, let me just write the unified current model for a PMOS transistor I DS will be K p prime W by L into V max ok, I will tell you what that is; V GS minus V TP minus V max by 2 into

1 plus lambda; lambda p into V DS ok. This is obviously, if V GS p or V GS is less than V TP ok. And, it is 0 if V GS is greater than V TP, there is no current through the PMOS transistor if V GS is positive or has not yet inverted the channel ok. What is V max? Is simply going to be maximum of V GS minus V TP V DS and V DSAT p ok; I am not writing it in terms of mod because its little bit confusing; yeah where no.

So, here I am not asked you to do any mod V DS is whatever V DS value, if its minus 0.2 volt you substitute minus 0.2 volt in this. Yeah. You just put negative values, exactly whatever mathematically whatever this equation says you just follow it that is the idea; that is why I am not trying to write this in terms of mod. Because, that becomes confusing especially when you bring in the threshold voltage and all that.

So, what we will do now is to simply compare what the sign of each of these parameter should be. We had 5 parameters that define the level 1 spice model for the NMOS transistor, we have similar five parameters here. So, I will just write that on one side K prime, what is K prime then V DSAT right, then lambda then V T naught and gamma. These are the 5 parameters for the level 1 spice model.

We had two transistors NMOS, PMOS and let me also write the threshold voltage equation here V TH is V T naught P plus gamma into root of mod V SB plus psi S minus root of mod psi S and there is a gamma P here. So, in an NMOS transistor all these parameters were just positive ok. We understood why each of these parameters for example, why gamma should be positive because if you increase V SB threshold voltage should go up right and therefore, gamma has to be a positive number right. On similar lines I want to analyze for a PMOS transistor, what this value should be, should be positive or negative; exact value I am not worried about ok.

So, let us start with V T naught, it should be a negative value right because as I lower my V GS at some point I am going to invert the channel there right. So, therefore, this has to be a negative value. What about V DSAT? Negative value right because, the current will flow only if V DS is negative right and therefore, that also has to be the even the saturation value has to be a negative value right. These are pretty simple ones. Now, what about lambda?

What should happen to lambda? What should be the effect of lambda? Positive. Why ok, if its positive it tell me why you should be positive, it is negative tell me why it should be negative? Yeah.

Negative, because V DS has to be negative, only then you will have current. And, with some lambda being introduced that current should go up that is what you want, if the channel is brought closer, then the current mod of the current should go up the magnitude or the current should go up. But, that can happen only when V DS is negative, remember this is just a convention. The drain source voltage has to be negative only then it can be you can have a current and therefore, lambda also has to be a negative number. Why? Because, this is a negative quantity.

Only is this is also negative, this 1 plus lambda V DS will be a positive term that increases the magnitude of the current. Are you; are you following me here? Right. What about K prime? Yeah, positive. So, remember I just look at the equation I wrote very carefully, I wrote I DS equal to something.

I did not say I SD equal to that, if I DS is equal to something what should it be? Negative, because the current will flow from source to drain, but I am looking at I DS therefore, it is not a physical thing where this term has to become negative. Just to make my I SD I DS my K prime has to be a negative number right. And therefore, this also will be a negative number ok. We have solved 4 parameters pretty simply. What should happen to gamma? Why? So, let us go back to our.

Student: (Refer Time: 17:45).

Yeah for it to; it should come.

Student: (Refer Time: 17:52).

Yeah, but what is decreasing threshold voltage?

Student: (Refer Time: 17:59).

No, but decreasing threshold voltage for a PMOS means what? Decreasing mod of the threshold voltage yeah or I am increasing, I am adding a delta to the V T right. But, you are right its basically decreasing the mod of the threshold voltage, it is easier to invert the channel if the body is negative right, correct. So, if V SB increases; if V SB increases what should happen to the; what should happen to the V TH of my PMOS transistor or what should happen to the mod V TH? Let us ask a simpler question, it should decrease right V SB goes up V T V TH mod V T it should decrease.

You agree? All of you agree with this? Its opposite of an NMOS transistor, if V SB goes up the threshold voltage for an NMOS goes up right, but for a PMOS transistor it should mod of the V TH should come down. What does mod of the V TH come down mean?

So, in this equation let us say this is minus 0.25 volt or minus 0.3 volt ok. Then plus gamma P into something V SB is going up, if V TH has to mod V TH has to come down what would happen to this second term? It should be positive right yeah. So, root of mod V SB plus psi S minus mod psi S this should be positive. So, if V SB goes up and gamma P into that term has to be positive what should be the sign of gamma P? Yeah. Why?

Student: (Refer Time: 20:38).

That is the catch here right, it may appear for example, that V SB; if V SB goes up root of mod of V SB plus psi S also goes up, that is not true because a psi S itself is a negative value ok. So, the way you should analyze this equation is write this as V T naught plus gamma p into let us substitute a value for psi S minus 0.25 plus V SB, minus root of mods minus 0.25. V T naught plus gamma P into this will become, what is it? 0.25 minus V SB, I assuming V SB is less than psi S mod psi S. You cannot arbitrarily increase V SB beyond 0.25 volt 0.3 volt and all that, some small deltas is acceptable minus 0.5.

So, now if V SB goes up then what is happening to root of 0.25 minus V SB? Its becoming less; that means, this term will become negative. If now gamma P into that term has to be positive so, that the V TH actually comes down mod of V TH comes down implies gamma P has to be less than 0.

And therefore, this also has to be a negative quantity, is very nice because all positive terms parameter values for NMOS transistors, all negative parameters for PMOS transistors. But, you should know why they have to be negative and there are some caches like this; especially for PMOS substitute values and remove the mod otherwise that analysis will go completely wrong ok.

I can leave it to you as an excise to go back and try out what happens you know how you can do this back gate analysis. If you apply a body voltage which is negative what should happen to the threshold voltage all that, just try it yourself and see that the equations tie up now as an exercise. If you have any doubts we can discuss it in the next class ok. So, any other questions with regard to the PMOS transistor here? Yeah.

Student: (Refer Time: 23:41).

Yeah.

Student: (Refer Time: 23:45).

Correct.

So, you have to consider the maximum of these voltages which is for the negative, yeah no not magnitude absolute value, not absolute the value actual value.

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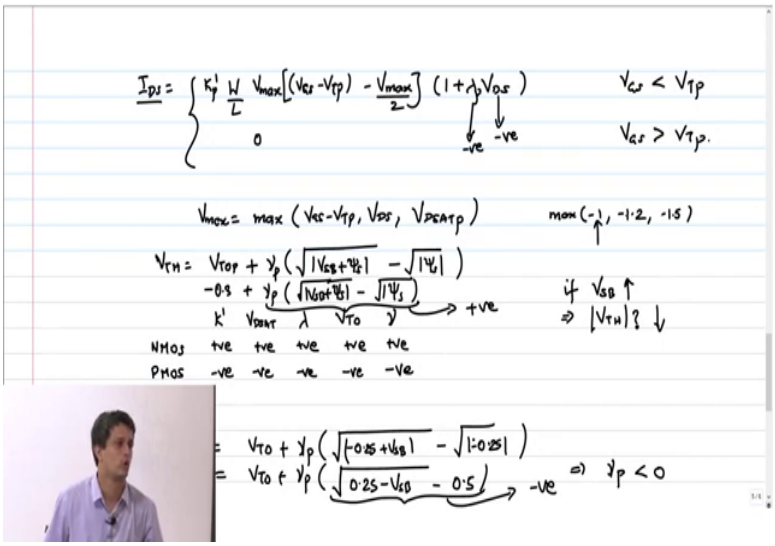

So, you are going to do if I substitute your values it will be max of minus 1 minus 1.2 let us assume that this is minus 1.5 or something; V GS minus V T right that is. Which is a maximum in this? Yeah, that is value that you have to take or you or you have to do min of mod of all these values ok. But, I think that is actually very dangerous better deal with actual numbers ok.

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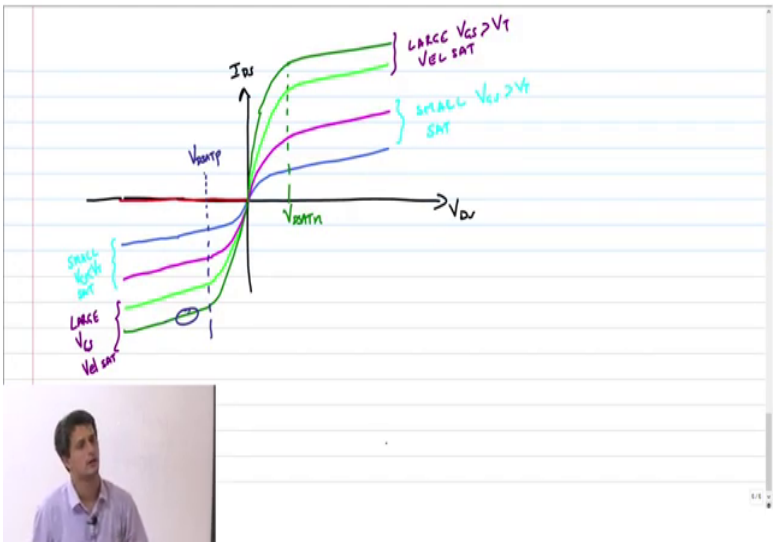

So, let us look at a few plots V DS versus I mean I DS versus V DS. In which quadrant will the PMOS current be? Which of the 4 quadrants will the PMOS current exist? The third quadrant right, V DS has to be negative and I DS is also a negative number right. And therefore, these plots of is a V GS is not enough to turn on the transistor; obviously, the currents will just be 0; no big deal about that.

As you start increasing V GS you will have this kind of a current right and if I increase my V GS slightly further, then it will remain it could be in saturation region for low V GS. For low V GS values it could be in saturation, it need not go into velocity saturation mode. But beyond a certain point of course, everything will enter velocity saturation and it will start looking like this ok. This is small V GS; small V GS of course, less than V TP only then it will conduct right.

These are large V Ts, large V GS sorry and it can get velocity saturated right. This will end up in saturation region ok. Similarly, you can plot the I D versus V GS again that will be in the third quadrant ok. So, your question really will be somewhere here this your V DSAT right magenta what is the color I have not used this. This will be your V DSAT value for V DSATP will be somewhere here right. And if your V DS is large enough; that means, it is negative then of course, the current will be somewhere here in, this particular region which gets determined by the V DSATP ok.

So, that equation I have written there is mathematically consistent, just substitute the values and you will get the also; do not do any conversion from all this that nothing ok. Which one? This one? This is V DSAT because at the saturation value, it is the current is saturating right. So, you look at the sim the corresponding currents for the NMOS transistor that I draw here right. The magenta is again it can be in saturation right, then and this will be your V DSAT right n.

The current is saturating at a particular V DS value, it does not increase any further which depends on the V GS value also. If it saturates earlier then that will basically dominate and you will get a saturation current otherwise you will get a velocity saturated current. Clear? Not convinced? Why? You agree with.

Student: (Refer Time: 29:33).

That is V DSAT yeah velocity saturated drain source voltage, the drain source voltage at which the current becomes velocity saturated ok. To just fini corresponding thing this is small V GS greater than V T and it enters saturation region. This guy is large V GS greater than V T and it enters velocity saturation and of course, the slope is basically your because of lambda P right. Clear? Ok.