Digital IC Design
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Lecture – 10
Substrate and Gate Leakage

So, last class we stopped with the discussion on sub threshold Leakage, right.

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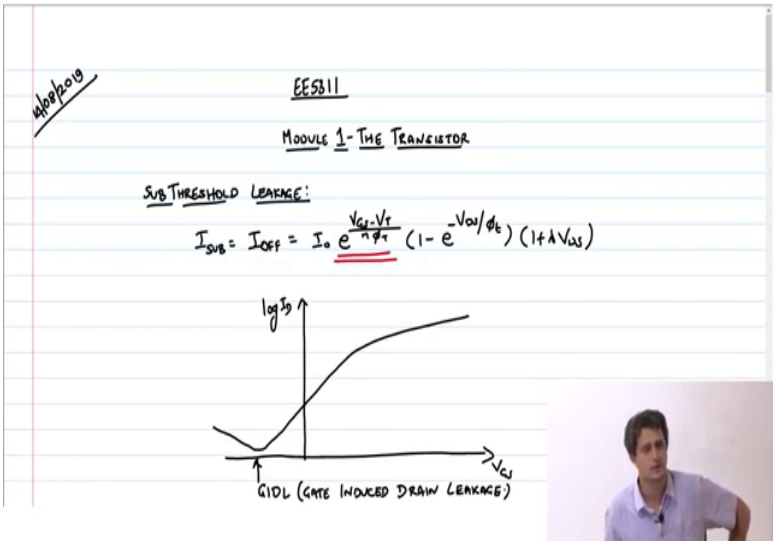

So, we finished with sub threshold leakage; we said that the NMOS transistor can behave almost like a BJT, because now the drain and source are so close to each other that the channel is so thin right that it behaves like a base. And if you remember for BJT action, the base has to be very very thin, right. And therefore, you do have some current flowing through

between drain and source even when the gate voltage is below the threshold voltage of the transistor, right.

And we said that the most important thing was that sub threshold leakage also referred to as I OFF many times, when you say off state current. Today we will see a couple of more you know, leakage mechanisms; but by default if you say I OFF it is these sub threshold leakage, ok. This is some I naught e power V G S minus V T by n phi T right into what 1 minus e power minus V DS by phi t into 1 plus lambda V DS, right. This was the equation for sub threshold leakage. The most important part is really this exponential dependence on V GS and V T, ok.

And as I said as a designer if you look at the plot of log I D was this V GS, it will look something like this ok. And if you keep reducing V DS further it will keep coming down, at some point it will go up and this point is basically because of the introduction of something called griddle, gate induced drain leakage. I would not even go into what this leakage mechanism is this; but the only thing I would like to say is that you can not indefinitely reduce V GS on a negative value and expect that sub threshold leakage will keep coming down.

So, there is a point at which you can up to which you can go, beyond that sub threshold leakage may come down; but other leakage mechanisms take over right, which is basically called gate induced drain leakage, ok. This is what are designer should be aware of, this is where we stopped last time.

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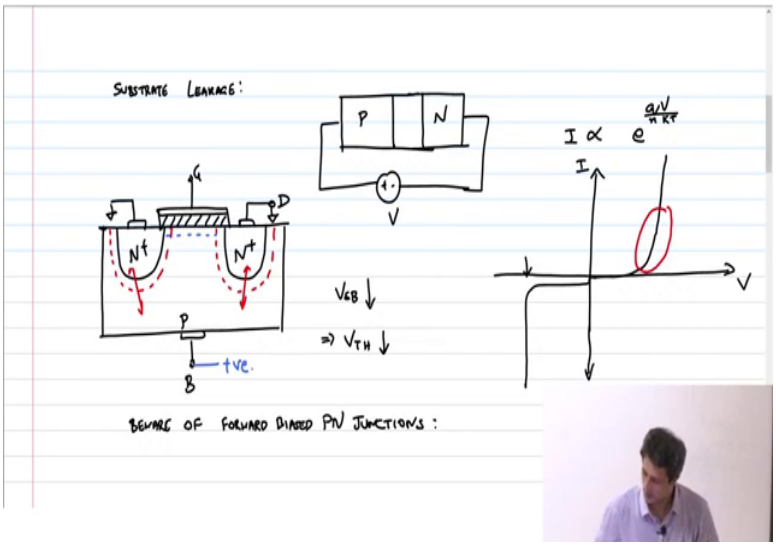

So, now let us proceed with a few more important things. So, basically you have substrate leakage. So, before we go into substrate leakage, if you have a simple P N junction right; what happens, if you plot the this is P and this is N and if I apply a voltage like this ok, then the leak the current through the P N junction is some I naught e power q V by n K T right similar to whatever we had for sub threshold leakage, right. I just say let us leave it at this, proportional to this ok. I am not even going to worry about all of this.

It is proportional to this; which means that, there could be an exponential current with the forward biased voltage that you are applying. And of course, if you look at this I versus this V curve; this will be like you know after some cutting voltage it happens. And this is sort of some you could have some negative voltage and then you can have a huge reverse bias leakage, breakdown current that will occur,.

So, these points are important, because even if you reverse bias your junction; you should remember not the reverse bias it too much, because beyond that you can have a breakdown

current, right. So, we are going to apply these concepts now to an NMOS transistor and see what happens, what are the conditions under which we can operate the device safely. N plus N plus oxide is a P substrate; now we said that I can have a body contact here, I can have a gate contact here, source could be grounded, drain could be some V D, right. So, I will call it D, ok.

Now, what happens to the threshold voltage of the transistor if V S B comes down, if V S B decreases? V S B comes down implies V T H will decrease, right. So, if V S B is coming down it means that V B S is going up right; V B S is a positive value. So, if you apply a positive value, then you can get some either electrons or some depletion that happens and therefore, threshold voltage will come down, right; this is the back gate effect that we have abstracted out. So, this is good, you could have a larger current in the transistor by doing this ok; but what happens if V B is connected to some positive value. So, remember that this source is now grounded, ok.

And V D also could be grounded when it is not being used; I mean typically it would either be ground or it could be V DD right, in digital technique. So, for now let us assume this is also V DD also grounded. So, now, this is my depletion region. So, what you see is both the source and drain junctions they are going to form P N junctions with a substrate, right. So, there is one P N junction here, another P N junction here; and by connecting the body to a positive voltage, you are forward biasing that junction. What does forward biasing the junction mean? It means there is an exponential increase in current as shown here in this curve, ok.

And therefore, if you are slightly increasing it, maybe 10 millivolt, 20 millivolt, maybe even 100 millivolt sort of ok; but be prepared for the extra leakage that is going to come up of. Of course, you cannot take it to like you know 200 millivolt, 300 millivolts; then the leakage will be uncontrollable after that, right. So, you do not want to actually forward bias any junction in the transistor ok, rather than you do not want to; I should say you should beware of forward biasing any junction in the transistor, ok. So, that is the right thing to say, beware of sorry forward biased P N junctions.

The reason I say this is, using the body to adjust the threshold voltage is a valid technique and later you might try to connect this body to V DD and expect that the threshold voltage will come down and therefore I can do something; well that is not possible. Because the substrate leakage will kill you in that case right, you should be very very careful about which junctions are getting forward biased and what the magnitude of current is.

You can use simulations to figure out what those currents are right. I do not want to, it is not possible to come up with a back of the envelope calculation; because this is really a second order effect ok, but you have to be very careful and watchful about this leakage mechanism as well.

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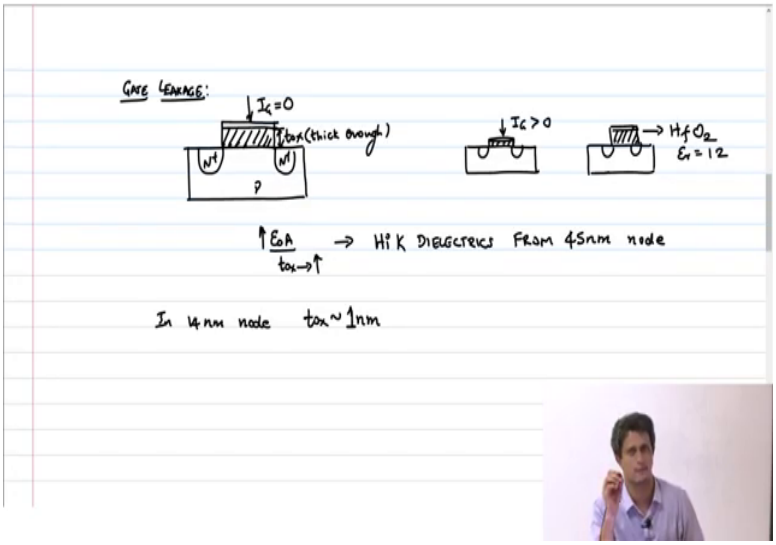

So, the next leakage mechanism that we will discuss right or as a designer that you should know about is gate leakage, ok. So, when I had my long channel device, I had my N here right

N plus N plus P this was my metal; I had a rather thick gate oxide, ok. This was my gate oxide, right. And it was reasonably thick; thick enough until about 45 nanometer. What does that mean? It means from 180 nanometer, 130 nanometer, 90 nanometer, 65 the transistor started shrinking.

Why did this shrink it? So, that you gain power, you gain area, you gain delay everything right by bringing the drain and close together, closer together we would achieve greater speeds with that you also got lesser area. You also got lesser power and of course, why lesser power, because if I bring these two junctions close by, I have to reduce my supply voltage also; otherwise the junction will break down.

In all this you were actually able to gain significant amount it, really there seemed to be nothing which stopped you from scaling, it was all win going from 180 down to 65 actually, right. Somewhere at 130 the sub threshold leakage started coming in and became a reasonable concern, 90 nanometer it became a real concern; but up to 45 nanometer you could just scale this device and obtain a new device which would just look like this ok, N plus and this would be my oxide thickness, there was no problem.

The problem is, if you continue to do this beyond 45 nanometer, 22 nanometer and so on what happens is this gate oxide becomes so small right, that quantum mechanical tunneling can occur across the gate oxide. So, if I ask you what is the current that is flowing into this gate of a NMOS transistor, what was your answer earlier? I G is 0, because that is actually going straight into an insulator.

Unlike a BJT where the base current is very very small, right and that is what is going to result in a larger emitter current, collector current and so on. Here the gate current is very very very is negligible, is 0 in fact, right. If you scale the device, then this current started going up; I G became greater than 0, this is purely a quantum mechanical effect it cannot be explained through classical effects, right. The wave function of the electron would sort of go into the oxide and there is a finite probability that the electron will be found on the other side of the

oxide as well. And this forms a significant amount of current, if you just blindly skip scaling your device.

So, what people did was? They did it, they need to do something to prevent this right; because your NMOS transistor the greatest advantage is this gate current is 0. Recent insulators you do not have current flowing there at all ok, you will see the advantage of this later on. But the moment you break this assumption, lot of things actually break down. So, people had to do something to stop this. So, what people did was they wanted to increase the thickness, right.

Now, if you increase the thickness, then your capacitance goes up; which means that. the gate control actually comes down, right. So, they had to do something where the capacitance remain the same, but my thickness still went up; so that the quantum mechanical tunneling sort of came down. You wanted to move this to a similar device right; small device like this, but with a I am drawing it slightly exaggerated with a larger gate oxide, ok. What do you want to do? You want to do epsilon not A by t o x, right. To remain the same after increasing the thickness, how do you achieve that? Yeah.

So, what is the other parameter you have, if you increase your oxide thickness and you also increase epsilon naught by the same factor; then the capacitance would still remain the same, right. And that is why people started into introducing H i K dielectrics from 45 nanometer onwards, 45 nanometer node.

What is H i K dielectric? You are just instead of using silicon dioxide as your oxide; you introduce some new materials which gives you a higher permittivity, relative permittivity and the material that was used is hafnium oxide. It turns out that you cannot put any material there, because it has to now gel with silicon very well; there has to be very little defects when you go from silicon to hafnium oxide and so on.

So, now the gate stack right has become very very complex, it is not just hafnium in fact. In fact there are many more materials, so that you can smoothly go from silicon to this other material, ok. So, this allowed you to get an epsilon r of about 12; relative permittivity of

hafnium oxide is about 12. So, therefore, I could increase my gate oxide thickness by a factor of 3 compared to silicon which is 4 right; epsilon r is 3.9 or 4.

So, by a factor of 3 I could increase the thickness of my gate oxide; wherein I have killed quantum mechanical tunneling now, because that purely depends only on the thickness, right. But my capacitance has still remained the same ok; but does not mean that this is very very small, because in 14 nanometer the oxide thickness typically is 1 nanometer.

In 14 nanometer technology node let me say t o x is approximately 1 nanometer, ok. So, again the scales is very important; when we say thick, thin and all that even with hafnium oxide and all that, we were able to come to about 1 nanometer, ok.

So, they have continued scaling after introducing hafnium oxide in 45, they have continued scaling further and brought it down to 14 nanometer where it is oxide thickness is about 1 nanometer, ok. So, typically as a designer now you do not have to worry about gate leakage so much unless you are doing some you know non volatile memories and stuff; wherein you can you introduce defects and stuff like that when the gate leakage can go up. But you should be aware that this could be a potential problem and you cannot take it for granted that the gate current is 0 ok.

Any questions? Yeah without, no exactly; so it turned out that even in 45 nanometer, you had to bring this. See the tunneling is also functional voltages, right; how much barrier you need energy to cross those barriers. So, in 14 nanometer you have also been able to bring down the supply voltage; from 1.2 volts or something in 45 nanometer you would have brought it down to 0.8 volt. So, therefore, you can bring the thickness down little further. So, it is not just the dimensions at scale, also you supply voltage that has to scale. So, therefore, it is still sort of, yeah ok.

So, with that we have covered almost all the short channel effects that you should be aware of; wherever possible we have accounted and you know incorporated those effects into our level one spice model, right. Of course, we have not incorporated gate leakage, in those

equations we do not know, we really do not care also; you can use the simulator to handle those special cases.