Transmission lines and electromagnetic waves
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Lecture – 01
Transmission lines

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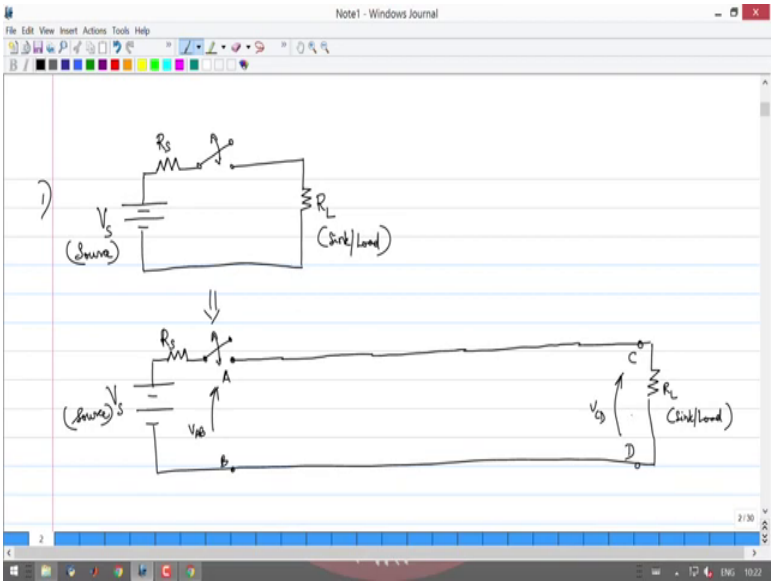

Ok So, we will begin by starting with the most elementary circuits that we would have started with an electrical engineer. We start with DC circuits, which have a source that is represented by a battery ok. It has some series internal resistance associated with it right. So, we can mark this as V source. This is the series internal resistance of the battery itself.

Let us assume that there is a switch and there is a wire that is connecting it to another resistor. This is probably one of the first circuits that we come across in electrical engineering. We tried to learn Ohm's law and the loop Kirchhoff's voltage law extra.

So, I will mark this as R_L and I will mark this as a switch which opens and closes ok. You can make contact or break contact depending on the time.

Now, when we look at this circuit, we can identify that this part is a source, the other part is a sink or a load and the part in between that connects them is what we are going to focus on a little bit. These are going to be the wires. Now, if we were to close this switch ok, we would expect that the there is a path for the current to flow and the voltage is going to be divided between this resistance R_S and this resistance R_L.

And we write down Ohm's law and Kirchhoff's voltage law for this, but one of the things that we do not do is when we treat this as a basic circuit, we are not putting some important information over here. So, to illustrate that, I will redraw the circuit in a slightly different way to just make you understand where I am getting it right.

So, I will draw the same source, with the series resistance which is internal to the battery and I am having a switch that makes or breaks contact. But, drawing a very long wire to connect this resistor. So, I will mark the quantities once again, source voltage, series internal resistance, a switch that opens and closes and then, we have sink or a load all right. Strictly speaking, in low frequency circuits these wires would act like short circuits.

So, the lengths are typically not at all mentioned and you do not get a feel for them when you are looking at a circuit diagram. For all we know the source could be placed very far off from the sink all right. So, there is a difference between these two circuits. Once you start incorporating the dimension of space inside your circuit diagrams and the question is when is it important and when you can avoid using space inside your basic circuit diagrams all right.

Now, when you have an abnormally long wired connection like this in your basic circuits, a question that crosses the mind is suppose we close this switch, a voltage will start appearing at this point and we marked this point with some coordinates all right.

The voltage between the two wires at this point all right. So, we can mark those to be AB and the load coordinates can be marked as BC or CD right. At the instant when you are closing in low frequency circuits, the assumption is that the voltage V_{CD} V_{AB} is going to be equal to the voltage V_{CD} That is the assumption that you make in your low frequency circuits.

But we know that no signal including the fastest signal that we know just light can travel at infinite speed. There has to be a finite speed for a signal to travel from one place to another place ok, which means that at the moment when the voltage at V_{AB} is non zero immediately after you close the switch, if your wire is very very long, then, the voltage across the point V_{CD} all right is going to be different, which means that between the 2 edges, we are going to be having a difference in voltages and this has to be considered.

And when do we consider and when do we not consider is the question that we are going to be answering now all right. So, we already know that if your wires are going to be extremely long, you will have to start to consider the effect of space. You will have to start to consider the effect of time, because of a finite velocity as associated with the signal.

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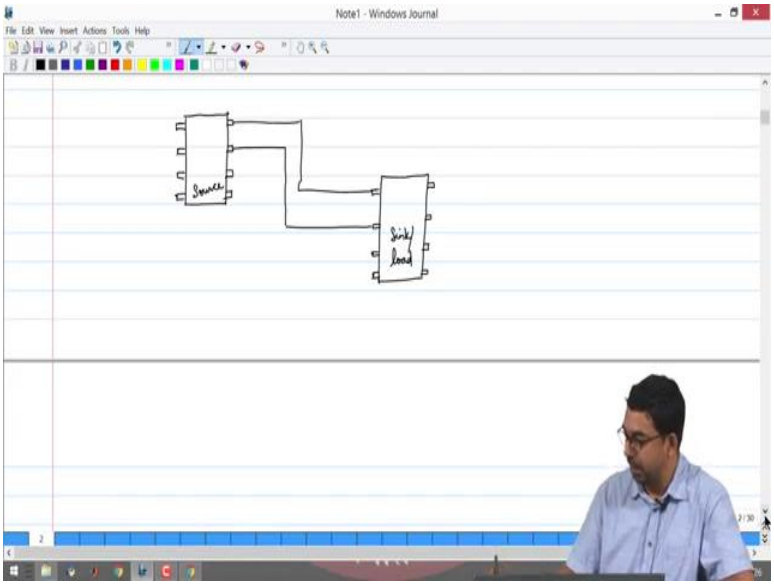

Now, when does it become important? All right. Suppose, you are going to be having a PCB board, which has some pins. So, this is an IC on a PCB board. It has some pins and I have another IC ok. And let us say that now this is going to be a source right. And let us say that this is going to be a sink or load this information is traveling from left to right over here. There could be some interconnections between these pins all right. Now, there are also many other ways the pins can be connected.

For example, you can loop all right, you can have a ground pin that is looped which means that you will be having something over here, which will be coming to this side this is a loop. So, it forms a ground pin. This could also be a ground pin, but they are on the same layer of the PCB. So, you have a current that will flow on the top line and complete the circuit through the bottom and this is known as a loop.

Usually, a loop is avoided in an integrated circuit design. So, what they do instead is they have a ground plane below the PCB board and the ground is usually connected by vias so that you have the current flowing on the top layer of the PCB and the return path is usually at the bottom layer of the PCB. This could be taken as one particular example right

Now, in this case we are having two different lines. It is also possible that the two different lines could have two different lengths all right. If that is the case, this circuit needs to make a decision based on the inputs at some instant of time. So, a knowledge of the delay between these lines, is going to be important. If one of the lines is going to be shorter than the other line, you will need to be aware of it to make a quick decision first.

Even in the simplest case when you are using logic gates, for example, in nand-gate, an or-gate extra, the assumption that you make is both the inputs occur at the same time across the 2 pins, but it is quite possible that the signals will appear at different slightly different instant of time ok.

So, we are going to consider cases, where this length and the time delay are critical alright and it seems that there is a way we can figure out when it is critical and when it is not.

So, we will go back to a circuit that we have drawn right and we will try to just make a fine distinction as to when it is critical and when it is not ok. So, most of the communication happens in terms of frequencies that means, you have a periodic signal instead of a simple switch that is closing and opening right.

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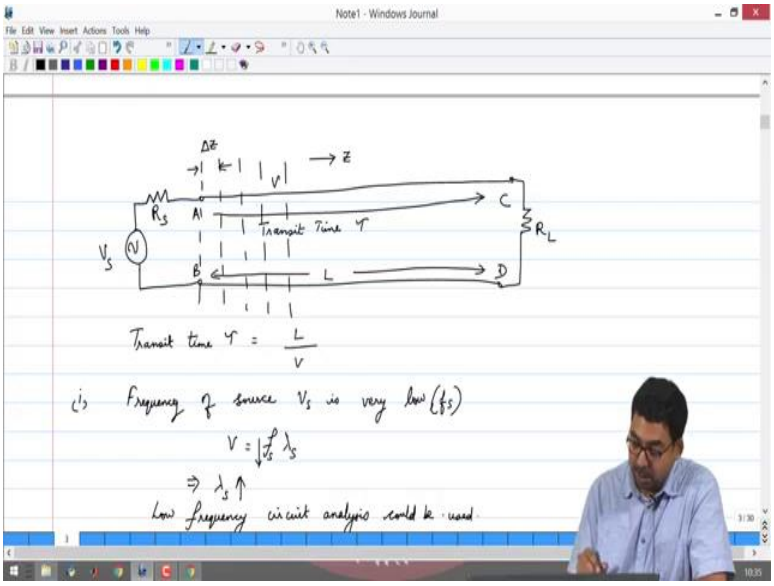

So, we can start by using an AC source instead of a battery. It has an internal resistance ok and then, you have a long interconnect connected to a load resistor.

So, in this particular case we already know that the signal velocity is not going to be infinite due to physical constraints right. So that means, that there is a finite velocity with which the signal is going to travel and that means, that we have to talk about some time that the signal takes to go from AB to CD, we call this as a transit time all right. And it's usually represented by the signal velocity, let us say that it's V ok.

And since this is a sinusoid, we can expect that between the points AB and CD, there is a good chance that there is a phase difference ok. Now, usually when we think about phase difference

we only think between 0 and 2π, but one has to understand that $4\pi, 6\pi$ are also phase differences, just because they are multiples, you do not actually observe them.

But there is actually a delay all right. So, there is going to be a phase difference between the signal that is coming at AB and CD.

Now, in conventional circuits either when you deal with dc circuits like what we had planned right, what we had begun with or in AC circuits the assumption is this is shorted. So, the voltage drop across AB and CD are identical, then you can use your conventional circuit class which is Kirchhoff's current law and voltage law.

In this particular case, if you try to apply KCL because your wire length is very long, you will start having drops across your short circuits which will violate your basic input-output criteria.

So, the approach to do a circuit analysis with lines that are long or have transit times that are large is by using what is known as Transmission line theory. Now, for the first time in the circuit diagram, we are adding some notations. Let us say that the length of the shot circuit that you are seeing is L. So, previously a short circuit diagram did not have length marked on it, never. Previously, it did not have time marked on it, previously, it did not have velocity marked on it ok.

Now, we are marking some more quantities and we can say that the transit time is tau and it is simply the length divided by the velocity V ok. Now, there are some cases that we have to look at ok, if the frequency of source V_S is very low.

If the frequency is very low ok, that means, we can say that your velocity is going to be the product of your frequency of the source fs. So, let us say that this is ok and consequently, the signal now has a wavelength lambda s and the relationship between the velocity and the wavelength is the velocity is equal to frequency times wavelength ok.

And if your frequency is very low all right, it means that the wavelength is going to be really high ok. It also means that your signal is going to be, you know, not showing any significant phase difference between the points AB and CD right.

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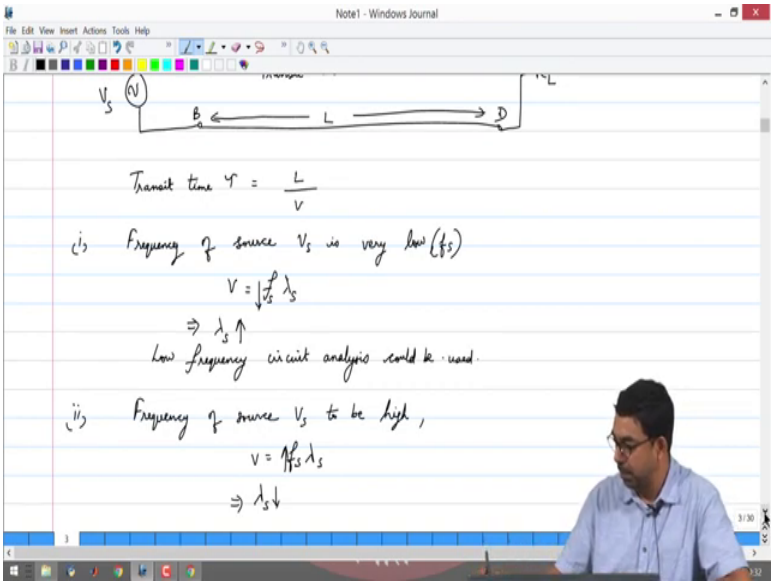

So, in this case one can always use low frequency circuit analysis right. However, if you are having the frequency of source V_S to be high ok, then you can write down the velocity is going to be

$$v = f_s \lambda_s$$

and f_s is going down, f_s is going high actually, I am sorry.

It implies that your wavelength is going down, that means, it can probably fit multiple waves within the same line all right and it is quite possible that you will have an enormous phase difference between the points AB and CD in your circuit diagram.

Now, in this course we are going to be focusing on the second case which is going to be high frequency circuit analysis all right and we are going to not invent a new theory for it. We are going to see how we can take the existing theory for low frequency circuit analysis and actually apply it for the high frequencies circuit analysis as we want in this course ok.

So, one of the approaches that we could take is divide this into a number of small regions right. So, you could always mark this to be some small sections all right and if we call this direction with the coordinate z, you can say that we are uniformly gridding the wire with a spacing of Δz ok.

And the choice of Δz is such that there is no phase difference or no time delay between the left hand side and the right hand side of the third section of the wire, it's really tiny. So, the delay is really really tiny. If that is the case, for each of these sections you will be able to apply low frequency circuit analysis or Kirchhoff's current law. So, that is the approach that we are going to start with.

But the question becomes non trivial when you look at it as even though if you divide it as sections ok, and even though we have considered a short circuit, there is actually a delay right. So, in this particular case I have not drawn any resistance for the wires. These are short circuits, these are ideal circuits. I mean ideally interconnects and you do not have any resistance connected to it, but there is a delay all right.

So, we have to explain this delay and from low frequency circuit analysis, we already know that we can use R_C, R_L and usually R_C is considered to be a time delay and R_L will also give a time delay which gives us a hint actually that there is more than simple wire present over here ok.

You have to account for this delay by making use of some L and C all right and we also learned in our earlier circuit analysis courses that R_C is known as a time constant ok. If you do not have any resistance, your time constant will vanish, that means that you need to have some small resistance present in your circuit all right to begin with.

Then, if that is the case, what will the circuit model for each of the small sections look like and what are the approximations that we can make to make our solutions a little bit easier?

Now, this is a wire carrying the wire I mean carrying current on the top a wire carrying current in the bottom all right and we started with a specific example where we are having say 2 ICs on a PCB that are interconnected like this and the ground plane is below ok.

If this is the case, we can say that the wire is carrying some current that is time varying all right. It is going to have some self-inductance, obviously. The wires are spaced apart all right and in the case of your PCB, they are present in the top and the bottom layer separated by a dielectric. They resemble a capacitor in the cross section.

So, there is a capacitance that is coming into the picture and there is also some small finite resistance associated with copper traces that goes on PCBs right. So, this resistance is going to be present along the wire and no dielectric is ideal. So, even though you have a trace on the top layer of the PCB and a ground plane at the bottom of the PCB, you cannot apply infinitely large voltage. There is going to be some breakdown at some point and even if you apply sufficiently small voltage you cannot say that the dielectric is ideal. It is going to have some small value of current trickling down from top to bottom.

So, there is a tiny value of resistance which is present there. So, by making use of this analogy, we can start to build some models which are known as phenomenological models ok ok.

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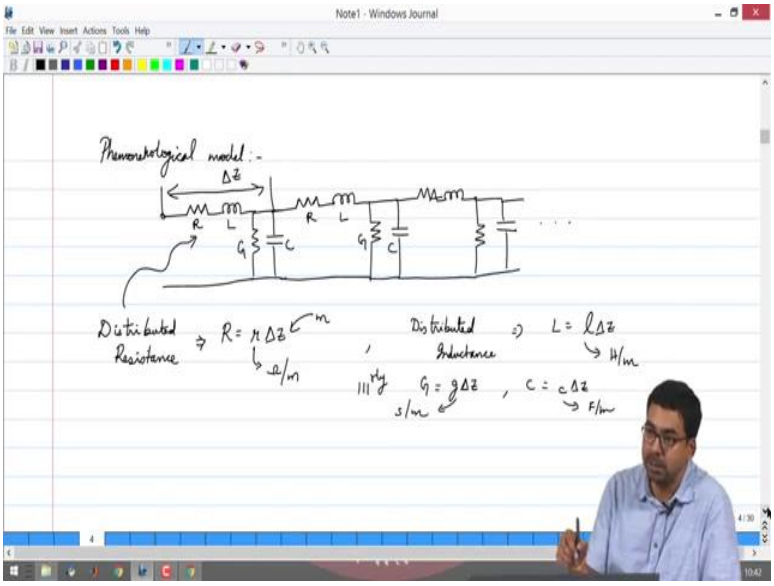

The more accurate, it becomes it will be known as a physical model all right. But it is not empirical last year because we are not basing this simply based on measurements, we are associating some science to it to build this model ok. It is based on some phenomenon here, the phenomenon that we are observing is transit time velocity and the fact that even if you break down the circuit into small chunks, you still need to have some small tiny resistances present ok.

If that is the case, what would that be all right? So, we will be having the equivalent circuit for that interconnect to be having, say , a smaller inductor, a tiny capacitance present between the top and the bottom line. So, this is the top line and this is the written part ok, you will have an inductor and a capacitor, but this means that we have drawn everything ideal and once again, the question of delay becomes a question I mean becomes unclear.

So, the way to start analyzing this is by starting with an elaborate circuit and actually crossing out quantities which will help us to arrive at a simpler solution. So, we know that there is an R_C, R_L effect because of the delay.

So, we can say that we can start with an R_L right and then, we will have a resistance between the top and the bottom lines and a capacitance between the top and the bottom lines and this unit keeps repeating again and again in each small section ok.

Forms, what is known as a ladder network ok and we can call series resistance to be R, this is L, this to be a conductance G, this is a capacitance. So, its R, L, G, C right ok. Keep in mind that we are still using bulk quantities like R L G and C. So, the unit of R is a norm. L is going to be in henrys. G is going to be in Siemens. C is going to be in farads right.

But we know that these are divided into small sections and usually if you are buying a coaxial cable or if you are designing PCBs, you are worried about the length and you are also worried about the value of these quantities per unit length because now you are dividing it in small sections right. So, we will have to come up with some way to say that this section is right.

The length is Δz, if that is the case, we will have to say that this R is going to be a distributed parameter ok and we can say that this R is some oops Δz ok. So, this represents some bulk single resistance that we have put in the circuit.

Actually, the resistance is present throughout the line. So, if this is the case, then we have to say that this is going to be in Ohms per meter and this is going to be in meters and put together for a given section of the line you will be able to calculate the resistance for that entire section.

Similarly, each of these quantities are for a specific section right. So, we will have to say that distributed inductance, it means that $L = l\Delta z$ and similarly, you will be having $G = g\Delta z$ and capacitance is the moment you start writing down quantities all right, which involve a per meter. For example, here the unit is going to be Henry per meter, here it is going to be Siemens per meter and here it is going to be Farads per meter all right.

When you start denoting all the passives like this it is a clear indication to a circuit designer that you are talking about distributed parameters, not lumped parameters ok. So, it gives them an idea clearly that you are not talking about low frequency circuit analysis, but you are actually considering the tiniest delay as possible in your circuit and account for it very very clearly ok.

Now, that we have divided this the natural question that comes through the mind is given transmission line or a given set of wires all right, which are represented by this circuit, is going to have Δz to be very small and you will have the circuit repeating again and again and it is not going to be easy to solve for the loop currents or the node voltages. Because you have an enormous number of nodes and an enormous number of loops, is it possible to do some analysis in a cleaner analytical manner? That is the question.

Since these are identical units repeating again and again, one could always say that we could evaluate the quantities I and V for a given unit and then try to see what meaning we can arrive using that unit cell to build a complete picture of this entire circuit ok. So, the analysis is usually done using a single unit cell right ok.

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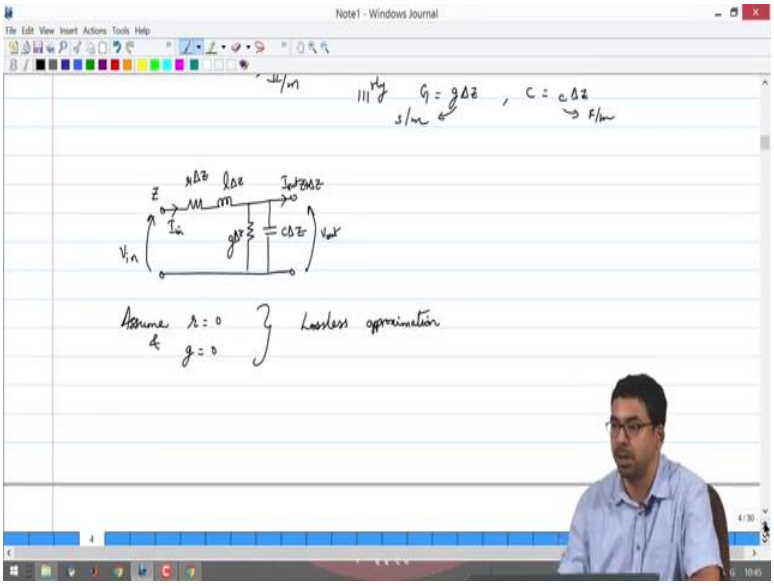

So, we can start with a single unit cell and say this is r Δz, series with l Δz, g Δz and it is a small section of your entire circuit. This is the repeating unit. We will call this portion with a space coordinate of z, this portion will be z + Δz ok.

So, we can say that the voltage here is Vin and the voltage here is Vout right. The current that is entering this particular portion of the circuit can be In, the current that is coming out here is Out ok. So, we can start to write down some equations which relate Vin to Vout In to Out extra ok. But before we start doing this, let us make our job a little bit simpler ok.

We started with the circuit that has R L G and C ok Suppose, we consider a scenario where the lines are ideal, that is they do not have any loss or resistance at all. We could go for one more level of approximation and reduce the amount of math that you need to do to arrive at an analytical expression. So, let us start with a simple case. It is the line that is ideal all right and your dielectric that is between the top and the bottom layers of the PCB is an ideal dielectric.

It does not have any trickling conductance going from the top to the bottom. If that is the case you do not have any conductance between your 2 layers of the PCB and you have infinite conductivity between the top layers of the PCB which means that r is equal to 0 and g is equal to 0, it is an approximation. This approximation is usually referred to as a lossless ok.

So, it reduces the number of components for which we need to derive an analytical expression for the voltage. So, I will do this for r equal to 0 and g equal to 0 first. Later on, in the course once we are comfortable in handling this lossless approximation, we will go for the full lossy approximation which is more indicative of what will happen in reality ok.

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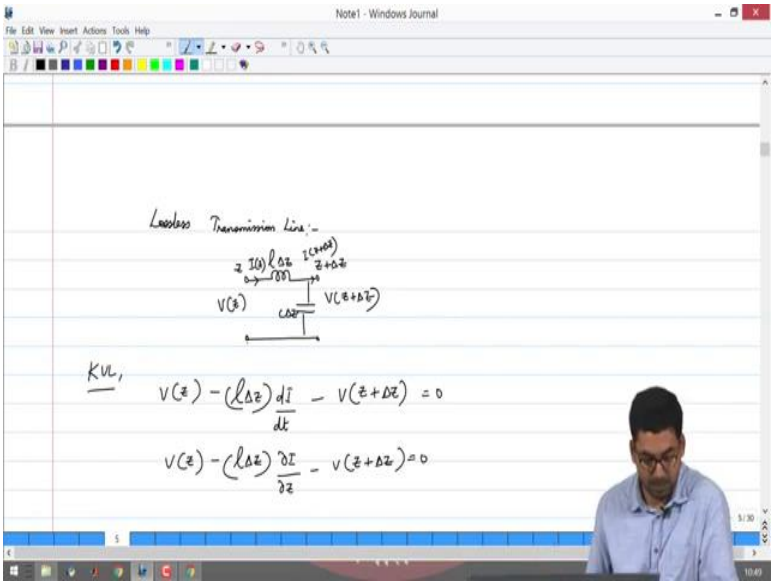

So, now your lossless case ok, you have

$V(z + \Delta z)$. I(z) coming into the circuit. $I = (z + \Delta z)$ going out and our job is to simply find out the relationship between the input and the output quantities and we are saying that this is a transmission line. Transmission line now I think we are comfortable to define. What is a transmission line? Transmission line is a branch of this electric circuit, where we are dealing with very long interconnections, where the transit times are comparable to the period all right and the frequencies are very high ok.

So, in such a case we have to divide even a short circuit into a number of smaller elements, where you can apply KCL and KVL and when you indicate such a unit cell, it is abundantly clear to the designer that you are considering time transit effects ok. So, now, we can apply KVL all right. So, we go around the loop and we apply Kirchhoff's voltage law. So, we can start with the voltage on the left side

$$V(z) - (l\Delta z)\frac{dI}{dt} - V(z + \Delta z) = 0$$

This is using Kirchhoff's voltage law. Now, though I have written

$$V(z) - (l\Delta z)\frac{\partial I}{\partial t} - V(z + \Delta z) = 0$$

which is consistent with your low frequency circuit analysis, we learned that $V = L\frac{dI}{dt}$ in low frequency circuit analysis.

We have introduced space in our circuit already alright and we also know that the space and the time are going to be dictating the velocity, that means, they are related in some way. It means that the current as we have indicated in the diagram is a function of space $I(z)$, $I(z + \Delta z)$, we have written that its function of space is all right.

So, this means that the current is going to be dependent both on space and on time all right. So, the correct way to write this equation is not using ordinary derivatives, but actually using partial derivatives ok. So, the correct way to write this now will be

$$V(z) - (l\Delta z)\frac{\partial I}{\partial t} - V(z + \Delta z) = 0$$

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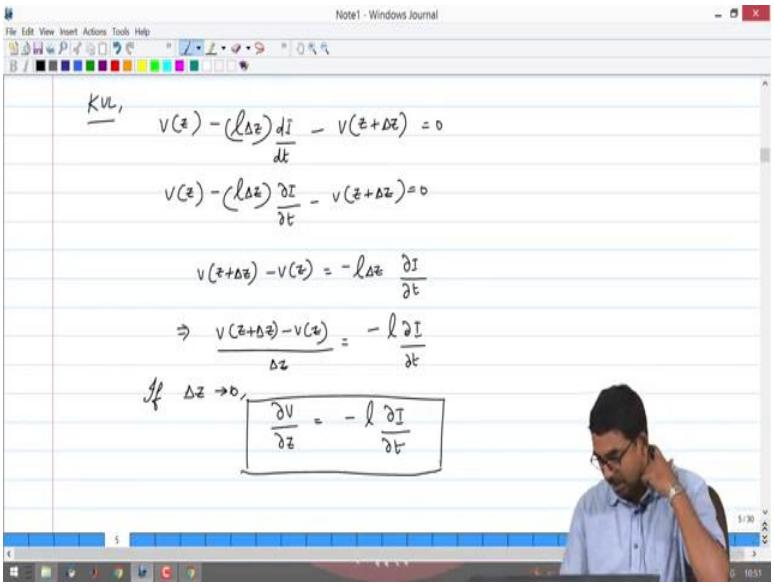

So, we can have

$$V(z + \Delta z) - V(z) = -(l\Delta z)\frac{\partial I}{\partial t}$$

$$\frac{V(z + \Delta z) - V(z)}{\Delta z} = -(l\Delta z)\frac{\partial I}{\partial t}$$

So, if Δz is really really really tiny as Δz tends to 0, the left hand side becomes simply derivative of

$$\frac{\partial V}{\partial t} = -l\frac{\partial I}{\partial t}$$

This is a very important equation and for people who have studied circuit analysis in your undergraduate, you may not have seen a derivative of voltage with respect to space in a circuit analysis.

So, for the first time we are having space being treated as an independent variable in circuit analysis. So, previously we just had $V = L\frac{dI}{dt}$, but now we are having

$$\frac{\partial V}{\partial t} = -l\frac{\partial I}{\partial t}$$

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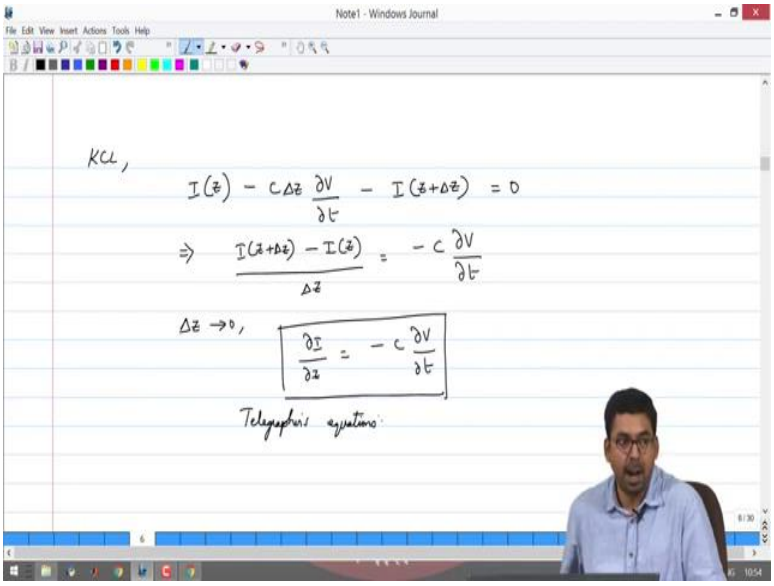

Now, similarly, if one were to use KCL or Kirchhoff's current law. So, you will have the incoming current $I(z)$ minus the current going through the capacitor branch ok. So, that can be represented as

$$I(z) - (c\Delta z)\frac{\partial I}{\partial t} - I(z + \Delta z) = 0$$

$$\frac{I(z + \Delta z) - I(z)}{\Delta z} = -(c)\frac{\partial V}{\partial t}$$

This can be rearranged as Δz tends to 0 which is a very small section, it will be having

$$\frac{\partial I}{\partial t} = -c\frac{\partial V}{\partial t}$$

So, now, we have 2 equations, one equation has been obtained by using KVL and the other equation has been obtained using KCLs and in both of these cases, we noticed something. Spatial derivative of voltage is dependent on time derivative of current and spatial derivative of current is dependent on time derivative of voltage.

I believe that for a person who has studied circuit analysis in the undergraduate, this will be the first time they are actually seeing space derivatives and time derivatives coming on each side right. So, we will stop here. The names of the equations that we have written down are a Telegrapher's equations and these are the starting point for analysis of transmission lines.

So, to summarize what we studied in this particular lecture, we saw that we could connect different ICs on a PCB using interconnects or a source and a sink that are very well separated using some ideal short circuit lines. But when your frequency is high and when the transit time between the 2 edges of your line is considerable, then you will have to think about using KCL KVL for your analysis. It is not going to be easy to apply.

So, you have to divide your transmission line into a number of small sections and to account for the delay, you have to use R L and R_C and to minimize the analysis, we have assumed that R and G are going to be 0. In this particular approximation we know we call it as a lossless transmission line approximation and once we do this approximation, we get some equations governing the current and the voltage in these circuits, which is space derivative corresponding to time derivative of the other quantity ok.

So, we will stop here and we will meet for the next lecture at the same place.