Multirate Digital Signal Processing
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Lecture – 13 (Part-1)
Noble Identities and Polyphase Decomposition – Part 1

Good morning, we begin lecture 13, we today we will do a recap of lecture 12 and also look at the very interesting and important results, which is referred to as noble identities, that is more or less the foundational building block for all of the work that we will be doing in multi-red signal processing along with polyphase decomposition.

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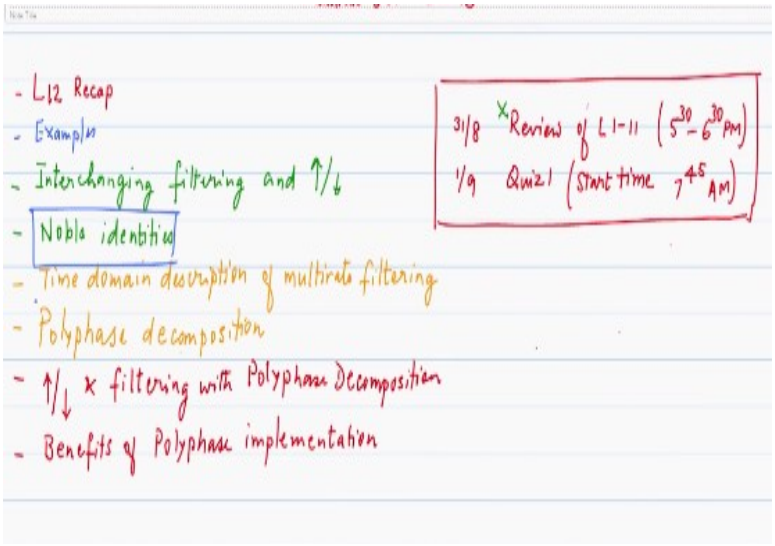

So it is a combination of the noble identities and the polyphase decomposition, both of which are going to be covered in today's lecture. Before we begin just wanted to mention that the TA's feedback was that the review may not be necessary because students have not had many doubts on either on assignment 1 or assignment 2. So, the review stands cancelled, if you do need that to be done please let the TA's know and then we will arrange for the review.

Tomorrow morning quiz 1 starts at 7:45, so again please take advantage of the additional 15 minutes, it is a 50 minute quiz with 15 additional minutes just to give you time to settle down and you know get comfortable with the paper. So let us quickly summarize the results that we have looked at in the last lecture.

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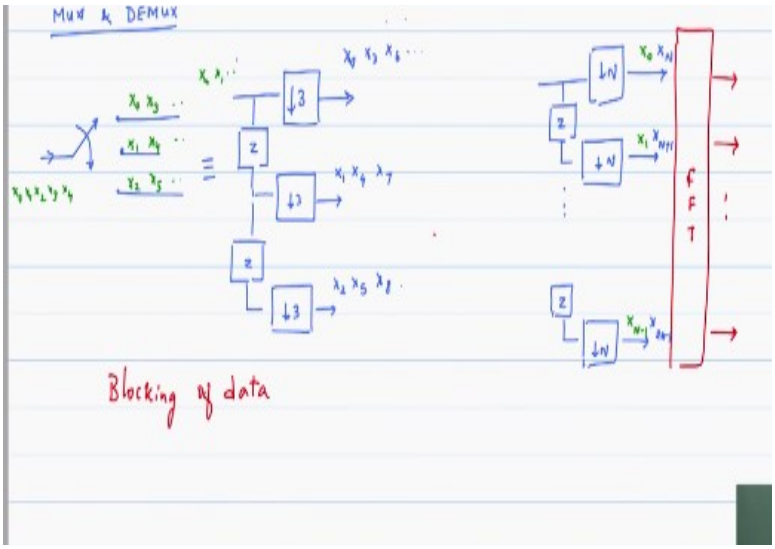

And I would say that one of the key results, if I were to summarize would be in the following manner.

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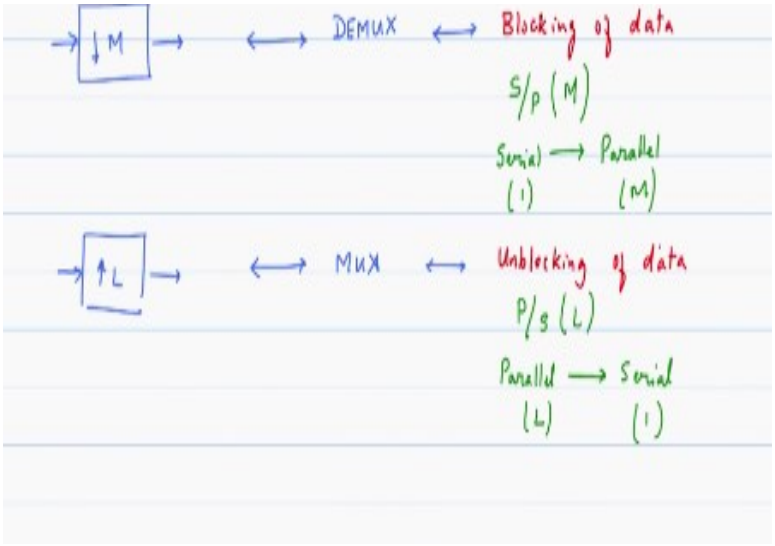

That we said that the down converter or the down sampler down sampling by a factor of M we said was related to a demultiplexer, one that split a high rate stream into multiple low rate streams out of which one of them is being kept. So it has the view of demultiplexer and we also saw that this has the same role as blocking of data, creating blocks of data, blocking of data.

So that is linkage that I would like you to keep in mind and we also have one more very important way of describing this particular operation that we have been talking about and that would be in the context of a serial to parallel converter and it is a M channel serial to parallel

converter. So basically it is a serial to parallel and number of parallel channel, serial is one channel, parallel is M channel right the high rate.

So this is the you can think of this as the serial stream and this effectively the down converter, down sampler only one stream is coming out, but effectively there are other streams that could be visualized when you look at it in the form of a structure okay. So again this representation, the down sampler has got not only the down sampling operation, it is also very closely tied to the demultiplexing operation and also the blocking of data.

So those are linked concepts and in the same manner we can also indicate the counterpart, the up sampler, by a factor of L. This would be the multiplexing operation. We showed that this was a multiplexing operation where L-1 0 valued entries are being multiplexed into the signal. This can be viewed as the unblocking of data, that is removing the blocks and making it into a serial stream, unblocking of data and this we would refer to as a parallel to serial converter of dimension L.

L basically this is the up sampling rate factor okay. So this would be a parallel, that is basically this up sampling by L in combination with some delay elements or advanced elements will give us the multiplexing, the demultiplexing and also the blocking, unblocking of data. So these 2 blocks are useful for us. So parallel to serial where I have L channels in the parallel side and serial will be 1, okay.

Now let me just reinforce this with the slide that we drew in yesterday's class. I did not want to start with that, but basically summarize it, but useful for us to review the slide that we looked at last time okay. So the downsampler, embedded with some delays, gave us a demultiplexer and we said that if these are advance elements then we have a demultiplexer that is going in the clockwise direction okay.

So very important, so this is the blocking of data and when you have the advance operations then this would correspond to a serial to parallel converter of; let me write M in the general case in this particular case it is equal to 3 okay, serial to parallel conversion with clockwise commutative okay that is also important because if you changed it to delay elements then we saw that it went in the counterclockwise.

So clockwise direction okay, so there is a shorthand notation that we use, and maybe it is good for you to sort of keep in mind, that if I write down SPM then basically it refers to this structure with M channels okay. So serial to parallel converter in the conventional way of blocking of data that is X0, X1, X2, X3, X4 and then so on.

This would be the structure that would be using, and of course this is directly linked to the application that we discussed yesterday, where if I was taking data, blocking it into non-overlapping segments and doing in FFT operation. For example if I wanted to do spectral analysis, then this would fit perfectly. So basically what I would ask you for, to do is implement a serial to parallel converter with M channels.

So you would do a multirate structure which is indicated in this manner, which would be exactly what we are trying to implement in this case, so that you can get the data samples being fed in appropriately in the form of blocks.

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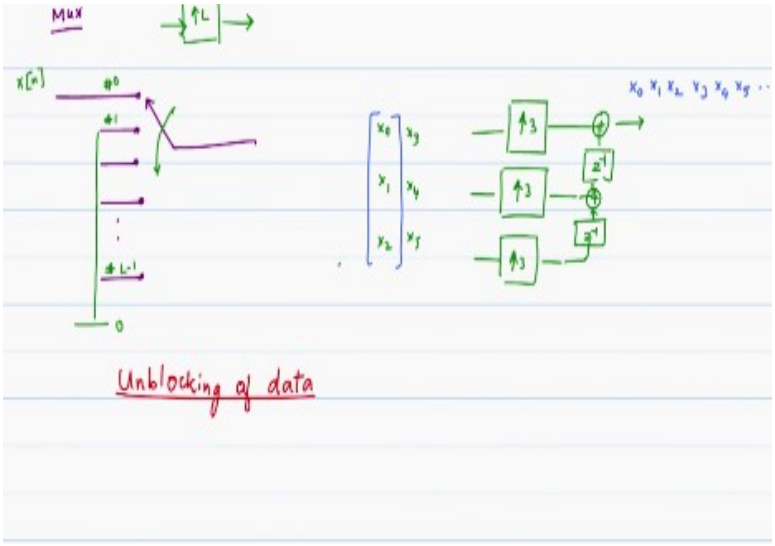

Now the counterpart the up sampler we said that can be viewed as a multiplexing operation where L-1 0 valued samples are being fed in which is indicated in this one and of course if you combine the up sampler with the delay elements this would give us the parallel to serial conversion, this would be the parallel to serial conversion in this case with L = 3 channels with the anti-clockwise commutator okay.

So with anti-clockwise commutator now the reason we choose clockwise in one direction and anti-clockwise in the other direction is so that the data will come out in the correct sequence.

So if you chose the anti-clockwise in the where you did the serial to parallel conversion you would have to do the other one to get the corresponding sequencing correctly here.

So this would be anti-clockwise commutator and like last time there is a short form notation, which we will just say parallel to serial with L, which means basically this structure with the anti-clockwise commutator being implemented which means that you would have to combine up samplers with delays and then appropriately combine them and take them out. So again simple concepts but once you start putting it together you will see that there are some very interesting results that we can obtain. So let me reinforce this with an example.

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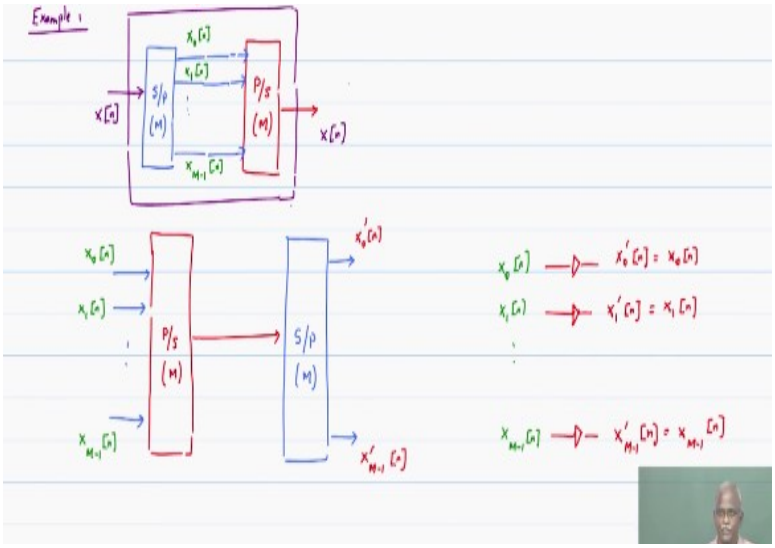

So example of what we have just looked at currently. So example 1 applying the concepts of multiplexer and demultiplexer. I have X of N. I am going to introduce a serial to parallel conversion of order M okay, which means that I will have M streams coming out, I would just like, for convenience I would represent them as X0 of N, these are the subsequences X1 of N and the last one as XM - 1 of N, M parallel sub sequences okay.

Now I am going to ask you to apply a parallel to serial converter okay, of the same dimensions M and then take the output okay. It is sort of a trivial example and this output is X of N okay. So no issues, very straightforward okay. Now that was not the main question okay. Now here comes the actually the interesting question. So I have M signals coming in, I label them as X0 of N, X1 of N, XM - 1 of N.

So just before I do that, so that means this whole block effectively was equivalent to a gain of 1, right, basically you got input and output X of N which means the that whatever was inside if you treated as a black box it actually was giving you unit a gain okay. So now I have M inputs streams. I ask you to apply a parallel to serial converter, a parallel to serial converter of dimension M, which means that I will produce a single stream coming out, am I right?

Then at the other end I ask you to do a serial to parallel conversion, serial to parallel conversion okay. So this would be a serial to parallel conversion of order M, of order M, which means that I would once again get M channels coming out, am I right. Now keep in mind this means that parallel to serial converter with a counter clockwise commutator. This is a serial to parallel converter with a counterclockwise commutator okay.

The basic definitions as I told you were all defined in the previous slides. So if I now were to label these output signals as X0 prime of n all the way to XM - 1 prime of n, is there a relationship between the primed signals, output signals and the input signals obviously there should be which one is getting mapped into which one,? Are they going directly or are they getting swapped around, is there any delay coming into the picture or they are coming in exactly as before?

What is the link between the input signals and the output signals okay? Interesting task you can verify that it is X0 of n, X1 of n... XM - 1 of n, all of them have got unity gain and show up as X0 prime of n which basically means that this is equal to X0 of n, this is X1 prime of n which is equal to X1 of n and XM -1 prime of n, is = XM - 1 of M okay.

Now though it does require a little bit of looking at the structure, looking how the signal is flowing, which branch is connected to which branch and then basically convincing yourself that yes this is the case. In other words, interchanging the parallel to serial and serial to parallel should not change things you should basically get back to original sequences; however, now see we have a very rich multirate structure.

We deliberately chose to have delay advanced operators on the input side when you did the serial to parallel conversion. Now you could have done it with the advanced operators, you could have done it to delay elements and so basically when you have combinations of these, that is in other words we have the delay elements, advanced elements and the ability to split.

You start getting some interesting combinations and interesting structures and again you may think, you know why would you waste time trying to create different ways of interleaving and deinterleaving. Actually that is not the intent at all, it is actually when you take communications problems and you analyze them sometimes they map into this form of, different forms of parallel to serial conversion and serial to parallel conversion.

And again we will be looking at those examples and hopefully when we come to those concepts then you say oh yeah okay, now this makes sense. This is why we are doing a counterclockwise commutator on the serial to parallel side and then on this side. So keep this structure in mind this actually leads to several interesting foundational results which we will build on in the lectures to come.