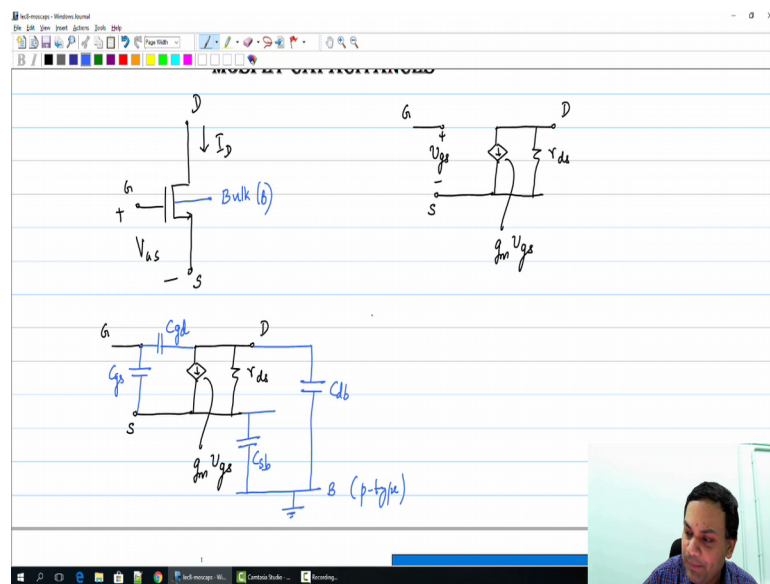


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Lecture - 08
MOSFET Capacitances

In this lecture we will briefly look at the different types of capacitance is associated with a MOSFET.

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So, far we have been assuming that the MOSFET is an infinitely fast device and therefore, the output drain current will respond almost instantaneously to the applied gate source voltage. But in reality this is not true and therefore, the MOSFET will have a certain delay associated with it which we will model as capacitances.

And if you look at the three terminal model of the MOSFET that we have built so far the MOSFET presents an open circuit between the gate and source terminals and between the drain and source terminals it presents 2 components one of them is the voltage controlled current source corresponding to the transconductance of the device which is g_m times small v_{gs} which is the small signal gate source voltage. And it also presents resistance which we will represent as R_{ds} which is due to channel length modulation.

Now, to understand the capacitances of the device we have to realize that the MOSFET also has a fourth terminal which is the bulk terminal or B and there are various capacitances associated with the between the different terminals of the MOSFET. Now, I will show the capacitances in blue on the same figure. So, it turns out that the MOSFET has 4 capacitances associated with the device itself. So, the first capacitance is the gate source capacitance which we will represent as C_{gs} , it also has a capacitance between the gate and drain terminals which we will call C_{gd} , it has 2 more capacitances associated with the bulk terminal. So, there is a source bulk capacitance C_{sb} and there is a drain bulk capacitance C_{db} .

As you can see now due to this capacitances the MOSFET will not respond instantaneously to any applied gate source voltage there will be certain delays associated with the device. Now just wanted to point out that in this course we will not be studying each of this capacitances in too much detail the things we need to remember that the largest capacitance associated with the MOSFET is C_{gs} and in saturation the C_{gs} is approximately equal to two-thirds W times L times C_{ox} where W is the width of the gate of the MOSFET, L is the length of the gate of the MOSFET and C_{ox} is of course, the oxide capacitance per unit area. This is normally the largest capacitance associated with the MOSFET.

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largest capacitance : C_{gs}

In sat. region: $C_{gs} \approx \frac{2}{3} W L C_{ox}$ — oxide cap per unit area

Width Length

Assume: Every node of circuit has capacitance to ground) Circuit & System analysis

Now obviously, each capacitance has a certain dependence on dimensions has a certain dependence on also on doping concentrations etcetera so, but we will not worry about those things here in this course, we will assume that every node has some capacitance to ground, we will assume that every node of the circuit has some capacitance to ground.

This will, you will find that this will make a job much easier we will assume this only for circuit analysis, circuit and system analysis. And I also wanted to point out that normally since we have not seen this bulk terminal 2 often before normally this bulk terminal is connected to the lowest a potential in the circuit if it is a p type substrate and therefore, the drain bulk and source bulk capacitances have one node grounded.

Now, I also should tell you that C_{gd} is normally a small capacitance, normally a small capacitance, but it can become significant as the device get smaller and smaller. Let us take a quick example to understand the effects of this of this capacitance. So, we will take the simplest amplifier that we have always seen which is a common source amplifier. So, let us assume that we have a common source amplifier with a resistive load.

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$$\frac{v_o}{v_s} = -g_m R \quad (\text{neglecting } r_{ds})$$

$$r_{ds} \gg R$$

$$v_o = -g_m v_{gs} \left(R \parallel \frac{1}{sC_2} \right) = -g_m v_s \left(R \parallel \frac{1}{sC_2} \right)$$

$$\frac{v_o}{v_s} = -g_m \cdot \frac{R \cdot \frac{1}{sC_2}}{R + \frac{1}{sC_2}}$$

$$= \left(-g_m R \right) \cdot \left(\frac{1}{1 + sC_2 R} \right)$$

low-frequency or DC gain

So, at the gate I apply the combination of a V bias I will call that V B plus some small signal voltage v s. Let us assume that this resistance is R now I need to assume the capacitances in the circuit I am going to make my job simpler by ignoring C gd for now.

So, I know that the significant capacitances in the circuit are going to be these two capacitors.

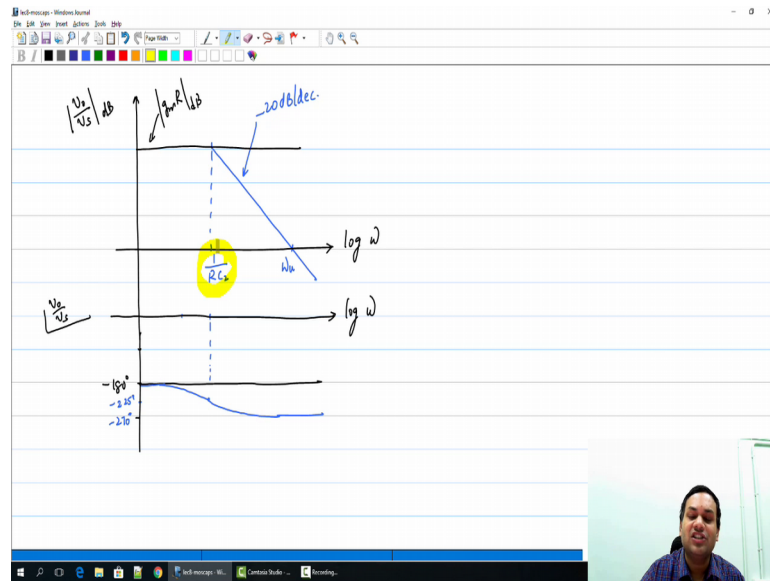
Now, I also know that those capacitances will come typically from devices connected to the terminal, but I will just call them C_1 and C_2 for now because I just want to find out what happens to the circuit when I actually have capacitances from every node to ground. Because normally I given the size of the device and given the device properties I can calculate what C_1 and C_2 are so for now at the system level I am just going to assume that there are capacitances C_1 and C_2 . At low frequencies we know that the gain of the amplifier which is the v_o by v_s is minus g_m times R this is of course, true only at low frequencies and I am also neglecting r_{ds} in this particular expression and normally normally r_{ds} , r_{ds} would be much much larger than R .

Now, suppose you have capacitances C_1 and C_2 I now have to draw the new equivalent circuit and I will do that here the small signal equivalent circuit will look as follows. So, v_s is directly applied across C_1 which generates the gate source voltage and again for the purposes of this discussion I am going to assume that r_{ds} is much larger than R . In such a case the output voltage is nothing, but minus $g_m v_{gs}$ into R parallel $1/sC_2$, as you can see there is since v_s is assumed to be an ideal voltage source in this case the voltage appears directly across C_1 and you can write v_o in terms of v_s in this manner.

Now, what is the expression for v_o by v_s ? V_o by v_s is nothing, but minus g_m into this expression and this can be further simplified in the following fashion, I am going to write it in two steps. The first portion is the small signal gain of the circuit in the absence of capacitances in other words it is the low frequency or DC gain of the circuit. So, it is often called DC gain even though it is not at DC, it is the low frequency gain of the amplifier and that is of course, multiplied by 1 plus sC_2R . This gives you the frequency response of the circuit which happens to go to 1 when the when you operate at very low frequencies.

Now, as you can see in this particular case the transfer function which is the gain of the device has a single pole response. So, now, let us quickly draw the bode plot for this particular circuit.

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So, if I were to draw the magnitude and phase response of the circuit. So, I am going to plot v_o by v_s magnitude and the angle of v_o by v_s . At very low frequencies which I am going to draw in black or rather without the capacitances the circuit looks ideal it has a constant gain irrespective of frequency whose magnitude is g_m times R .

The phase of the circuit is now at constant is now a constant value of minus 180 degrees. Now, with the capacitances C_1 and C_2 it turns out that this behavior is valid only at low frequencies and at higher frequencies the circuit goes the magnitude of the gain goes down at minus 20 dB per decade in this particular plot. Now I will just point out that this is now in dB and not just the magnitude and you are plotting it as a function of log of omega.

And the pole frequency in this case is at 1 over $R C_2$ and also this frequency at which the gain goes to 1 is often called the unity gain frequency and that can easily be calculated from the previous expression here. What about the phase response? Now, it turns out that in this particular circuit at low frequencies the phase still minus 180 degrees, so the circuit starts off at minus 180 degrees. But as we know after it hits actually a little bit before it hits the pole at 1 over $R C_2$ the phase starts to degrade starts to reduce further and that starts happening at approximately one-tenth of this frequency.

And at the pole frequency the phase should the pole should give a phase of exactly minus 45 degrees and that will happen here it will be at minus 225 degrees at the pole

frequency and at very large frequencies the pole should contribute 90 degrees and therefore, it should asymptotically go to minus 270 degrees. So, the phase response will look something like this. Now, as you can see the circuit looks the or rather the circuit or the phase response or the magnitude response looks nothing like the low frequency equivalent when you start increasing the frequency to really large values that are comparable or larger than $1/RC$ which is the pole frequency of the system.