Analog Integrated Circuit Design
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Lecture – 43
Fully differential two stage Op-Amp

Hello and welcome to lecture 43 of analog integrated circuit design. We were looking at fully differential Two stage Op-Amp now the differential half circuit of that consists of two common sources amplifiers in cascade.

So, it gives you the gain of two stages and the frequency response and other things are quite similar to like slew rate and noise and so, on or the same as what we would find in a two stage single ended Op-Amp. The only difference is that the mirror pole and 0 that appear in the single ended Op-Amp, do not appear in the two stage Op-Amp.

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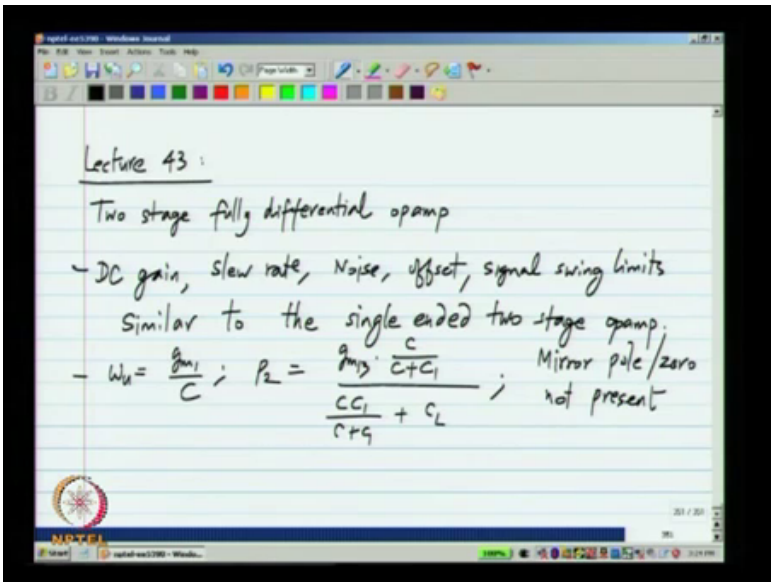

So, the differential operation is by enlarge the same; these all can be calculated for the fully differential case, but these will be similar to single ended two stage Op-Amp. Now the parasitic poles are also similar in that the unity gain frequency is g m 1 by C and the second pole is related to that except that there will not be the mirror pole zero that is the pole zero due to the current mirror is not present.

Now, because of these reasons we will not discuss this further in perhaps a later summary lecture, I will quickly summarize all of these quantities. We will concentrate on the common mode feedback circuit for the fully differential two stage Op-Amp.

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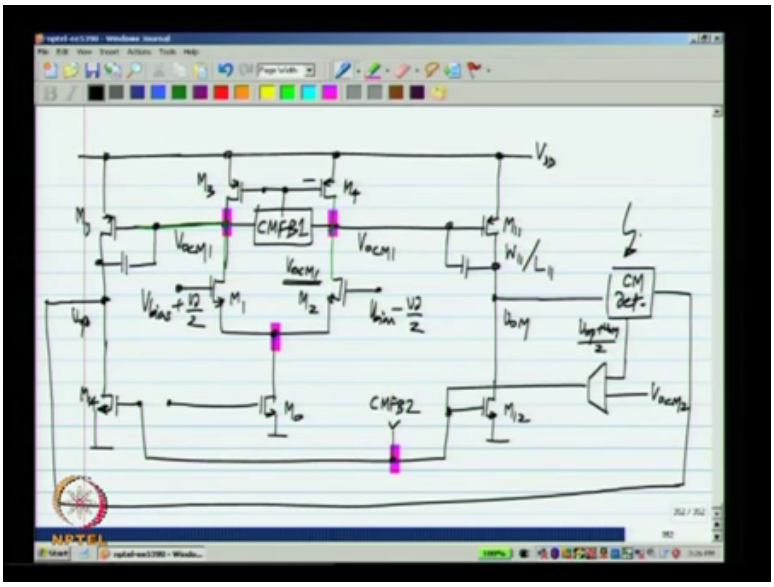

For now I will assume that the first stages is independently stabilized using some circuit which can be any one of the several circuits that we discussed while discussing the fully differential single stage Op-Amp.

Now, because the first stage is required to provide gain and if you have any resistive load here ah; it will compromise the gain of the Op-Amp severely. We will assume that the common mode feedback used for the first stage is one of those which does not have a resistive input? We will not use a resistive common mode detector, but we will use one of the other things either a buffered circuit or the circuit where we compare V o p and V o M separately with VOCM and so on.

Now, the active common mode detectors are usually non-linear, but if you consider a two stage Op-Amp; the output stage will have a large swing and the first stage output will have a relatively small swing. So, the non-linearity will not affect much and it is quite all right to use one of the active common mode detectors at the output of the first stage. For the second stage, basically we have to go on adjusting we gates of M 12 and M 14 until V o p and V o M the common mode of that reaches the desired value.

So, what do we do? What we need to do is to detect the common mode of the second stage that will give us V o p plus V o M by 2 and compare that with the desired common mode voltage VOCM 2 and apply it to CMFB 2. In this case what can be use for the common mode detector? And if you observe while discussing the two stage Op-Amp; I had said that the output can support a large swing. You have just one transistor at the top to the upper rail and one transistor at the bottom to the lower rail. Now with these you get the maximum swing that is possible in a CMOS circuit that is 1 VDSAT away from either of the rails.

So, in this case we have to use a common mode detector that works with large signal swings and really the only choice is the resistive common mode detector. Now this will add resistive load to the output of the two stage Op-Amp, but a two stage Op-Amp can handle resistive loads; even if the gain of the second stage is compromise the little the first stage provides the bulk of the gain. So, it is to use a resistive common mode detector with the two stage Op-Amp ah. In fact, it is necessary to be able to support a high swing output.

The trans conductor that we use here is basically the single stage a single ended Op-Amp; what I will do now is to draw only the common mode equivalent circuit.

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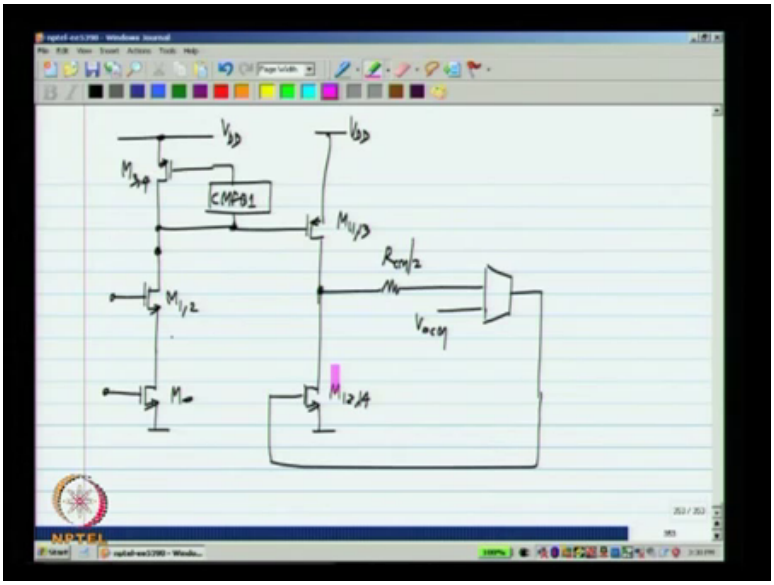

This is the first stage M 1, 2 in parallel we have M 0 and we have M 3 and 4 in parallel. And we have this the first stage common mode feedback 1; here what I mean is the

common mode half circuit corresponding to that one; feeding it to M 3 and M 4. And the output of M 3 and M 4 is also connected to M 11 and M 13 and we have the loads M 12 and 14

So, we have the common mode detection and like I said we will use a resistive common mode detector. So, we have R by 2 here I will call it RCM by 2 and that has to be compared with VOCM and fed back to the gates of M 12 and M 14.

Now, because we are feeding back to the gate of the NMOS; the output of the single ended single stage Op-Amp that is used for common mode feedback has to be able to support voltages closer to the lower rail. So, we cannot use an NMOS input here it is not suitable we will use a PMOS input stage with NMOS current mirror load.

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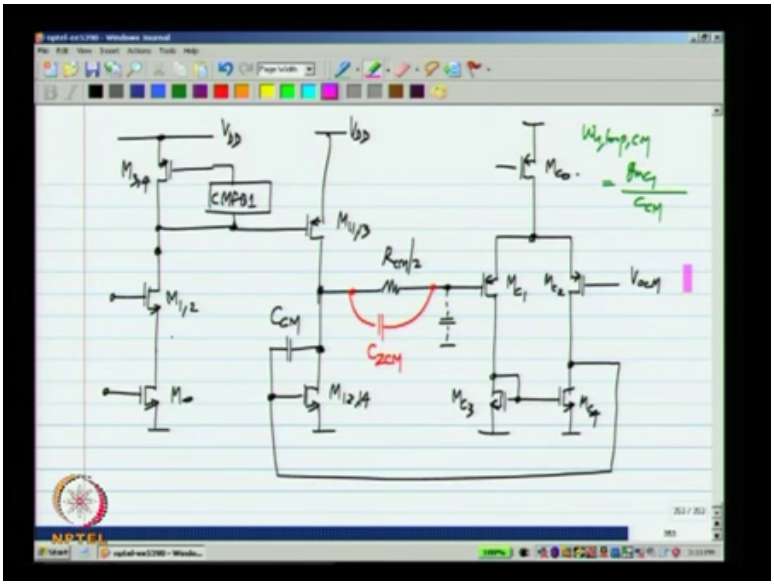

And we have to complete the loop this way. So, this forms the common mode feedback loop and for this for the loop gain to have an integrator like behavior; the easiest thing to do is to have an integrating capacitor over there. So, the equivalent picture looks exactly like that of a two stage Op-Amp except that we have a resistor in the middle.

Now, because of parasitic capacitance is here there can be a pole due to this resistor and that capacitor which adds a lot of delay into the feedback loop. As usual we counter that by connecting a capacitor over there. So, as before the common mode feedback loop; I mean this way I have seen in case of the fully differential single stage Op-Amp.

The common mode feedback loop itself looks like a two stage single ended Op-Amp in unity gain feedback. The first stage consists of the g m consisting of a form by M C 1 and M C 2 and the second stage consists of M 13 and M 14 which are basically the loads to the second stage in the differential picture.

Now, again we know how to make this feedback loop nice and stable we know what its unity loop gain frequencies. So, I will not analyze that further the unity loop gain frequency of the common mode feedback circuit will be gmc 1 which essentially if you consider only this loop; this is the first stage and that is the second stage divided by C; I mean to prevent confusion with the integrating capacitor and the differential picture let me call that C C M and I will rename these capacitors C Z C M just to imply that they introduce a 0 into the loop gain. And the DC loop gain of such a loop is quite high; so, we can expect that the common mode here will settle to something that is equal to VOCM.

Now, there is one other issue here that we discussed while discussing the single stage Op-Amp. If the output of this when the loop is broken let us say all the devices are identical; if the output of this single stage Op-Amp.

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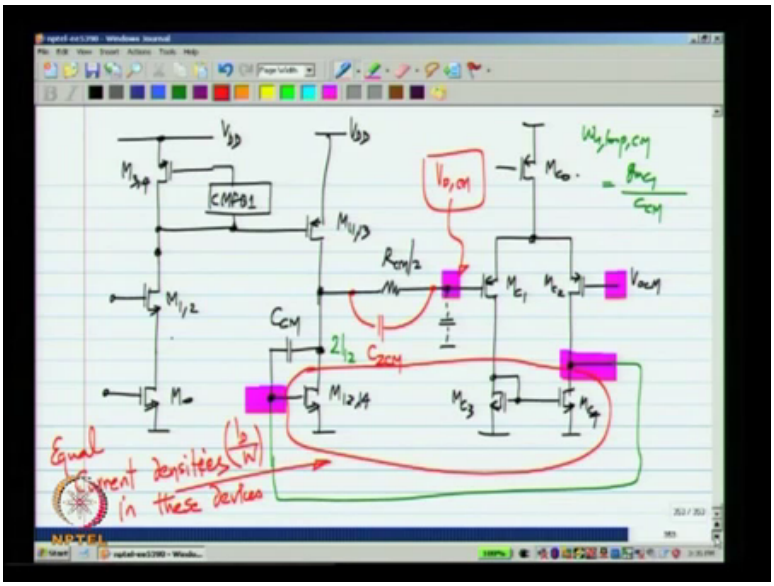

Here is different from the voltage that is required at the gates of M 12 and M 14 to supply the desired current ok; remember the current two times M 12 has to flow here in the common mode picture and that needs a certain voltage here.

Now, if the voltage that comes out of this again we are assuming a fully symmetric here. So, the voltage will be same as VGS of M C 3 that is different from the VGS required here when you connect it up; this voltage has to shift and there will be a systematic offset between that node and that node. So, to avoid systematic offset what we need to do is to have same current densities; equal current densities in these devices, when I say current density what I mean is the drain current divided by the width of the MOSFET.

So, if that is the case then the voltage that we get out of this in the ideal condition equals the voltage that we need here. So, when we connect it up the loop will stabilize with this voltage being exactly equal to that voltage we extensively discuss the issue of systematic offset in the two stage single ended Op-Amp and it is the same thing here. Now did not mention this while discussing the fully differential single stage Op-Amp, but even in that case you have to equalize the current densities in the trans conductor used for common mode feedback and the load transistors used in the Op-Amp.

So, this will stabilize to VOCM. So, as before ah for checking that the loop works properly you have to resort the simulation you can simulate the loop gain, you can also apply a common mode step and look at the step response. So, this is this is the way to stabilize a two stage fully differential Op-Amp.

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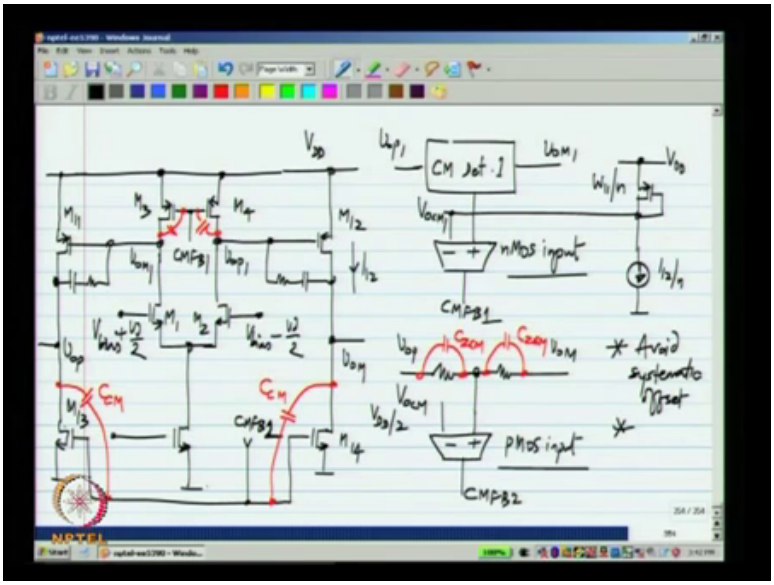

Let me try to draw the complete circuit here it is going to be very difficult but just to show you the seeming complexity. The concepts are very simple it is the same thing over

and over we have negative feedbacks everywhere the Op-Amp itself is made so, that it can be used in some negative feedback.

But to make the Op-Amp work properly, you need two more negative feedbacks inside to stabilize the common mode voltages. This is the fully differential two stage Op-Amp showing only the differential picture. And these are the integrating capacitors and these are the outputs V o p and V o M. And I will call the outputs of the first stage V o p 1 and V o M 1. So, we have to pass V o p 1 and V o M 1 to the some common mode detector and compare its output to VOCM 1 and feed it back to CMFB 1.

Now, as discussed earlier VOCM 1 must be derived from some replica bias that will establish the correct quiescent voltage at the output of the first stage. And what is the meaning of the correct quiescent voltage? Is the quiescent voltage that establishes the desired current in the second stage. We need a certain quiescent current I 12 in the second stage; so, that can be done by having a scale replica of the output stage in the biasing branch this replica biasing is a very common thing that is used in analog circuits.

For the second stage we will invariably use the resistive divider although in some cases you could probably use something else if you are not concerned about swings. And again you compared it with VOCM that is the common mode reference for the final output. And because the final output goes very close to VDD and also comes fairly close to ground that is within 1 VDSAT of VDD in ground.

The output common mode voltage is frequently selected to be the half the supply voltage. Although this is not a sacred number and you could choose something else if that is required. For now I will say this is VDD by 2 and again this is also supplied to the second common mode feedback circuit and the way we have the structure M 3 and M 4 are PMOS devices.

So, the trans conductor that generates the first common mode feedback voltage must have an NMOS input that is when the levels will be compatible. And similarly in the second stage we need to provide the feedback to the gates of NMOS devices. So, this should have a PMOS input and you need to mind the current density.

So, that you avoid the systematic offset in both cases and also you may have to use capacitors across the resistor to reduce delays in the common mode feedback loop. And

finally, you may have to use integrating capacitors for making the common mode feedback loop gain look like an integrator. And this may be needed in both stages whether you need an explicit capacitor here or a capacitor elsewhere it entirely depends on the bandwidth requirements and s o, on of the common mode feedback circuit.

If you do add capacitors here they will load the differential picture, but you just have to live with it maybe you find some way of minimizing the value of these capacitors and live with that. Now, in this case each of the common mode feedback circuits for the first stage and the second stage will equivalently look like the feedback loop around a single ended two stage Op-Amp. So, all the things that you can do with a single ended two stage Op-Amp, you can do here for instance you can add resistors in series with capacitors to cancel the right half plane 0 in that feedback loop. In addition you can also have resistors in series with integrating capacitors of the main Op-Amp.

Now, that is the just of the fully differential two stage Op-Amp; we need to have a common mode feedbacks for both stages or find some way of stabilizing the common mode voltages of two stages. Now one thing I want to point out here is that you see that the circuit already has become so, complicated that I cannot put all the transistors on this area that is available to me.

So, what does it mean? It does not pay to memorize circuits or a think of different circuits in an isolated fashion, here we have the main Op-Amp which will be used in some feedback circuit, but to make the Op-Amp work we have two more feedback circuits. Only way that you will clearly understand all of these things is if your first principles are solid. So, please pay attention to all of the loop gain and the basic feedbacks of with the single ended circuits and then you will be able to analyze something like this and also more importantly design something like this.

Now, this is very important because in a given circuit you could have ten of these things. So, you just imagine the complexity we will never be able to put down the entire circuit on paper and the only way to even begin to make sense of it is by having a systematic approach. Now like before like with the single ended fully differential Op-Amp; we have a choice of common mode feedback circuits available.

Now, as I mentioned there is just too much variety and I will not be able to go through all of them, but I will discuss one more interesting common mode feedback circuit that can be used for the first stage in this case.

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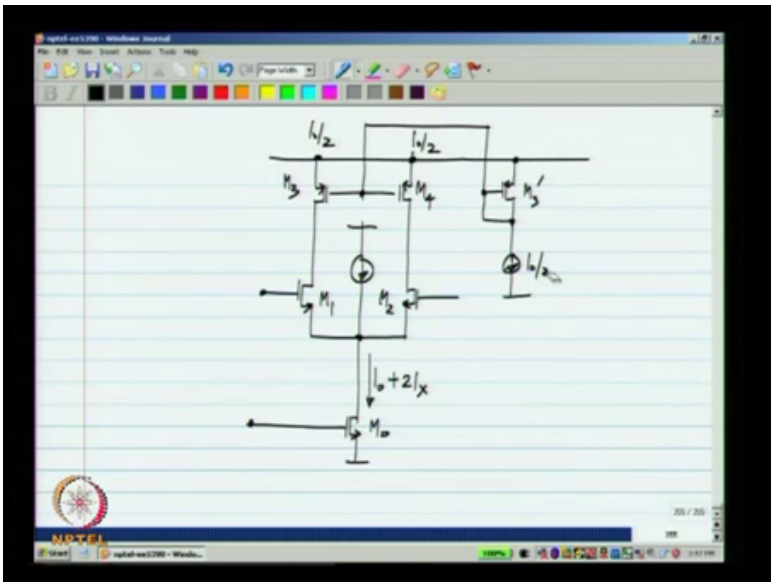

Ah It will become clear why it is suitable for the first stage; for the second stage we will use the conventional one with a resistive common mode detector and feedback using another trans conductor.

Let me draw only the first stage here; now so, far whenever we stabilize the common mode of stage like this the tail current was fixed and the currents on top were varying and it was varied by means of a feedback loop. So, that their sum exactly equals the current from the tail source. So, here we will do something different; we will bias these with the fixed voltage V g 3; what I mean here is that it will be from some current mirror.

That is the current in this is not variable it will always come from some circuit of this sort; some replica. And we will say that we have currents I naught by 2 in each of these branches where I naught is the total tail current. Now, what I can do is instead of the current from the top are fixed. So, I can vary the current at the bottom until the total current going into M 1 and M 2 equals the currents delivered from M 3 and M 4.

Now also the way I will choose to change the tail current is not by changing the gate voltage of M 0 that is possible, but in this case I will not do that what I will do is I will

just make sure that the current in M 0 is more than I naught. So, let me call it I naught plus 2 times sum I X I will choose the transistor M 0 and the current in M 0 that way. So, that it is more than the desired current.

Then what I will do is I will take a portion of it and bleed of the tail that is I remove 2 I X from this current I will get exactly I naught. So, you can imagine that I can have a current source here which is variable. Now I can go on varying this until the current that is flowing into M 1 and M 2 becomes equal to I naught. So, for that this current has to be equal to 2 I X; now as before I do not know what the value of 2 I X is; the only way I said this is by using negative feedback.

Now how can I make a current source that is that provides current that pumps out current. The easiest way to do that is by using a PMOS transistor let me remove all of this I will level this V G 3.

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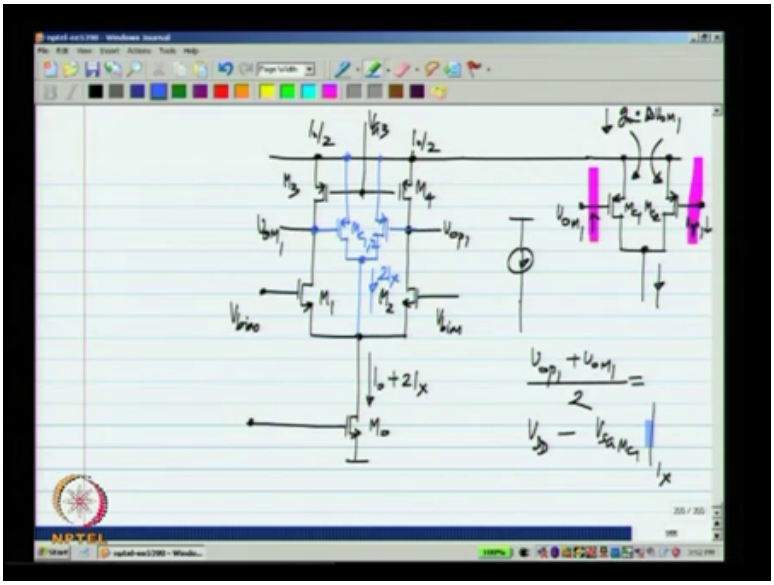

Now, a current source like this which can source current can be implemented using a PMOS transistor with that gate bias to some voltage. Also when I have a current like this and I want to make it variable what is the quantity to which it should respond? It is the common mode output of the first stage. So, always we look at the common mode output of a particular stage and based on that we vary the current until the current satisfies some particular condition. In this case it has to be equal to I 2 I X more importantly the currents in M 1 and M 2 it should be exactly equal to I naught.

Now, that is the total current should respond to V o p 1 plus V o M 1 by 2 ok; in other words V o p 1 plus V o M 1 let me assume that this is V bias plus V d by 2 and that is V bias minus V d by 2. Now we also know that the transistor here which I wanted to behave like a current source in the small signal sense; it is a voltage control current source from the gate to drain and it has a linear relationship.

Now, I will combine this with the fact that I want the current source which should respond to V o p plus V o M by 2. So, what should I do then? Remember the case where to detect the common mode we made some circuit for V o p and V o M separately and added up the currents I can do exactly the same here. So, let me call this V o M 1 and V o p 1 and I will add up the two currents.

Now, what happens here is that let us say V o M 1 increases by a small amount and V o p 1 decreases by an equal amount; the current in this transistor will fall down by g m of this transistor times delta V o M 1. And the current in this will increase by exactly the same number I am assuming these two transistors M C 1 and M C 2 are identical to each other and they have the same quiescent current.

So, what happens is this current does not change at all if they vary in equal and opposite directions. So; that means, that it does not respond to the differential of V o p and V o M, but it will respond to the common mode let us say both of them increase this current will reduce and if both of them reduce this current will increase.

Now, what is it that we want here if V o p 1 and V o M 1 are too high; that means, that the currents from M 3 and M 4 are too much that is why their being pulled up. What can we do from here? The total current in M 1 and M 2 has to increase and for that this current source has to decrease.

Now, if you look at what I described earlier; if you increase both of these voltages the total current here will decrease. So, this just this structure is suitable for being used in this place. So, I will sum the two currents and connect it up there; now what happens is that let us again imagine that there is no differential input by symmetry these two voltages will be equal. Now what will be the stabilized value of these two voltages? The current in this has to be exactly equal to 2 I X.

So, the voltages here and there essentially the output common mode of the first stage VOCM 1 V o p 1 plus V o M 1 by 2 will be equal to VDD which is the upper rail voltage minus the gate source voltages of these two transistors. Let me call these M C 1 and 2; this is VDD minus V S G of M C 1 at a current of I X ok; these two currents are same and equal to I X. So, the total current is 2 I X.

So, the output will get stabilized to VDD minus V S G of something. So, that is that is how the common mode stabilization can be done for a single stage Op-Amp. By the way this can be used for the single stage Op-Amp, but it is also very interesting for use in a two stage Op-Amp.

Now, we do not need to do anything more than this. So, that is why this circuit is very simple and quite attractive.

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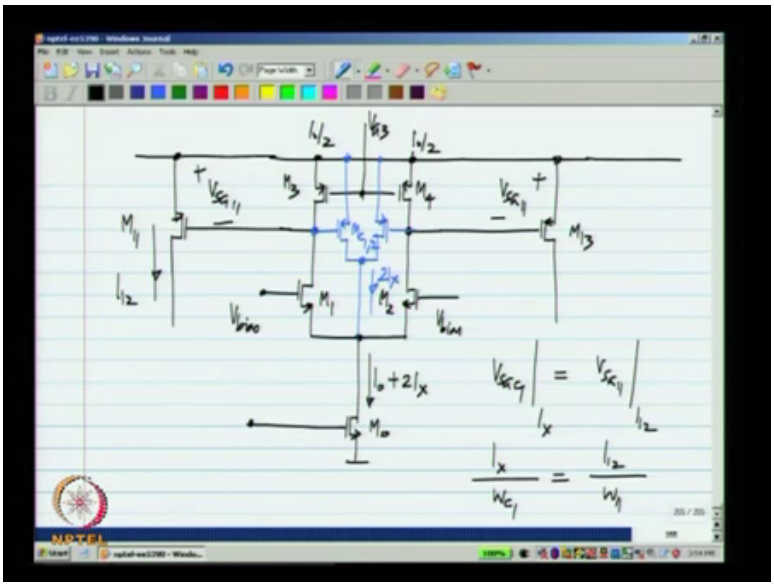

Now also in a two stage Op-Amp what happens is the outputs of the first stage go to the second stage amplifier transistors M 11 and M 13. And the output common mode voltage should be such that M 11 and M 13 carry a certain current. Because M 11 and M 13 are biased by the common mode output voltage of the first stage.

So; that means, that this has to carry some V S G I will call it V S G 11 V S G 11. Now if you remember what I just said the output common mode voltage of a first stage will be VDD minus V S G of M C 1 and M C 2. So, the voltage between VDD and this point is

V S G C 1 at a current of I X. We want this to be equal to V S G 11 at a current of whatever is required that is I will call this I 12.

Now, this is an extremely easy thing to do. So, for this to happen all we have to do is to make sure that M 11, M C 1 and 2 and M 13 have the same current densities that is in other words M C 1 and 2 are replicas of M 11 and M 13. So, what we need to do is I X divided by W C 1 should be the same as I 12 divided by W 11 and the same thing for of course, M C 2 and M 13.

So, by using replica transistors of the transistors in the output stage we can make a very simple common mode feedback circuit for the first stage. And the output common mode voltage of the first stage will get set to the right value required to bias the second stage. So, the main advantage of this kind of a biasing circuit is that we do not need any other circuit to generate a reference; simply by making these blue transistors replica of M 11 and M 13, we get the correct values of current in M 11 and M 13 now our job is not finished.

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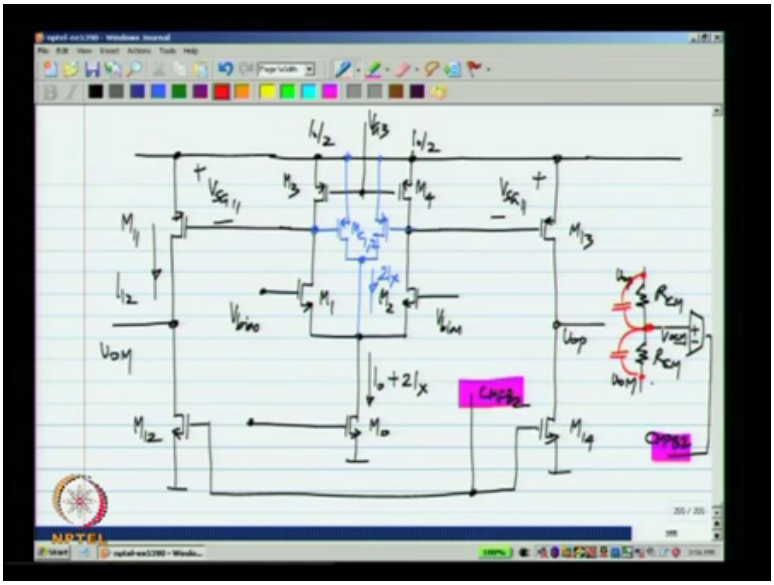

We need to provide the common mode feedback to the second stage that is M 12 and M 14. So, that the output common mode voltage reaches the desired value and that we do in the usual way by using a resistive common mode detector; comparing the output to some desired VOCM and feeding it back to CMFB 2. So, this is same as that one.

Now, as usual we may have to use a capacitor here so, that the common mode detector works properly for high frequencies. Now this is the exactly the same as what we were doing earlier; so, I will not go into the details of that again. So, far we have looked at a couple of ways of stabilizing the common mode voltages in a two stage Op-Amp all of them involve separately stabilizing the first stage output common mode voltage and the second stage output common mode voltage. This is in fact, the preferred way to do it there is a way to have a single loop that stabilizes both common mode voltages, we will look at that shortly, but it is a little more messy to stabilize and its much simpler and generally it does not cost much to stabilize the common mode of each stage separately.

Now, the first stage output common mode voltage has to be of the right value to bias the second stage. So, that can be done by using replica transistors in one way or the other; the final output common mode voltage is usually close to VDD by 2 because in two stage Op-Amp we are also generally interested in supporting a large output swing.

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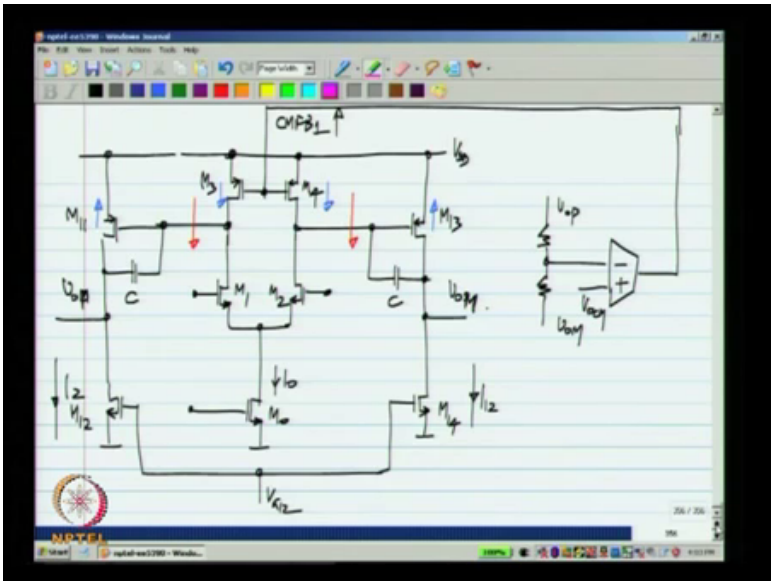

Now, let me consider the two stage fully differential Op-Amp again and let me go back to the topology where the current source here carries a current I naught which is exactly the tail current required for the differential pair. Now what we were earlier trying to do was or what we always try to do in common mode feedback is to make the currents from M 3 and M 4 equal to the current from M 0. Similarly currents in M 11 and M 13 equal to the currents in M 12 and M 14.

The way we went about it was we adjusted this current in M 3 and M 4. So, that it becomes equal to whatever is in M 0 and the current in M 11 and M 13 were set to some fixed values by adjusting the common mode output voltage of the first stage. Finally using a second common mode feedback circuit; we adjust at the current seen M 12 and M 14 to be equal to that of M 11 and M 13.

Now let us say we have fixed current sources at the bottom in the second stage; let me call it V G 12. So, this means that a certain fixed current I 12 is going through both these transistors if they happen to be in the saturation region. Now, what do we need to do the first stage remains the same I have to adjust this voltage until the current in M 3 and M 4 becomes equal to current in M 0.

Now the second stage the current in M 11 and M 13 must be made equal to that of M 12 and M 14. Now how would we control the current in the current in transistors M 11 and M 13. If you observe let us say I change this voltage; let me call that CMFB 1 now what happens is let say I increase this voltage; the currents in M 3 and M 4 will reduce and the output voltage here will reduce. Because the currents in M 3 and M 4 will reduce these node voltages will be pulled down.

Now, because these voltages are pulled down the V S G of M 11 and M 13 are increasing; so, the currents in M 11 and M 13 will increase. So, you can see that this voltage CMFB 1 controls the current in M 3 and M 4 as well as the currents in M 11 and M 13. So, it looks like we do not need two nodes to control these two, we can perhaps just control only this single voltage CMFB 1 and adjust the output common mode voltages, stabilize the output common mode voltages of both the stages.

And the way to do that is let us say this is V o p and V o M sorry V o p and V o M, we detect the common mode voltage as always using a resistive divider and compare this to a certain value VOCM and let the output continuously increase or decrease CMFB 1.

Now, what happens here is that let us say the output common mode voltage V o p and V o M; the average of the two is too high. Then what should happen is that the output voltage must be lowered so; that means that the current in M 13 and M 11 must reduce. That means, these gate voltages must increase which in turn means that CMFB 1 must reduce.

So, we need a trans conductance of that polarity over there trans conductance or an amplifier that is if V o p and V o M are too high; this should be become small V o p and V o M are too low this should become larger by the way I should add the integrating capacitors here. Now, in the common mode half circuit let me redraw the common mode half circuit of this.

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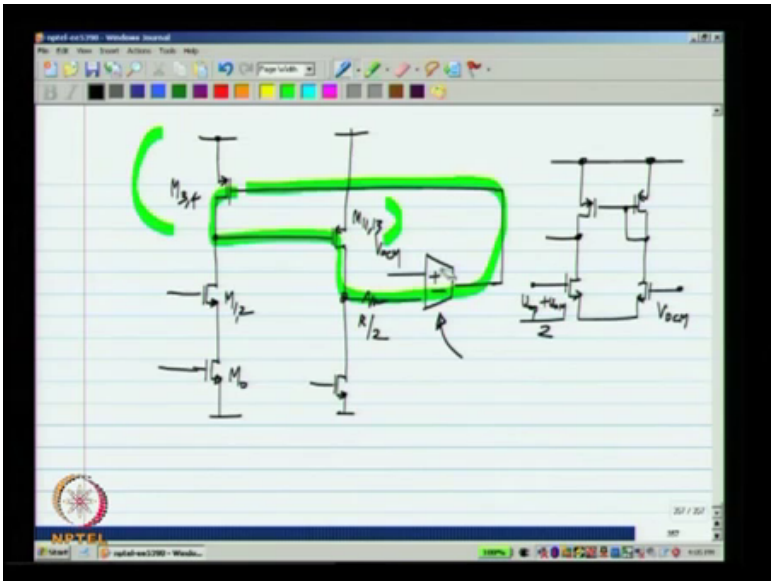

What I will have is is that one we have R by 2 over there and VOCM. Now you see that this feedback loop has a common source amplifier M 3 4, another common source amplifiers M 11, 13 and this trans conductor or an amplifier. Now we have not yet said what amplifier it is, but if we use what we have been using all along that is a single ended single stage Op-Amp will have 3 stages in feedback a single ended single stage Op-Amp followed by a common source amplifier followed by another common source amplifier.

Now, this looks like a 3 stage Op-Amp and you know that a 3 stage Op-Amp makes like a two integrated capacitors. So, it is a more complicated thing to stabilize a 3 stage Op-Amp compared to a two stage Op-Amp. So, we would not like to get into that complication; so, usually what is done is to use not an Op-Amp in this place, but use a low gain amplifier. Normally perhaps we would have used something like this ok; this gives the output.

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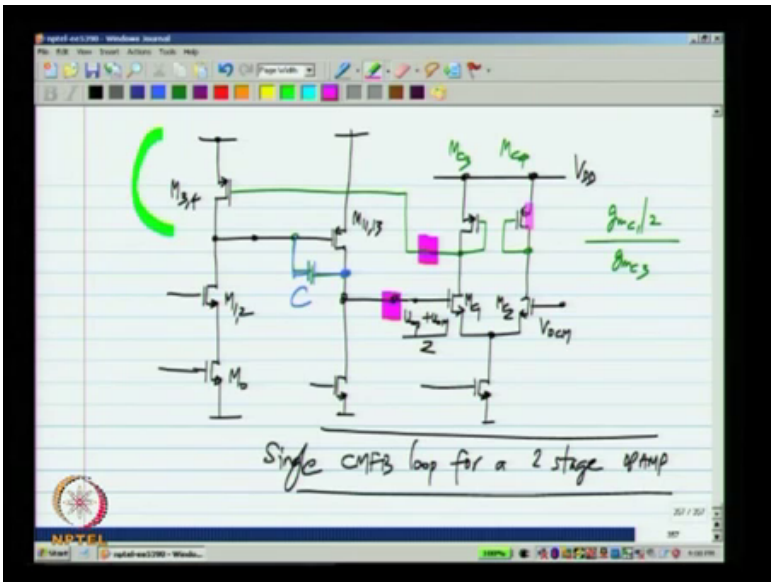

and if we use this the main problem is that the it is possible to use this something like that.

So, then we need to have an integrating capacitor over there and then we need to have an integrating capacitor over there. And the integrating capacitor of the main Op-Amp will be over here. Now all this becomes quite complicated to stabilize; so, what is normally done is not to use an Op-Amp in this trans conductor, but use some amplifier that has a positive incremental gain and it is very easy to make a low gain amplifier all that is done is to do this.

Now, you know that the diode connected transistors have an impedance of 1 by g m. Now this is like a differential pair loaded by 2 resistors whose value is 1 over g m ok; if I call this M C 3 and M C 4; the gain from this point to that point will be simply gmc 1 divided by 2 divided by gmc 3. So, then the equivalent circuit will have a low gain amplifier with some parasitic pole and common source amplifier M 3 4 and a common source amplifier M 11 13.

Now, this is lot easier to make stable and in fact, many times the integrating capacitor used for the main Op-Amp; you see now that that also appears in this big feedback loop. So, let us imagine that the gain from here to there is almost 1; it is a ratio of g m it is close to 1. Then we have this M 3 4 and M 11 13; so, the same integrating capacitor will also act as an integrating capacitor for the common mode feedback loop.

So, it is possible to use a single common mode feedback loop for a two stage Op-Amp. In that case you have to reduce the gain of the trans conductor that you use so, that you do not get into very complicated 3 stage stabilizing networks, but also even if it is possible it is not very commonly done its not advisable.

Because now you have too many constraints you have some integrating capacitor for the main Op-Amp, for the differential picture; you have to use the same thing for the stabilizing the common mode feedback loop as well; that means, that the g m of M 3 4 has to be constrained in some way. So, this just adds too many constraints and its usually much simpler to use separate common mode feedback circuits for the two stages of a two stage Op-Amp.

So, that kind of brings us to the end of common mode stabilization circuits; like I said there is a huge variety and in the exercises there will be many problems that you can try and solve. There are also lots of references on common mode feedback networks; now this can be extended further if you want ah 3 stage Op-Amp with common mode stabilization, you can choose to stabilize the 3 stages separately that is usually the easiest thing to do.

Now, what we will look at very quickly is the difference between truly fully differential circuit and simply putting two identical circuits next to each other. We have been talking about how differential circuits are good you transmit signals and two wires and measure the voltages between them and each wire acts as a reference for the other wire.

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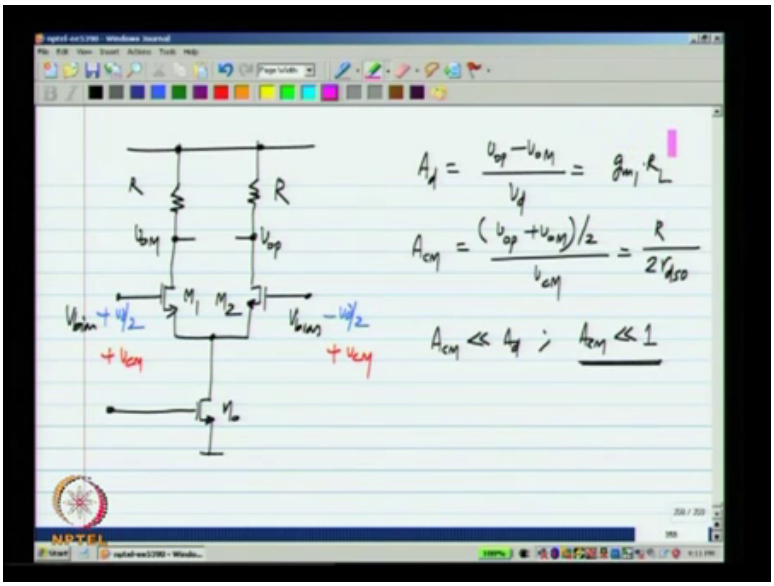

Now, the question that naturally occurs is I said that this is a differential circuit. I will show an ideal current source here, but even if with a real current source it works properly. And to the bias I could have a differential input that is plus V d by 2 and minus V d by 2 or a common mode input plus V C M and plus V C M let me say the load resistors are R.

Now, the differential gain of this amplifier which is V o p minus V o M by V d we know is g m 1 times R L a common mode gain of the amplifier which is V o p plus V o M by 2 divided by V C M this again we have worked out it is R by 2 times r d s 0. The important point here is the A C M is much less than A d and also A C M is much much less than 1; it is required as well usually it is not enough to have it to be much smaller than A d; you also need it to be much smaller than 1.

Now, this looks like we have already said that this differential pair is the differential version of a common source amplifier and that is reflected in the gain as well.

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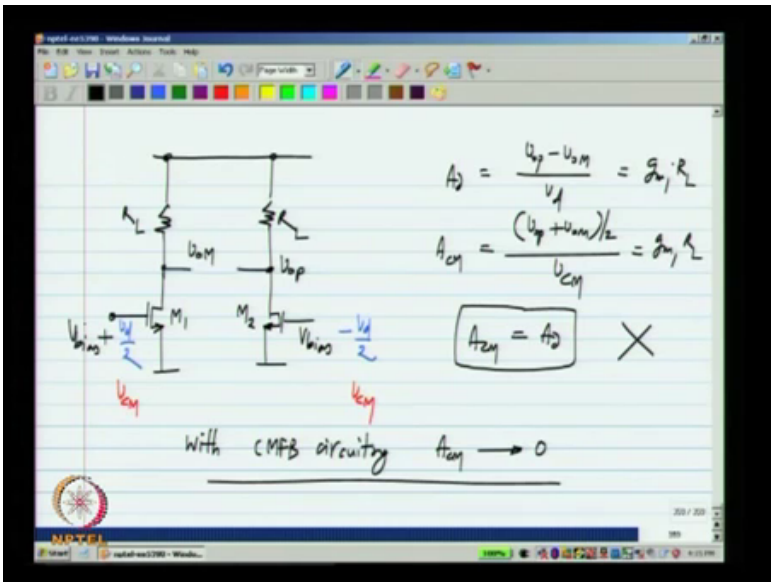

Now let us say I just put two common source amplifiers next to each other and I apply some V wires. So, that it has the same g m as before and let us say I apply V d by 2 and minus V d by 2 we can also try applying a common mode voltage.

Now, what happens now let me call this V o p and this V o M; the differential gain V o p minus V o M by V d equals g m 1 R L. And if you look at the common mode gain which is V o p plus V o M by 2 divided by V C M that is also g m 1 R L because each circuit operates independently whether I have V C M here or V d and minus V d it does not matter. If I have equal voltages on two sides the output will still reduce. So, in this case A d A C M equals A d. So, this basically is what makes the circuit useless for a fully differential operation. It is not enough to have two wires to carry the signal ok; so, finally, you have to respond only to the difference between the voltages on the two wires that is the essence of two fully differential operation.

So, if you have a chain of amplifiers even if every stage does not have common mode rejection; that is every stage does not have its differential gain much more than the common mode gain, there has to be something at least at the end which has sufficient common mode rejection. The differential pair is one such circuit; now when you put two circuits together like this the common mode rejection is 0 DB that is the differential gain and the common mode gain are the same and such circuits are known as pseudo differential circuits.

Now, you can use pseudo differential circuits if you think about it the second stage of our fully differential Op-Amp two stage Op-Amp is a pseudo differential circuit we simply put two common source amplifiers together, but the reason the whole of Op-Amp works is because we have two amplifiers in cascade and the first stage rejects the common mode signal. So, that is one thing also secondly, even the second stage has common mode feedback circuitry.

So, now if you let us say had current sources instead of these resistors and control them with common mode feedback circuitry; A C M would become much smaller than A d because the whole idea of the common mode feedback circuitry is to hold the output common mode voltage constant. So; that means, that A C M should become 0 with common mode feedback circuitry.

In reality it will be some small number we cannot simply put two circuits next to each other and use them as fully differential circuits. We will have to either have inherent common mode rejection like the differential pair does or we have to add common mode feedback circuitry which will kill the output common mode signal or we have to do both.

Thank you, I will see you in the next lecture.

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