

Analog Integrated Circuit Design
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Lecture – 42
Fully differential opamps

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Analog Integrated Circuit Design—Lecture 42

Fully differential opamps

- Fully differential single stage opamp—frequency response and offset
- Common mode detector
- Fully differential two stage opamp

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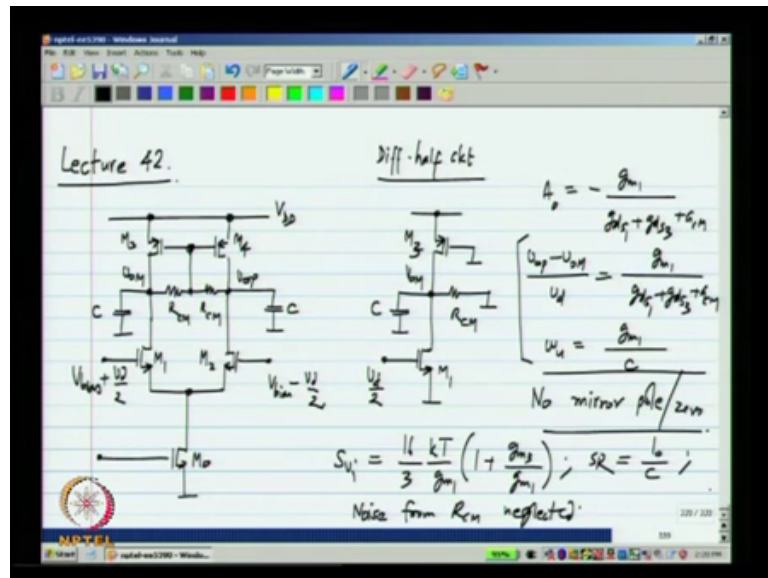
Nagendra Krishnapura Analog Integrated Circuit Design

Hello and welcome to lecture 42 of analog integrated circuit design. We were in the middle of discussion on common mode feedback circuits. The common mode feedback circuits can be very simple, in which case probably not much more is to be done. The components in the opamp stabilize the common mode feedback loop as well. Sometimes when the common mode feedback circuit is complicated, you have to take some special steps to stabilize it.

In either case the common mode equivalent circuits, the common mode half circuit looks like yet another feedback loop which could look like either one or two stage opamp ok. We have seen examples of both.

Now, in this lecture what we will do is, look at some other kinds of common mode detectors and see how to use them in feedback

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. So, first a quick review of very simple, this is the fully differential single stage opamp, when this part is the trans conductor and when loaded by capacitors, it becomes an opamp. These are the two register are the common mode feedback detector. Now the differential equivalent circuit is very simple ok.

So, the differential equivalent circuit, differential half circuit has a DC gain; that is from V_d by 2 to V_{OM} of minus g_{m1} by g_{ds1} plus g_{ds3} plus G_{CM} . Now when you have the full circuit at this voltage you will get minus of V_{OM} with the fully differential exudation, and the gain remains the same; that is the gain V_{OP} minus V_{OM} divided by V_d will be equal to g_{m1} by g_{ds1} plus g_{ds3} plus G_{CM} ok, and the unity gain frequency will be g_{m1} by C ok.

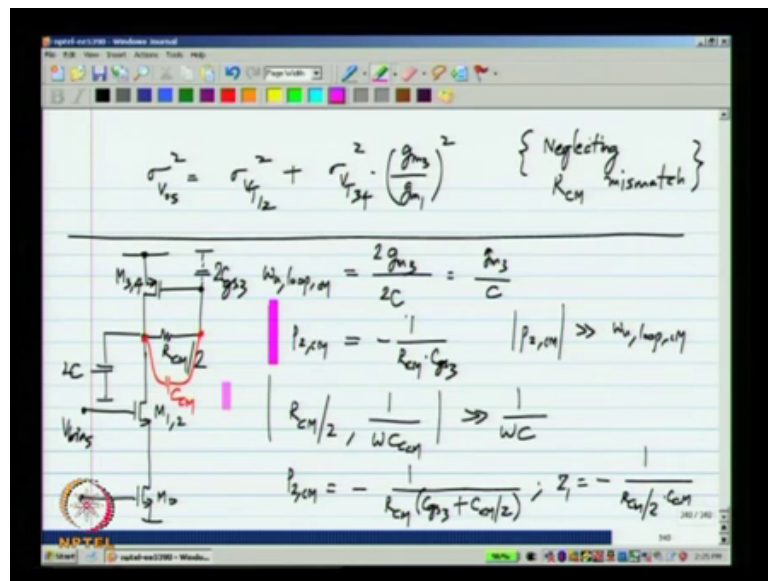
The C includes the load capacitance that you have plus any parasitic capacitance occurring at this node. Now in fact, this transfer function is simpler than what we had for the single stage, single ended opamp. If we recall in the single stage single ended opamp, we took the current of M_1 mirrored it and the output was taken from this side. Now because the current mirror has some pole in its frequency response half of the current was going through some pole and the other half will coming directly. So, we had this mirror pole and zero.

In the fully differential single stage opamp we do not have any such thing ok. So, that is actually an advantage of the fully differential single stage opamp and the other thing

remain the same ok. So, the noise we have already calculated, the input referred noise turns out to be exactly the same as what we had in the single ended opamp. I am not going to work it out here, but we have already looked at how to calculate the noise of the fully differential circuit. From the differential half circuit we just have to calculate the input referred speckled density or the output voltage noise speckled density, and then double it to get the corresponding quantity in the fully differential circuit.

Now, in this case we also have RCM which creates noise, but I neglected the noise from RCM and the slew rate will be limited by I_{tail} / C , because all of I_{tail} flows into M_1 or M_2 and the rate of change of the output voltage will be related to I_{tail} and the capacitor C . And finally, the offset again will be similar to what we had in the single ended single stage opamp.

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It will be equal to σ_{VT}^2 plus this is the mismatch between the transistors M_1 and M_2 plus the mismatch between the transistors that formed the load times g_{m3} by g_{m1} square ok. Again I have neglected the contributions from R_{CM} mismatch, well contributed to the overall offset, but because the value of R_{CM} is so large that it can be neglected.

And the common mode half circuit of this which we also discussed earlier, there will be a parasitic here. Now in this loop the integrator is formed by the g_m of M_3 and M_4 and these capacitors $2C$. So, the unity gain frequency of the common mode feedback loop is

gm 3 by C, and there is parasitic pole due to this R and that C ok. And this C is nothing, but 2 times Cgs 3.

So, this is and the left half plane of cause and minus for this is RCM by 2 RCM times Cgs 3 and we would like this to be at a frequency much more than the unity loop gain frequency; otherwise what happens is when you have a common mode excitation the output will ring. Now, there is the way to fix this and that is to have a capacitor CCM across RCM that is if the pole happens to be at a low enough frequency. Then you will have ringing, you will have poor phase margin in the common mode feedback loop the way to fix it if you have this capacitor which adds zero or a negative delay.

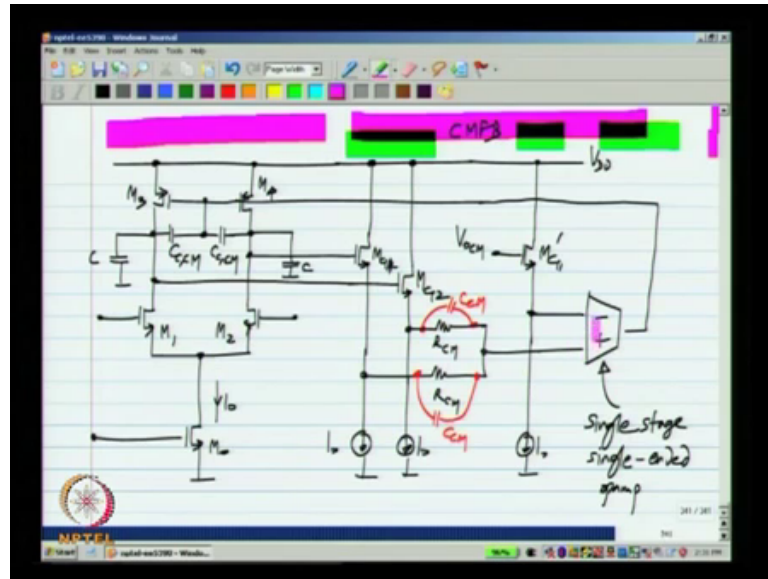
So, in that case you can again calculate the poles and zeros ok. Now the pole and zero calculation in this case is a little complicated, but what I will assume is that the impedance of RCM by 2 and the impedance of the CCM are much more than the impedance of the load capacitors.

Because what happens is, when you have this coupled RCS, we have this C and then R and then you will have some poles which cannot be calculated. So, simply even this is an approximation, when this part of the circuit as a very high impedance, insignificant current is drawn from this and we can act as though this circuit is isolated from that part ok. Now if this is not the case then you have to go on calculated exactly ok.

. So, in this case we can calculate the pole and zero and the zero is at and from all of this, you can calculate the phase margin in the loop gain function and make sure that, it is sufficient. There are many ways to calculate the stability of this. We have seen circuits like in other occasions; like when you calculate the frequency response of a common source amplifier we have a similar circuit with a capacitance from the drain to ground the capacitance, from the gate to ground and a capacitance between gate and drain ok.

Ah we know where the poles are. In such a situation there will be poles splitting and so on. So, then we can calculate what the close loop poles will be and whether the circuit is stable or not, and a simple feedback circuit like this, is almost guarantee to be stable. You do not have to work too hard to make it stable or to eliminate ringing and things like that.

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Now, we have discussed the other circuit quite extensively that is when we have a fully differential, fully differential circuit and let me show it right here. We could make a common mode detector with buffers so that the fully differential opamp is not loaded and you use a trans conductor to complete the feedback. Previously I had used the opamp symbol here, but it really a trans conductor, you do not make a full placed opamps in this case ok, it is really a trans conductor, because it has a high output resistance.

now in this case when the common mode feedback loop works properly, the common mode of these two voltages will be said to V_{OCM} M_{c11} M_{c12} and this M_{c11} prime are identical to each other ok, and we have this R_{CM} and R_{CM} here and we usually also have this capacitors C_{CM} to make sure that there is an too much delay in the common mode feedback loop.

We also have to have miller integrating capacitors in the common mode half circuit; it appears between the gate of M_3 M_4 and the drain ok. So, in the fully differential circuit it will appear between the gate of M_3 and M_4 and each of the drains ok, something like this. And finally, the actual load of the opamp will be here C and C . So, now, the circuit looks very complicated, but its not this part of, it constitutes the fully differential single stage opamp and M_3 and M_4 should act as COM constant current source in differential mode.

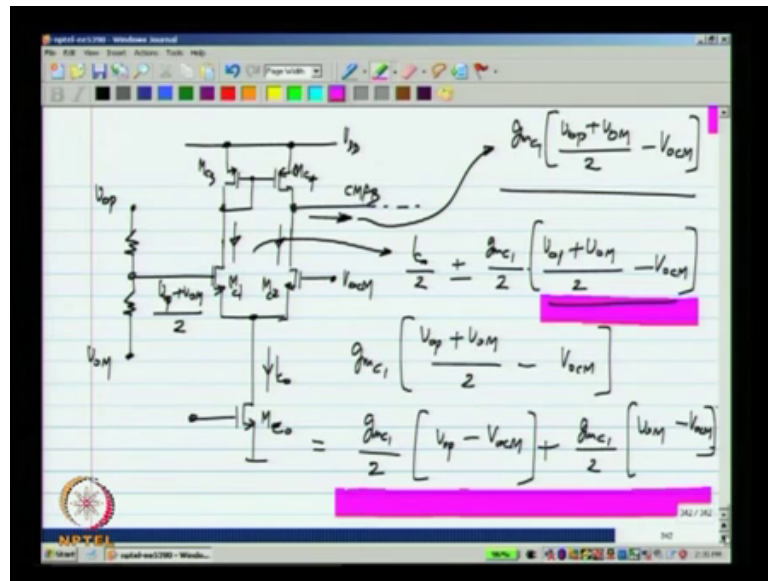
Now the rest of it for common mode feedback and this part is for detecting the common mode, this for the replica and this is for feeding the back to the gates of M3 and M4 and these are for stabilizing the common mode; that is to make the loop gain of common mode feedback loop, look like an integrating function and the many parasitic poles here and also zeros, and also in the implementation of this, which is the single stage, single ended opamp there will be parasitic poles and zeros and they have to be adjusted. So, that you have sufficient phase margin in the common mode feedback loop gain

Now the moment you add this CC CM in this fashion what happens is in the differential mode, there will load the, there will load the opamp, because in the differential mode this point is at ground and CC CM will appearing parallel with C. So, you have increase the load capacitance of the opamp. It will reduce the unity gain frequency, but we need this integrating capacitors or compensation capacitors to make the common mode feedback loop stable. We need to have these capacitors and that will invertible add to the load capacitance, we just have to lower than.

Now if you minimize the delays in other parts of the circuit you do not need to large capacitors here and they can be made as small as you wish ok, making new smaller. We will reduce the excess load on the opamp ok. Now, let us look a couple of different kinds of common mode detectors ah. In general the scheme with every common mode detection and feedback is the same, you detect the common mode and you compared to some reference value and then you feed it back. Here we needed a replica, because the common mode detectors has this voltage drop V_{GS} ok.

Now some of all of these can be merged together, the comparison may not be; obviously, visible that was the case with the simple circuit. We are not comparing it with any reference that we provides from outside, but the comparison is happening with the gate source voltage of the value of M3 and M4 ok. So, the output common mode will set itself to V_{DD} minus the gate source voltages of M3 and M4. Similarly this part the single stage, single ended opamp could be merged with the common mode detection ah. Let us say an example of that. Now for this illustration I will use the common mode detector without buffer ok

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This is because it is just more complicated to draw, but you will get the point even without the buffer. The part that I am going to draw now is a common mode detector itself plus the single stage single ended opamp used for feedback. So, this is the common mode feedback that goes to M3 and M4 ok.

Now, sorry these are \$I_{C0}\$, \$I_{C1}\$, \$I_{C2}\$, \$I_{C3}\$ and \$I_{C4}\$ or the current that gets pushed out of this, can be calculated the voltage at the gate of \$M_1\$ is \$V_{op}\$ plus \$V_{om}\$ by 2 and the current here. And there will be let me call this \$I_{C0}\$, it will be \$I_{C0}\$ by 2 plus or minus \$g_{m1}\$ by 2 times \$V_{op}\$ plus \$V_{om}\$ by 2 minus \$V_{cm}\$ ok.

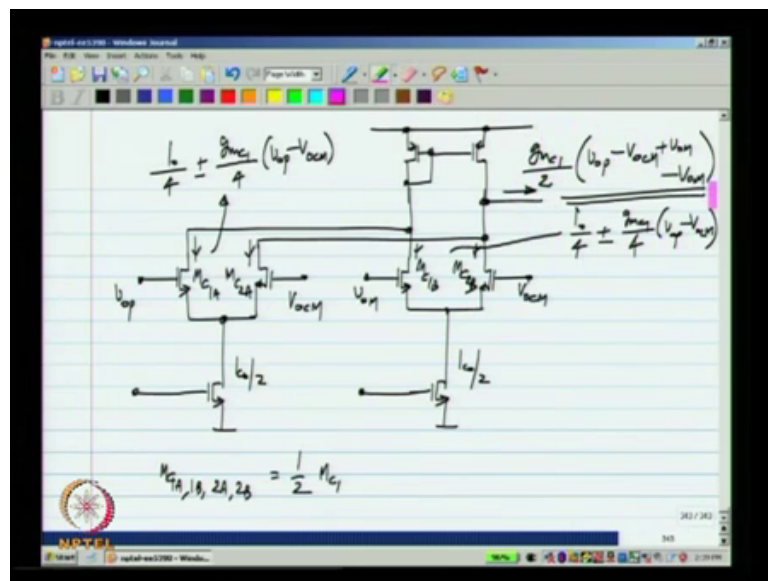
So, this part of it is the input to the differential pair \$M_1\$ \$M_2\$ that times \$g_{m1}\$ by 2 is the current in each of these transistors, and the total current output the bias component will be removed and this will be a doubled ok. So, this will be nothing, but \$g_{m1}\$, \$V_{op}\$ plus, sorry \$V_{op}\$ plus \$V_{om}\$ by 2 minus \$V_{cm}\$ that is the current that tends to flow here. If there is a load, remember this is going to the gate of the transistors in steady state. There will be no current there, but that is the current that tends to flow through the parasitic capacitance that is at that particular node ok.

Now, any other circuit arrangements the gives us same current will work equally well between \$V_{op}\$ and \$V_{om}\$, and the output current we need to have the same transfer function. Now how else can be do this. First of all we see that here we have \$g_{m1}\$ times \$V_{op}\$ plus \$V_{om}\$ by 2 minus \$V_{cm}\$ and this can be rewritten as \$g_{m1}\$ by 2 \$V_{op}\$ minus

$I_{D1} = \frac{I_0}{4} + \frac{g_{m1}}{4}(V_{op} - V_{ocm})$ and $I_{D2} = \frac{I_0}{4} - \frac{g_{m1}}{4}(V_{op} - V_{ocm})$ is not here, it has $I_{D3} = \frac{I_0}{4} + \frac{g_{m1}}{4}(V_{op} - V_{ocm} + V_{om})$ and $I_{D4} = \frac{I_0}{4} - \frac{g_{m1}}{4}(V_{op} - V_{ocm} + V_{om})$ ok

So, now each of these is a certain different voltage, this is between V_{op} and V_{ocm} and between V_{om} and V_{ocm} and we know that we can generate currents which are of this form by passing this differential voltage to a differential pair ok

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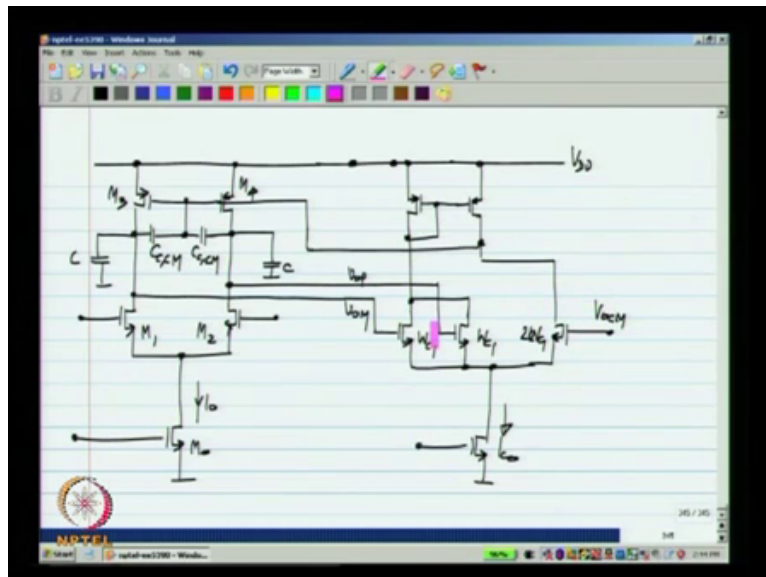
. So, what I will do is, I will have two differential pairs V_{op} and V_{ocm} , V_{om} and V_{ocm} and I add up the currents. Let us I have $I_0/2$ flowing here, $I_0/2$ flowing there and then these transistors; let us say each of these transistors is half the size of the M_{C1} used in the previous circuit ok. So, we have half the current of before and half the device has us before when I say half of M_{C1} half the width ok. So, the g_m of these transistors is $g_{m1}/2$ ok.

So, what happens is, in each of these will be a differential current. Now these two currents will be $I_{D1} = \frac{I_0}{4} + \frac{g_{m1}}{4}(V_{op} - V_{ocm})$ and in these two transistors, it will be $I_{D2} = \frac{I_0}{4} - \frac{g_{m1}}{4}(V_{op} - V_{ocm})$ and we mirror this current as usual to remove the bias component, but if you calculate the total current that tends to flow out of this, if there is a load capacitance or a voltage source will be the bias, current sources will cancel out and will have $g_{m1}/2(V_{op} - V_{ocm} + V_{om})$ minus V_{ocm} plus V_{om} minus V_{ocm} ok. This is exactly the current that we had earlier. We had this plus that one which gives you the same expression as this.

Now, this is the circuit in which the common mode detection and the trans conductor are merged together. What we have done is? we have taken the single stage single ended opamp and split up the input transistors pair into two parts and also made the tail current half, basically the differential pair is split into two halves. So, each half has half the gms before ok, the one of the differential pairs.

We apply VOP and VOXM to the other one, we apply VOM and VOXM and finally, when you add up all the currents together what you will get? You will be $g_{m1} \times 2 \times VOP + VOM - g_{m1} \times VOXM$ ok. This is exactly the quantity that we wanted. So, this circuit can also be used for common mode feedback circuitry. And how do we use that let me copy this over. So, I will remove all of this stuff.

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This is one of the differential pairs and this is the other differential pair add up the two currents together and whether in to the other side, I also add up these two currents ok, and this is the output of the single ended opamp, which is used for common mode feedback. So, we complete the feedback loop in this way. The rest of the circuit remains this same. The CC CM is the integrating capacitors if you want to think of it that way.

Alternatively, you can think of it as providing feedback around M3 and M4 high frequencies ok. For low frequencies the feedback goes through the complicated circuitry which as high DC gains for high frequencies. The feedback around M3 and M4 is close through CC CM, this is VOP and that is VOM. So, this also works equally well and

again, because we have connected gates of MOSFET to the differential pair, there is no resistive loading of the differential pair and the DC gain is not compromised.

So, we can think of a lot of circuit like this. I will quickly discuss one minor variant which is actually more frequently used. Now if you look at it, imagine the quiescent condition where both V_{OP} and V_{OM} are equal to V_{OCM} , then this voltage and that voltage will be the same ok, so you can simply connect those two together. In that case you see that this transistor and that transistor are in parallel, the gate is at V_{OCM} , the source is the same and the drains are also connected together.

So, I will redraw this differently, I will show these two transistors like this and they are added together and this transistor which is of twice the width. So, this is W_{c1} and W_{c1} , this will be $2W_{c1}$ and the total current is I_{C0} ok. So, this circuit is the same when the opamp is in quiescent condition, when V_{OP} and V_{OM} are equal to V_{OCM} . Now it turns out that this circuit has some advantages when V_{OP} and V_{OM} are different from V_{OCM} , how the circuit behaves and so on ah. It is somewhat advantages to have this circuit with the two sources tied together than the previous one.

So, this circuit is also use quite often and it has the same benefits of not loading the differential opamp ok. It does not load the opamp in the differential pictures. So, this also is some circuit which has a merge ah, in which the common mode detection and the trans conductance are merged together ok. Now, there is the use, variety of common mode feedback circuit and you can think of your own circuit as well. So, I will not going to the details all of that ah, we have looked at a couple of them and we will use it for the $n=2$ stage opamp as well.

There is one more common mode feedback circuit that will discussed, but in general the principle is the following; that you have two current sources; one on top, one on the bottom and you have to adjust one of them. So, we need a variable current source and one easy way of doing that is to have a MOS transistor and various gate voltage; that is what we went doing so far. Now, there are many other variants as well, you can have a degenerated current sources and where is the degeneration resistance that gives you yet another type of common mode feedback circuit.

And similarly the common mode detection and the way you amplify the difference between the detected common mode and the reference voltage can be very different. So,

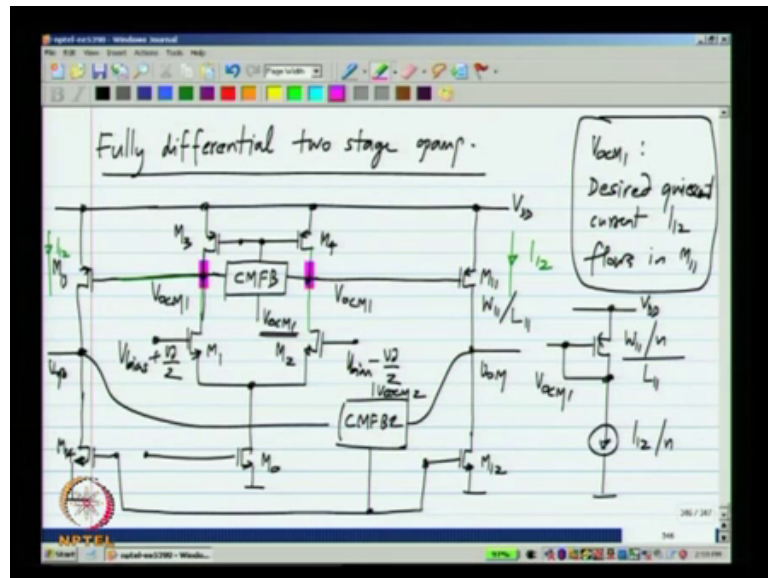
by combining all of these you can easily come off with many many common mode feedback circuits ok. Now exactly which one you use, depends on the details like the signal range over which the circuits operate, how stable they are how fast they are so on ok.

So, we have discussed the single stage fully differential opamp quite extensively. Now the differential picture is extremely simple. In fact, it is simpler than the single ended single stage opamp, because the mirror pole and zero go away and this behaves like truly single pole system ok, with the pole very close to the origin; that is it behaves more or less like an integrator and all the other differential characteristics also we have calculated.

Now, what we will do is, go on to the two stage opamp which we said was improvement over the single stage of opamp. I am not going to discuss the cascode opamps in detail; like cascode opamps are nothing, but the single stage opamp with each transistor replaced by a cascoded transistor ok. So, the common mode feedback works exactly in the same way for a cascode amplifiers, as it does for the simple differential pair opamp and all the arguments that we made so, for apply also to the cascode amplifiers. So, I will not discuss it further, you can make either the telescopic cascode or the folded cascode fully differential very easily ok.

All you have to do is, to add a common feedback circuit in the manner that we just described. And as with a single stage opamp if you have resistive loading because of the common mode detection circuitry that will compromise the DC gain, your constraint to use common mode detectors which present a high impedance; that is basically the gate of a MOS transistor. So, besides that there is nothing special about common mode feedback circuit for telescopic and folded cascade amplifiers I am assuming that you will be able to work it out yourself.

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Now, we will go on to fully differential two stage opamp now let me first draw the single ended two stage opamp. This is the first stage with a differential input and the second stage is a common source amplifier and we can connect some load to this point. Now when we make it fully differential the output also must be differential. So, first of all the first stage will not be a differential to single ended converting stage like this, it will also be fully differential; that is the inputs and outputs are fully differential ok.

And to make the second stage differential we need to add a counterpart to M 11. Let me call it M 13 and this is M 14 and the bias for this has to be properly adjusted, so that the currents from these to equal the current in this similarly, the bias for M 12 and M 14 as to be properly adjusted. So, that the currents an M 12 and M 14 exactly equal the currents in M 11 and M 13, and this doe using common mode feedback. So, what I have here is a fully differential two stage opamp, but showing only the differential signal path components ok. I will not added the common mode feedback circuitry.

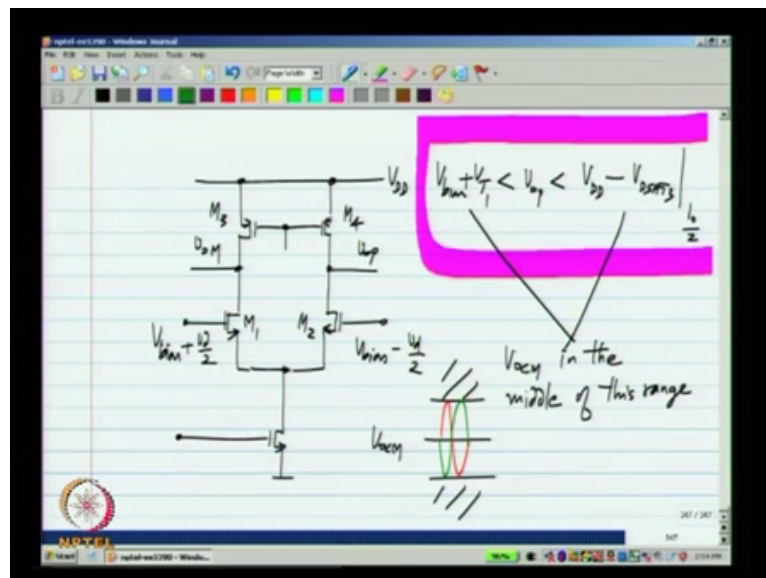
Now we need common mode feedback to the first stage and the second stage right. in both stages the current, from the top and the currents from the bottom has to be exactly equal to each other ok. So, we will see how to do the common mode feedback for this particular opamp. There are now many more options ok. One possibility is we starts with a, remember the first stage here. This is a single stage fully differential opamp, write this part of it, so we can start with making the single stage fully differential opamp with

common mode feedback that is I will show this as a box, this box includes common mode detection and feedback and the feedback as you know finally, comes to the gates of M3 and M4 ok.

Now we look at the details of this, but the common mode feedback circuits that we have discussed so far, we will work perfectly well. So, now the output common mode of the first stage is stabilize ok. Now only thing to figure out is what the output common mode is stabilized too; that is the value of VO_{CM}. Now before let us say we had this particular circuit.

In this case the output common mode voltage will be equal to VO_{CM} ok, what should be the value of VO_{CM} we did not discussed that, but it is kind of straight forward. There will be certain output swing limit for the fully differential opamp ok. Now VO_{CM} should be in the middle of that range, so that you can swing the maximum possible ok. I did not discussed the swing limits of the fully differential single stage opamp, but again it is quite simple not showing any of other details.

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This is how it will be operating and outputs are here. We know that if VOP becomes very large M4 goes into saturation or M3 if VOM becomes very large. Similarly VOP becomes very small either M1 and M2 going to try out region that is a VOP becomes small try out region, if VOM become small M1 goes into try out region ok. And the limits are straight forward. The limit on VOP is VDD minus V_{d sat 3} for a current of I

naught by 2 on the upper side and on the lower side it is $v_{bias} + V_T$ of M1 and M2 ok.

i am assuming that the signals being V_d is so small. So, it does not affect the limit ok, so this is the case. Now in quiescent condition VOP and VOM will be equal to VO_{CM} and we should said VO_{CM} to be in the middle of this range. So, that this is VO_{CM} and you have the maximum possible room for VOP and VOM ok; that is the idea. So, that is how you have select VO_{CM}.

Now, we have the fully differential two stage opamp and we assume that first stage has a common mode feedback circuit; that is the first stage is a fully differential single stage opamp with its own common mode feedback circuit. Now what should be the quiescent and output voltage of the first stage? We need a certain bias current, let us say I_{12} in the second stage ok, the common mode voltage at the output of the first stage equal to the VO_{CM} and VO_{CM} produce the certain current in M 11 and M 13 in the quiescent condition and that should be equal to the desired bias current in the second stage ok.

I hope that this part is clear in the single ended two stage opamp, what happens is? We have differential pair with a current mirror and that drives a transistor M 11 and M 12 is a fixed current source. When you put the opamp in feedback the current will M 11 becomes equal to the fixed current source supply from the bottom. When you have a fully differential two stage opamp, the situation is different ok. Now in this case the first stages is fully differential single stage opamp and its output produce certain current in M 11 and M 13 and we should using another common mode feedback circuit, make sure that M 12 and M 14 carry the same current ok.

They are not current sources at the bottom in this particular arrangement of the two stage opamp. So, VO_{CM} for the first stage let me call it VO_{CM1}. VO_{CM1} must be such that the desired quiescent current I_{12} flows in M 11 ok, and how do we produced that VO_{CM1}. So, let us say we make a replica of M 11, let us say M 11 has a certain width by certain length. Here we make let us say some multiple of that width divided by l_{11} , and we bias it with a current I_{12} divided by N ok; that is the desired current in M 11 is I_{12} .

Here we put I_{12} by N just to save of current and then we also have a transistor whose width is 1 over N times width of M 11, and then we die out connected ok. This will

provide V_{OCM} , because we know that if this V_{OCM} the voltage here were directly applied to the gate of M_{11} . The current in this would be the exactly equal to I_{12} , the desired value of I_{12} ok. Now, this is not directly applied to M_{11} , what is happening is this, V_{OCM} goes to the common mode feedback circuit and value here and there in quiescent condition when V_{d0} will be equal to V_{OCM} and that will give us the desired current. So, basically this V_{OCM} is not something that we independently said to be some absolute voltage, but we derive weight using a transistor level circuit ok.

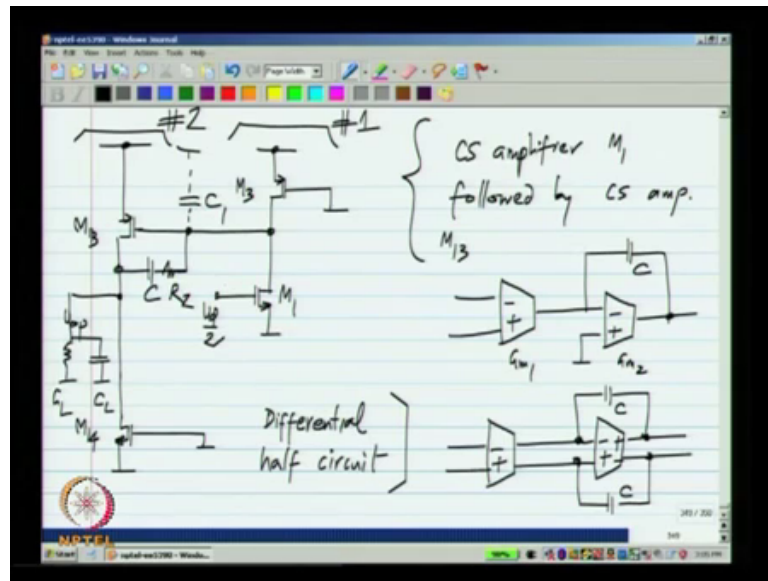
Now, this is another example of replica, we have to adjust V_{OCM} . So, that the output stage carry the certain current and we cannot put it to a voltage source and adjusted and hope to ah, hope to give the right current, because changes in transistor threshold voltage and current factor will give you different currents if you bias the gated a fixed voltage. So, you have biased with the current mirror basically ok. So, that is all, that is straight word.

Now that V_{OCM1} is derived like this. Let me correct these things, its V_{OCM1} , the output as to be again common mode stabilize the output stage. So, the gate voltage of M_{12} and M_{14} must be adjusted using another common mode feedback loop and what is this now? It calculate the common mode voltage of the output, let us say this is V_{OP} and V_{OM} and it will have some common mode voltage which will set the output common mode voltage to the desired value, and what is the desired value.

Again we look at the signal swing limit of the output stage and we said the common mode voltage V_{OCM2} to be in the middle of that stage ok. Now we will see how to realize this common mode feedback circuit. Now before we go into the details of the common mode feedback circuit of the two stage opamp, let us quickly go through the differential half circuit of the two stage opamp to avoid clutter, I will remove the common mode feedback circuits from this. We know that the common mode feedback circuits do not play a role in the differential picture, they may add load to the differential picture, but that is about it ok.

This is the point to which we apply the common mode feedback of the first stage and here is the common mode feedback of the second stage. Now, in the differential half circuit what do we have? We have this point to be ground and that point to be ground and also this point to be ground.

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So, we will have M1 with its source grounded M3 with its gate grounded, and this is M13 and M14 ok. So, this is the output. So, this is the posting input V_d by 2 and this is the output VOP. This is the differential half circuit of the fully differential two stage opamp, this is the first stage and here we have the second stage ok.

As before the differential half circuit is extremely simple, we have a common source amplifier M1 followed by common source amplifier M13. Now to make a two stage opamp we need to have the integrating capacitor here that I did not show earlier so that in there in the complete circuit it will appear here and there ok. Now in terms of trans conductors the single ended two stage opamp looks like that. This is g_{m1} and that is g_{m2} . Now the fully differential one looks like that. So, it is just a fully differential version of the same circuit.

. So, this circuit is again extremely easy to analyze. Now, because of the symmetry we do not have the mirror pole and zero in the first stage. In a single ended two stage opamp you have that, because first half of the current is mirrored, in this case you do not have that. So, the transfer function of this is lot cleaner than single ended two stage opamp. Now I want workout these thing, but you already know ah, we have analyzed the extensively the frequency response of a common source amplifier M13 with a capacitor C between its drain and gate ok

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$$A_{vo} = \frac{g_{m1}}{g_{s1} + g_{s3}} \cdot \frac{g_{m13}}{g_{s13} + g_{s14} + g_L}$$

$$\omega_u = \frac{g_{m1}}{C}$$

$$p_2 = \frac{g_{m13} \cdot C}{\frac{C \cdot C_1}{C + C_1} + C_L}$$

$$z_1 = \frac{g_{m13}}{C} \rightarrow \text{cancelled using } R_2$$

So, the DC gain of this will be the gain of the first stage $g_m 1$ by $g_{ds} 1$ plus $g_{ds} 3$ times; that is very easy to see in the half circuit. We have $g_m 1$ loaded by $g_{ds} 1$ and $g_{ds} 3$ times $g_m 13$ divided by $g_{ds} 13$ and $g_{ds} 14$. I am assuming that there could be some load here which will be G_L and the unity gain frequency; of course, will be $g_m 1$ by C . The non dominant pole will be at $g_m 13 C$ by C plus C_1 , where C_1 is the parasitic capacitance here; that is the conductance due to $M 13$ being in feedback. I will neglect the other terms associated with that and then you have $C C_1$ is series plus any load capacitance that is connected ok.

So, we have a load conductance G_L and the load capacitance C_L . So, this is what we assumed. In addition to this we have an RHP right half plane zero, which is at $g_m 13$ by C and this can be cancelled using R_G ok; that is using a resistance in series with the integrating capacitance.

So, the two stage fully differential opamp is just a fully differential version; that is all we do the first stages already almost differential. It used the differential pair, but we do not use the current mirror load, we used the current source load and the second stage you have replicate it to the other side and we get the fully differential opamp. The gain and frequency response are very similar to that of the single ended case ok. So, in the next lecture we will look at how to do the common mode feedback stabilization for the fully differential two stage opamp.

Thank you.