Analog Integrated Circuit Design
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Lecture – 41
Common mode feedback circuits

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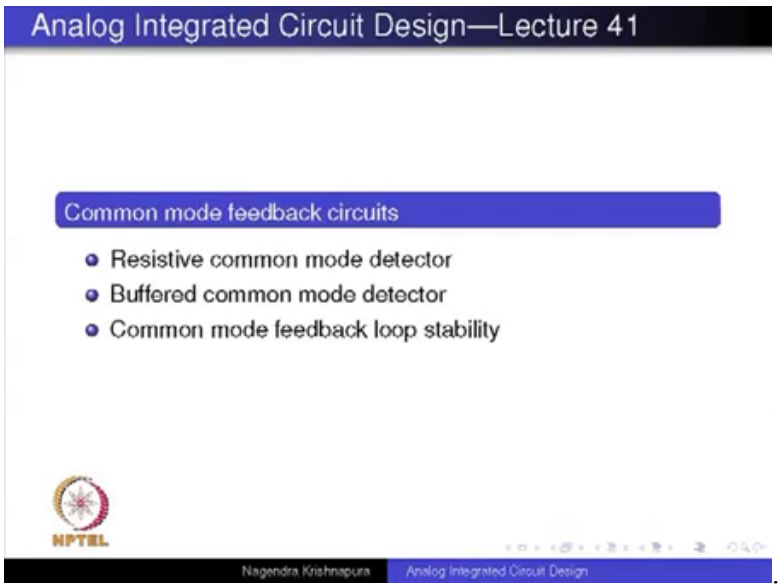

Hello, welcome to the lecture 41 of analog integrated circuit design. We have been discussing fully differential opamps. Fully differential circuits have a lot of advantages like immunity to noise and also that they cause less noise and interference to other circuits. So, that is why most of the circuits today are fully differential. Now, when you make a circuit fully differential, you need to have a common mode feedback loop to stabilize the output common mode voltage, ok?.

This is true of any circuit that you can think of and every circuit that we have discussed. So far can be turned into a fully differential version like the transconductor or the single stage opamp, two stage opamp, three stage opamp, anything that you take, ok? But each of these stages needs a common mode feedback circuit and sometimes like let us say two stage opamp, we need two common mode feedback circuits, one for each stage of the opamp.

So, we need to understand common mode feedback circuits very well. We will first do that with the single stage opamp because the single stage opamp circuits are simple. We can discuss a number of ways of a compilation common mode feedback in that circuit and then, we can translate that to any other circuit that we want to build, ok? Now, there is a great variety of common mode feedback circuits just like any other circuit, just like opamp topology there is a huge variety. We will not be discussing all of them, but we will discuss a few interesting cases and you can consult the literature and textbooks for a other possible common mode feedback circuit variants, ok?

But the basic principle behind all of them is the same. You will always have two current sources sort of fighting each other. One current source at the bottom and another at the top and this is necessary in order to have very high impedance, which is what gives you a very high gain, ok? But if you just leave it like that because of small mismatches in the current and the high impedance, the voltage will either go to somewhere near VDD or somewhere near ground and the transistors will no longer work in saturation region. We have to establish the common mode or the bias voltage at some desired value, somewhere in the between the supplier else. So, that the transistors are in saturation and that is why we have the common mode feedback circuit.

So, the job of the common mode feedback circuit is to adjust one of the current sources using negative feedback. So that it exactly matches the value of the other current sources. Now, when I say one of the current sources, we do not mean individual current sources, but the some of the current sources in the two differential arms of the circuit, ok? Now, another way to think of common mode feedback circuit is that it provides low impedance in the common mode. What is meant by common mode and differential mode? If you apply two signals either voltages or currents of equal magnitude and opposite sign, that is differential mode, if you apply to voltages or currents of equal magnitude and the same sign that is common mode.

Now, when you apply a common mode signal, it should appear like a low impedance circuit and when you apply a differential mode signal, it should appear like a high impedance circuit because for differential signals we need very high gain, ok?

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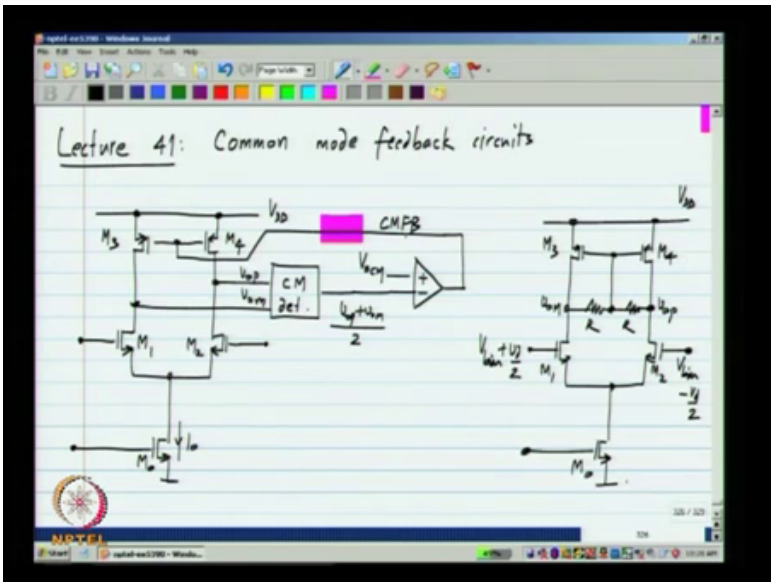

This is our single stage opamp and the voltage here at the gate of M3 and M4 controls the values of the current sources from the top and at the tail, I have assumed the fixed current source I naught.

Now, the common mode feedback can be used either said this voltage or this voltage. So that the tail current is adjusted in this particular case, I have assumed that the tail current is fixed and we are adjusting the value of the current from the top, ok? Now, a general representation of a common mode feedback circuit is like this. We have a common mode detector that is we have something that measures the common mode voltage compares it to desired common mode voltage VOCM and continuously increases or decreases the gate of M3 and M4 in a direction, such that the detected common mode voltage converges to the desired voltage VOCM, ok? It is a classic negative feedback circuit.

Now, in this particular circuit because increasing the gate voltage reduces the output common mode voltage VOP plus VOM by 2, the signs have to be of this for this particular opamp, ok? We also saw a very simple realization of this circuit where we did not have an explicit opamp for comparison. All we had was we made a common mode detector using a resistive divider of equal resistors, ok? Midpoint will be added VOP plus VOM by 2 they simply connected to the gates of M3 and M4.

Now, in this particular case the output common mode voltage will be stabilizing to the gate voltage of M3 and M4 at a drain current of I naught by 2, ok? When you apply a

differential voltage, what happens is that VOP will swing up. Let us say and VOM will swing down by an equal amount the average value does not change, ok? So, the common mode feedback circuit does not react to differential signals, that is a prerequisites of the common mode feedback circuit, it should not react to differential signals, ok? The same thing happens here, a VOP goes up, VOP VOM goes down by an equal amount this voltage does not change.

So, the currents delivered by M3 and M4 do not change at all. Now, the only problem with something like this resistive common mode detector is that, it will always load the opamp, or whatever stage we are detecting the common mode off.

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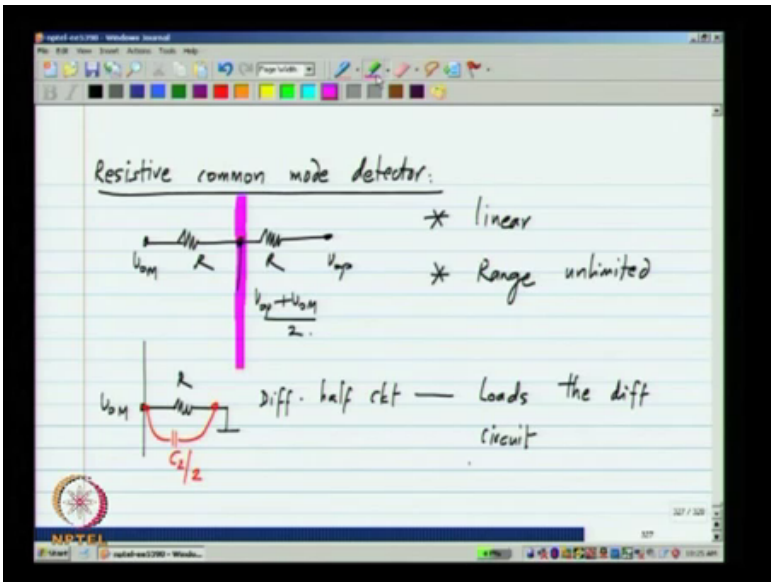

Now, the advantage of a resistive common mode detector like this is that, it is more or less ideal, we have VOP and VOM. Here, we get VOP plus VOM by 2 and first of all because we use resistors, it is linear even for large swings of VOP and VOM and also its range is not limited, ok? By itself VOP can swing to any value and VOM can swing to any value and the midpoint of this will still be VOP plus VOM by 2, ok? But the disadvantage is that in the differential picture, keep in mind this midpoint will be ground.

So, we will have this in the differential half circuit, ok? So, from the output to small signal ground they will be a resistance R, which will load the differential circuit, ok? So, while the resistive common mode detector is more or less ideal, it loads the differential circuit that is one disadvantage of it. For instance if you use it in a single stage opamp, it

will reduce the gain, ok? So, in order for it to not reduce the gain significantly, the value of R must be as high as possible.

Now, there may be practical problems in achieving this because if you want the high resistance, you need to have a very long and skinny resistance and that may take up a lot of area. So, that could be one practical problem, ok? And in any case, even if you make large resistance, you may not be able to make it much large, then the RDs of the transistors if you have a resistance R, that is smaller than the RDs of the transistors, the DC gain will be dependent on R and not on the RDs of the transistors, ok? In either case you will not be able to achieve the maximum gain that is possible in a single stage opamp.

So, a resistive common mode detective is usually not used with the single stage opamp, ok? So, that is one. Think now there is another issue, let us say, you go on making the resistance very large, what happens is there will be a parasitic capacitance from the midpoint. This is VOM, VOP. Here, I get VOP plus VOM by 2 at DC. Ok if you consider higher frequencies, let us say you go on increasing R, just because you do not want to load the circuit, what happens is that in the common mode half circuit, let me draw the common mode half circuit of this. For that I simply take this is the line of symmetry, I simply take this side and fold it back on that side.

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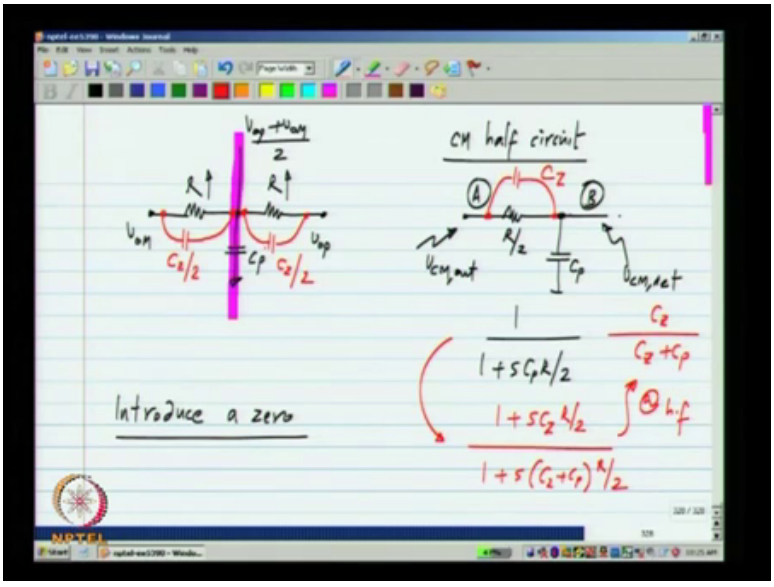

So, I have a resistance R by 2 and CP and this is the detected common mode, ok? So, here I have the common mode output and here, I have the detected common mode is clear, that for higher frequencies, the detected common mode is not the same as this because this is a low pass filter, ok? Now, this can also be a problem. Now, when we have this feedback loop, ok? If you have a pole in the common mode detective that adds to parasitic delay, ok? As we know any parasitic pole adds to delay in the feedback loop and that can make the circuit on stable. That can make this feedback loop on stable. You not looked at the details of this feedback loop gain, but will do that soon, but then, any case you know that a negative feedback system cannot have too many extra delays.

So, here the transfer function from this point to that point would be a first order loop as transfer function, ok? So, if R is very large; obviously, the delay is very large or the low or the bandwidth of this low passes filter is very small, ok? How do we fix this? We have earlier seen that by introducing a zero, we can essentially present an advance that is a negative delay and then, counter the effect of the delay. Now, how do we implement zero in this first? Order low pass filter that is very easy. All we have to do is to connect some capacitance like this. Let me just call that Cz in this particular case, the transfer function changes to from A to B, it will be ok. So, at high frequencies, it will simply be that of the capacitive divider, ok? It is easiest to think of this as the capacitor, Cz is the short circuit across R by 2 at very high frequencies.

So, all you have is this capacitive divider, you do not have the phase shift due to this RC circuit. You simply have an attenuation and the transfer function changes to Cz by Cz plus Cp, and Cz is comparable to Cp. This is some number, some fraction of one, ok? And that is quite acceptable as long as it does not give a phase shift. So, the many ways to think about this, you can think of the zero providing a phase lead or a negative delay, but in any case this can be used to stabilize the circuit.

So; that means, that in the actual circuit, remember this is only the common mode half circuit. So, in the actual circuit, you need to have half of the capacitor across each of the resistor in the common mode detector, ok? Now, this is fine, this can be done, but you see that this will also load the circuit, ok? So, now, in the differential half circuit, we will have this load as well. So, in addition to the integrating capacitor and the load capacitors of the single stage opamp, we also have the capacitance used in the common mode detector, ok?

So, that the passive common mode detector is very useful because it is linear, but it has some problems. First of all it loads the circuit that is the main problem ok? But the advantages that it is very linear. So, we will see that there are some situation where we will use this and in some cases where we will try not to use this one, ok? Now, what is the alternative? The one common thing whenever you are presented with a heavy load is to buffer it, ok? So, that is one of the obvious solutions.

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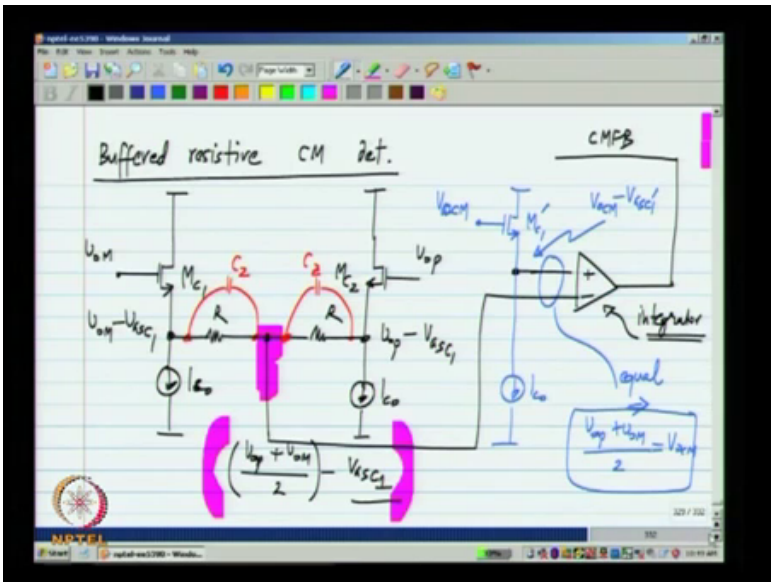

What is the buffer? We can use a source follower as a buffer. I will show it with an NMOS source follower, we could also use PMOS if the voltage ranges are compatible.

So, let us say this is VOP and VOM and we have two source followers MC1 and MC2. So, this will be some VOP minus sum fixed voltage, ok? VGS C 1 and this will be VOP minus VGS C 1, I will assume that for now there is no body effect in this transistors. So, the detector voltage here at the output will be VOP plus VOM by 2 minus VGS C 1, ok? So, it is related to the common mode voltage, but it also has a level shift, which is the same level shift of the source follower buffer, ok?

Now, our circuit looks something like this. We have to compare the detector common mode voltage to the desired common mode voltage and feed it back to current source transistors, ok? I will simply label this CMFB. A CMFB is nothing, but this node, ok? I am only concentrating on this part of the circuit here. Now, what happens is if the common mode feedback loop is stabilized, the detected voltage here and this VOCM will

be equal to each other. After all this opamp, here is measuring the error between the two and changing the common mode feedback voltage until this two become equal.

Now, this is a problem because VOP plus VOM by 2 does not equal VOCM, it will equal VOCM plus VGS C 1, ok? Now, this VGS C 1 is an unknown quantity, in that you can calculate it if you know the parameters of the transistor and the current exactly, but you do not know that, ok? So, you would in general like to avoid something like this, where you have process variations, ok?

Now, this kind of situation occurs very commonly in IC design as well you will have to deal with some quantities which in principle can be calculated, but because the parameters of the MOS transistors varies across process and temperature, these numbers also very quiet a lot. Now, a very common technique in IC design to counter this is to exploit matching, ok? It is very clear that instead of comparing the detected common mode voltage with VOCM, if I compared it with VOCM minus VGS C 1, I will get exactly what I wanted - VOP plus VOM by 2 will be equal to VOCM, ok? What I mean is, I should not do the comparison with VOCM, but VOCM minus VGS C 1, ok?

Now, how do I obtain this VGS C 1 in this expression? That is again very easy. I use a replica of this particular circuit, ok? I will write that here may be in a different color just to make that clear. So, let me call this MC1 prime and you use the same current, we call this IOC 0, these are also IC 0 and I connect it of there in the gate of this is connected to VOCM. Here, what we will get is VOCM minus VGS C 1 prime.

Now, this stage is a replica of these two stages source follower stages. So, VGS C 1 prime will be equal to VGS C 1. So, finally, when these two voltages become equal it implies that VOP plus VOM by 2 equals VOCM, ok? Now, this business of exploiting matching on integrated circuits is very - very common, ok? We have used it for simple circuits like current mirrors there are. So, many cases where you have two things to match, very well you have to match all the parameters, ok? In that case you simply use a replica circuit.

Now, that sounds weight. I have shown you one instant of it. So, whenever you have, let us say, voltage drops or some other parameters dependent on MOS transistor characteristics, you may be able to use a replica circuit. So, that, the dependence on MOS parameters which is also process dependent, will be cancelled out. So, this buffered

resistive common mode detector clearly does not load VOP and VOM, because looking into the gates of MC 1 and MC 2, we have high impedances ok, but the problem now is that initially when we had only resistors, the range was infinite, I mean practically you could have VOP and VOM of any values.

Now, if VOP and VOM become very small, they will drive this current source transistor into saturation. We can find out for yourself, what the limits are. ICO these current sources are also implemented using MOS transistors and similarly, if it becomes very large MC 1 and MC 2 will go out of saturation into tryout region, ok? Now, that is not very likely, because for an enhancement transistor with a positive threshold voltage VOP has to be above the supply voltage VDD for MC 2 to go into tryout region. So, that is not likely, but at least there is a lower limit. So, that is one problem, ok? So, we will end up with some swing limits.

Now, secondly, these transistors will have body effect, ok? If you use PMOS, you can avoid it, but as I have mentioned earlier, even with the PMOS tying the substrate to the source is not a very good idea, because it increases the parasitic capacitance at the sources greatly, ok? So, if you do a body effect, what happens is that this drop here is not a constant as I have represented, it is not just VGS C 1 on both sides if VOP is large and VOM is small, the VGS of MC 1 will be small and MC 2 will be larger, ok?

So, the level shift will depend on the absolute values of VOP and VOM. So, you will get some non - linearity in the detected common mode, ok? Now, this is a very common effect with any active circuit and with an active common mode deduction circuit the same problem will apply, but if you expect the swings here to be small, this kind of circuit can be used, ok? Now, what is the problem with a non - linearity in a common mode detector? The problem is that once the circuit becomes non-linear, it will not react only to the common mode VOP plus VOM by 2 in general, it will be some non-linear function of VOP and VOM, ok?

So, you will have some response to the differential component of the circuit as well and that is not good. It turns out that if you have some non - linearity in a common mode feedback circuit, that will be an even order non - linearity because of the symmetry of the circuit and even order non - linearity combine with some mismatch in the circuit can give you even order harmonics in the outputs of the circuit, ok? Now, this is a very general

description, for details you have to look at a specific circuits, but what you can expect from non - linearity in common mode feedback circuits and combined with mismatch in the differential part of the circuit is that, you will have even order distortion, ok? A fully differential circuit, it should have no even order distortion, but you can have it because of this reason.

Now, as before if R is very large, then there is a pole in the transfer function between the actual common mode VOP plus VOM by 2 and this point, where you do the comparison and you can reduce the effect of that pole by adding a zero using this capacitance, ok?

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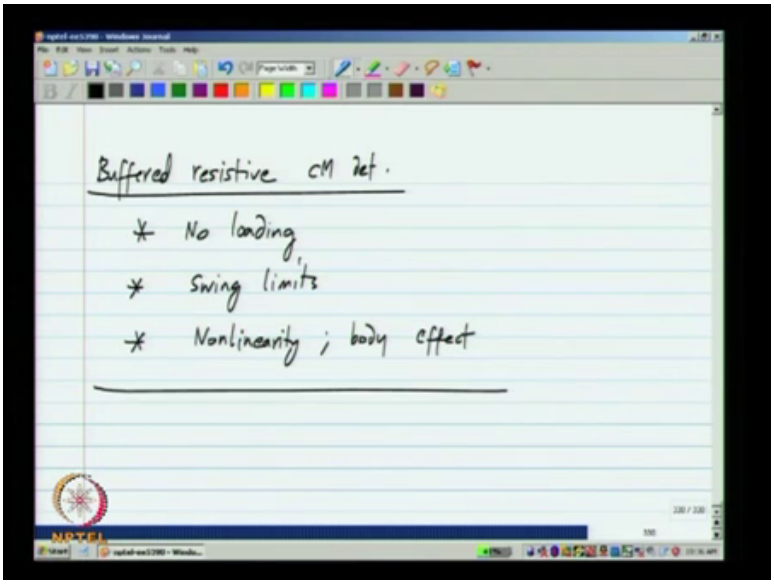

This is the summary of the buffered resistive common mode detector.

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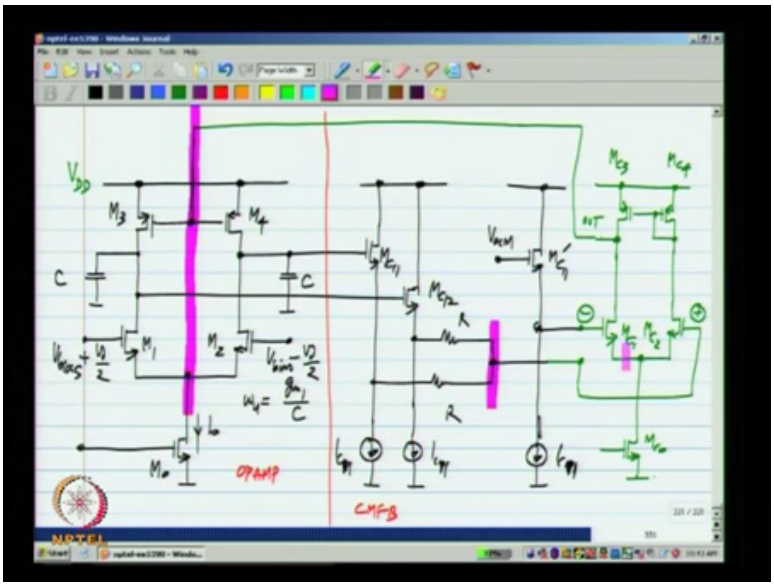

Let me just show you the full circuit of the single stage opamp, throughout slightly differently from before I will show these as current sources, but it is understood that you make them using MOS transistors, ok?

So, we compare this to and feed it back there, ok? We will see how to make this particular opamp shortly, ok? So, right now this is what the circuit is and we can also see that in the differential picture, this point will be a ground and this two will in the ideal case offered no loading in reality because of CGs of MC 1 and MC 2, there is some small loading on the single stage opamp, ok? I have not shown the integrating capacitors of the single stage opamp, whatever load capacitors you have here, will be the integrating capacitances and so, it is this part of it, that is the opamp and this is the common mode feedback, ok? And this implements a fully differential single stage opamp with a unity gain omega U equal to GM 1 by C and a DC gain, which is the GM of this transistor, divided by some of GDs of these two transistors, ok?

Now, we need to go ahead and implement that opamp. Now, we do not need really fancy opamp that so, we will start with simplest opamp, that we know that is the single stage opamp. Now, notice that this opamp has a differential input and a single ended output. So, the single stage opamp that we analyzed earlier with the single ended output is what we are going to use. Let me change the notation a little here, I will call this transistors MC 11 and MC 12. This is MC 11 prime, ok? This is all equal to MC 11.

So, the single ended single stage opamp looks like this. If this is the plus terminal and this is the minus terminal, that is the output and a common mode feedback is completed like that, ok? All this upper lines are VDD. First of all one remark about this circuit, this is just a single stage fully differential opamp with common mode feedback. Already you see that the circuit looks very complicated with many transistors, means probably at the limit of what I can draw in this area of the screen, ok? So, it is extremely important to understand what is beyond the circuits..

You cannot really mug of this circuits, you cannot learn them by heart and then, figure out how they work. You have to be able to understand each part of the circuit and then, understand the function of the circuit, ok? Also there is a huge variety of circuits. I can change from NMOS to PMOS. In most of the circuits, I can change the kind of common mode detective and so on. Ok?

So, the most important thing is to understand the principles beyond this common mode feedback circuit or in fact, any other circuit and ok? Now, we have this common mode feedback loop and like any other negative feedback loop, we have to make sure that it has a small enough delay and it is stable. Now, as well as the common mode feedback loop is concerned, we need to be concerned only with the common mode operation. So, I will use the common mode half circuit, that is normally, you would apply a differential input to this opamp, but I will now assume that we have applied only a common mode input and analyze the common mode part of it and we want to analyze the differential part, we can do it using the differential half circuit, ok?

Now, keep in mind that this is the line of symmetry, ok? And this is the line of the symmetry as well. So, these points will be at ground in the differential half circuit and in the common mode half circuit, I have to fold all of these circuits on top of each other in parallel, ok? For instance, this R comes on top of that R; these two transistors will be in parallel. These two current sources will be in parallel and so on.

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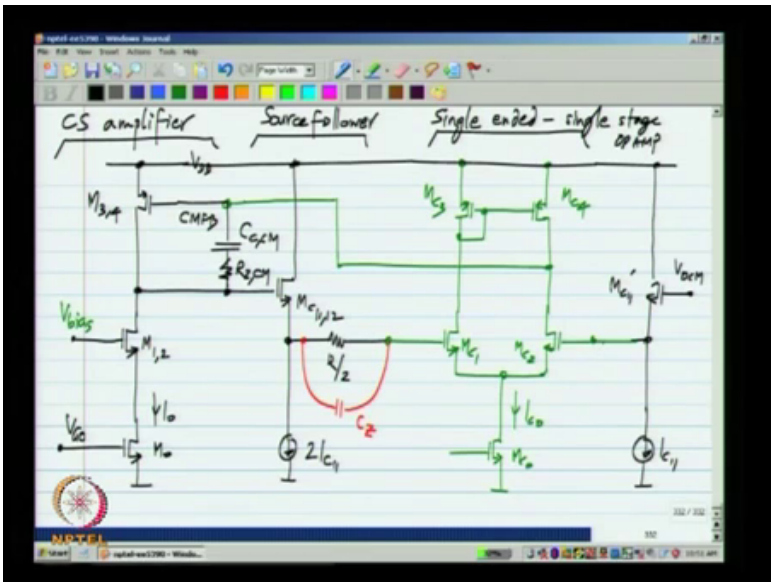

So, let me draw the common mode equivalent circuit. When I write M 1 comma 2, it means that M 1 and M 2 are in parallel and M 0 appears as it is with a current I 0, this is the common mode feedback node M 3 and 4 are in parallel there and here, I will have, MC eleven and twelve and parallel with a bias current of 2 IC 0 because I have a two current sources in parallel. I have the resistance R by 2, ok? And this part of the circuit will use the same color as before here, I have the replica could generate the correct half set of the source follower, ok? This common mode feedback circuit is completed from here, ok?

So, this part of it, which is really the differential opamp, simply looks like a current source in the common mode equivalent circuit, ok? So, this is at some V bias and this the bias for M 0 is derived from some current mirror. I will just call it VG 0, these two together for my cascade current source, ok? So, now, if you look at this circuit, we have a differential pair that is a single ended single stage opamp, ok? And the output of that goes to M 3, 4 and this output is from the drain.

So, basically M 3, 4 acts like a common source amplifier. This is a common source amplifier and the output of the common source amplifier goes to a source follower - MC 11 and 12, it has a series resistance R by 2, but let us now act as though it is not, there are assume that the frequencies are. So, low that no current flows through R by 2, because it is connected to the gate, we have a source follower, ok? So, we have a single ended

single stage opamp cascaded with a common source amplifier and a source follower in the feedback loop, ok? The feedback loop goes like this, right?

So, here we have it and then, the output of the single ended single stage opamp is like that and then, feedback loop gets completed that way, ok? So, that is the feedback loop. Now, what do we know about the stability of this? If you observe this circuit, we have is equivalent to a two stage opamp with an additional source follower buffer, a source follower buffer came because we use the buffer common mode feedback stage, if we did not use that even, that could not be there, ok? Because what we have in a two stage opamp is a single ended single stage opamp followed by a common source amplifier, ok?

So, the part that I have drawn in green plus the transistors M 3 comma 4 will act like a two stage opamp and it happens to have an additional source follower buffer MC 11 and 12, ok? In the common mode equivalent circuit, whatever we discussed earlier for the stability of the two stage opamp will apply here as well, ok? Now, we know that in order to have stability in the two stage opamp, we needed to have a miller or integrating capacitor from the gate of the common source amplifier to its drain, ok? So, this is what was called cc and because it is here for the common mode feedback loop I will call it CC cm, ok? This is what makes this GM and this C behaves like an integrator, remember what we what we need here is an integrator.

Now, what we have implemented is not an integrator by itself, but I transconductor and its transconductor in combination with this CC cm behaves like an integrator, ok? Now, another way to think about it is that, there are too many stages in feedback loop. So, there is a lot of parasitic delay. So, one of them has to dominate right one of the delays has to dominate, that is what we call by dominant pole compensation. So, the feedback has to be close around a single stage and that can be done by using this capacitor, ok?

So, anyway you think about it essentially, you will have a single stage and feedback, ok? And also as I mentioned earlier if this R by 2 is very large then, these R by 2 in combination with the CGS of MC 1 will cause a lot of delay in the loop. So, you may also have to connect a capacitor. So, there it creates a zero in the loop, ok? So, this is what we need in order to have a stable common mode feedback loop.

Now, you see that the circuit looks exactly like the two stage amplifier, where the CC cm is the integrating or the miller compensation capacitor, ok? And just like with the two

stage opamp, you can also add a zero cancelling resistor in series with this, ok? Now please do not get this confused with the opamp that we are trying to realize, we are trying to make a fully differential single stage opamp. Now, the common mode feedback loop for that opamp looks like the single ended two stage opamp, ok?

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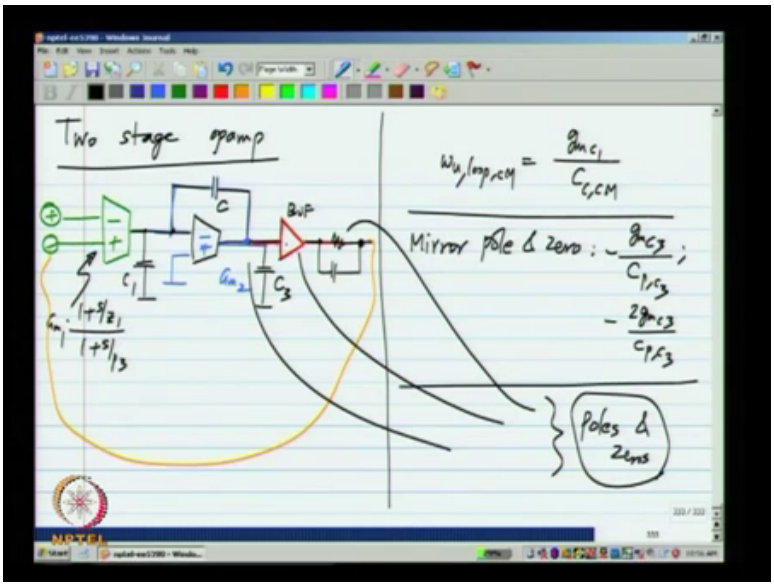

Now, because we have already analyzed the single ended two stage opamp to a great detail, we do not have to reanalyze that here we just have to associate the terms here with what we used over there, ok? That is recall, let the two stage opamp add a topology like this, when addition to that we have a buffer, ok? We also have parasitic capacitances here and there, ok? Let me just call it C 3 and this is C. Now, this Gm 1, we know is not a memory less Gm 1, but it has a pole under zero, ok? We these are the results that we have already derived for the two stage opamp. You can go back to those lectures and revise that if you wish to.

Now, this part corresponds to whatever I have drawn in green in the previous picture. So, that is the single ended single stage opamp and this Gm 2 in the second stage corresponds to this M 3, 4 and this integrating capacitor, possibly with something that cancels the right half plane zero and finally, this buffer is made using that in addition to all of this, we also have this in the loop, ok? So, you see that the loop is completed around this entire thing. This loop is an unity feedback, ok?

So, what we need to know is which components are associated with which part of this and if you wish to you can put down the values of Gms and calculate where the poles and zeros are and as certain if the circuit is stable, ok? Now, the unity gain frequency of this feedback loop, which is also the unity loop gain frequency because we have unity feedback around this, will be Gm 1 corresponding to this divided by C, ok? Now, translating the terms, it will be the Gm of these transistors, gm c 1 divided by this capacitor here, the integrating capacitor CC cm, ok? The unity loop gain frequency of the common mode feedback loop is gm c 1 divided by CC cm, ok?

Now, there are a number of poles and zeros. So, we will have the mirror pole and zero, due to the first stage it will be at gm c 3 divided by some parasitic capacitance associated with that. That is where the pole is and the zero will be at twice that value, ok? All these results you can recall from earlier analysis of the single stage opamp in addition to that we have the second pole, due to this, gm 2 and the load capacitance, ok? Very rudely it is gm 2 by C 3 plus C1, but we know it is not the case. gm 2 will be divided by some factor and so on.

So, you can work out the calculation and there also basically, poles at associated with this node and poles in the buffer and also due to this resistive element here, ok? So, there will be a number of poles and zeros. We have to make sure that the phase lag due to all of this poles and zeros at the unity loop gain frequency is, let us say less than some value, so, thirty degrees also. So that you could have a healthy phase margin, ok? When practice what you do is not to sit and calculate all of this analytically.

You need to know which of the components contributes to poles and zero, so that you can manipulate the values. If you need to, if you, if necessary you can change the poles, that is move the poles to higher frequencies and so on, but generally once the circuit becomes, so, complicated! These hand calculations will not be efficient. So, we will go to the simulator in one of the later lectures. I will show in detail - how to design an opamp using the stimulator and how to measure the loop gain and so on. So, that you can have a sufficient phase margin, you can design the feedback loop to have a sufficient phase margin and limited ringing in the step response, ok?

So, for this where will do is put the circuit in a simulator and there are ways to measure the small signal loop gain and are also ways to measure the step response, you will do

that and make sure that the stability is guaranteed, ok? When you carry out such an exercise and find out that the phase margin is not sufficient or there is a lot of ringing, you will need to know which components to change.

Now, the analysis that we have done earlier is useful for that, ok? So, you should know which components are contributing to the poles and zeros. So, that you can change that part of the circuit and improve the phase margin, ok?

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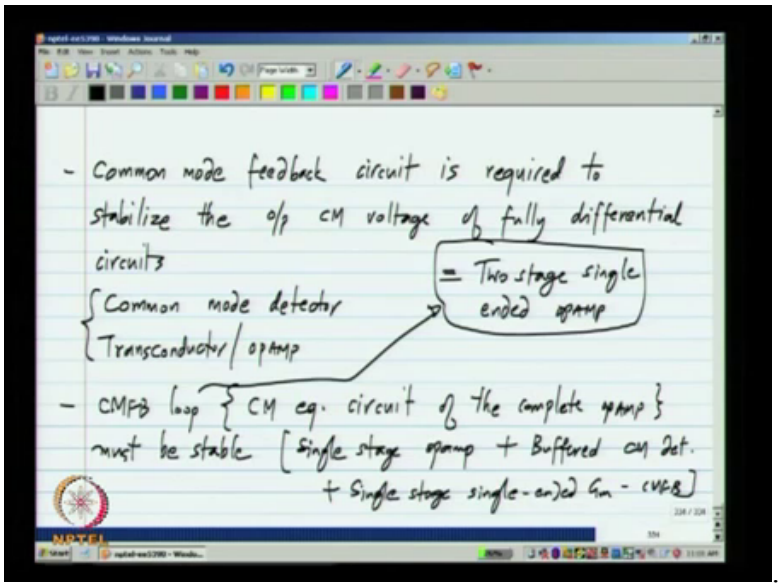

When summary a common mode feedback circuit is required stabilize the output common mode voltage of fully differential circuits, ok? Common mode feedback circuit consists of a common mode detector plus some transconductor or opamp to complete the feedback, ok? Sometimes this transconductor to compare the detected common mode to the desired common mode is not explicit, but it is implicit within some part of the circuit ok?

Now, the common mode feedback loop which basically is the common mode equivalent circuit of the complete opamp must be stable of course, like any other feedback loop and hereby, stability we mean not only not oscillating that is not nearly having poles in the left half plane, but also limited amount of ringing and overshoot. So, the common mode equivalent circuit can be anything.

Now, further particular case that we considered and this is a fairly typical case single stage opamp plus a buffered cm detector plus a single stage transconductor single stage - single ended transconductor for CMFB, ok? Now, in this case a common mode feedback loop itself looks like a two stage single ended opamp, ok? And you have to analyze this usually with the simulator and ensure that it is stable, ok?

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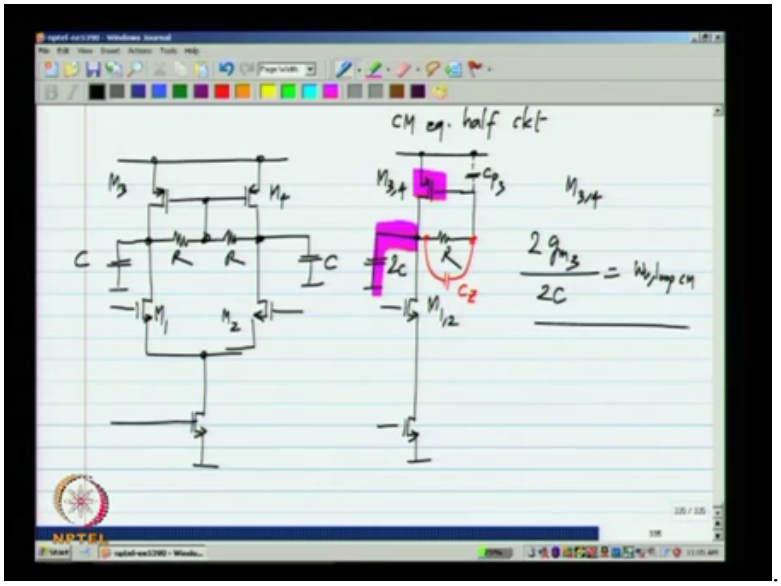

Now, if we go back to the very simple common mode feedback, we had earlier all way had was this R connected there, there will be invariable. Be some parasitic capacitance at this node due to this transistors as well as may be due to the resistors, ok? A common mode equivalent circuit of this is, ok? So, there may be some parasitic capacitance. Here, I will call at CP 3 and then, to make this into an opamp, we will have the integrating capacitors C, ok? We will have that.

Now, in this feedback loop, which is basically that one, the combination of M 3 comma 4 and this capacitors, sorry this should be 2 C in the common mode half circuit common mode equivalent circuit. So, this transistor and these capacitors behave like an integrator and this resistance in combination with CP 3 will be a parasitic delay, which can be reduced by adding a capacitor CZ, ok? Now, because we have one integrator and a single parasitic pole, it is quite easy to stabilize this one, ok? Compare to the other case where we had a two stage opamp. Now, the common mode feedback loop in this particular case

is equivalent to a single stage opamp and the common mode feedback loop, when we have a more elaborate common mode detector is like a two stage opamp, ok?

Now, this is a fairly typical case and you need to be able to work with this, but because we have analyzed the two stage opamp in great detail, you should be able to work it out. I am not going to write the expressions for poles and zeros here, I am assuming that you can associate these components with the components in the two stage opamp. Similarly, here the integrator is the gm of M 3, 4 that is, two times gm 3 divided by 2C that will be the unity gain frequency of the integrator in the common mode feedback loop..

In any feedback loop, you will have some integrator like behavior you will also have parasitic poles and zeros in the circuit. You just need to make sure that the effect of all those things is such that the phase margin is sufficient that is there is not a significant phase lag at the unity loop gain frequency, ok? This is the unity loop gain frequency of the common mode feedback circuit. See you in the next class.

Thank you.

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