Analog Integrated Circuit Design
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Lecture - 40
Fully differential circuits

Hello everyone and welcome to lecture 40 of analog integrated circuit design in the previous lecture we look at the advantages of fully differential circuits that is where every signal is carried on 2 wires and the 2 wires carry equal and opposite voltages with respect to ground. The main advantage is immediately to interference as well as that they cause less interference they are immune to both stray interference from other wires that may be passing and also interference due to voltage drops on power supply and ground lines ok.

So, we would like to make all the circuits that we already made fully differential that is the opamp and the transconductor and so on and that we look at in this class. Now in the previous class we also saw how to analyze fully differential circuits we can do that using common mode and differential mode half circuits, now as for as noise is concerned if you take a single noise source the circuit is not symmetric, but we can represent that as a combination of a common mode and differential noise voltages.

The common mode noise has no effect and the differential noise will have some effects and finally, we found out that we have calculate the output noise of a fully differential circuit we can take the corresponding half circuit do it is noise analysis as though that for the entire circuit and double the voltage noise spectral density.

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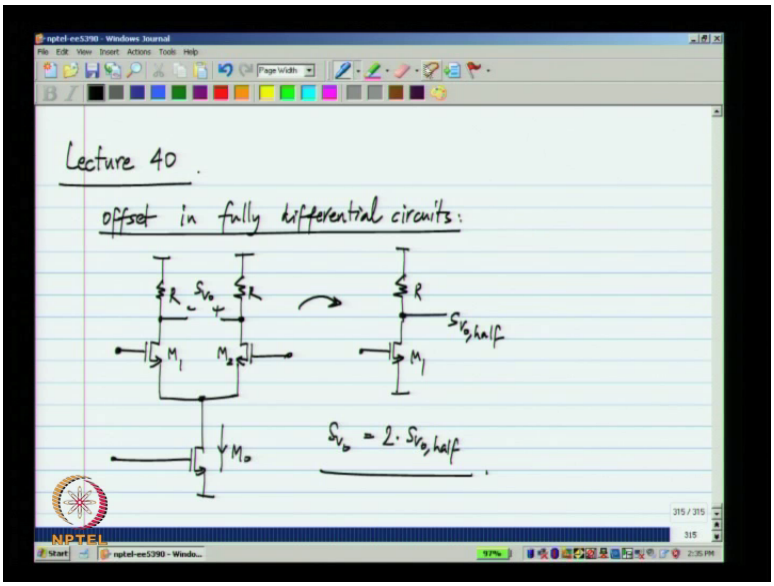

Now we will quickly look at how to calculate offset in a fully differential circuits then move on to design fully differential opamps [noise]. Now we saw that if we have a fully differential circuit such as the differential pair loaded by the resisters the differential noise voltage between these 2 notes will have some spectral density S vo. Now we take the half circuit and calculate it is output noise voltage spectral density let me call it S vo half S vo will be 2 times S vo half.

Now as I emphasized the noise current this register courses a certain output voltage here and there and similarly this register will cause some voltage here and there and so on, but the net result is that you take the half circuits do it is own noise analysis and double the spectral density to get the output noise spectral density in a fully differential circuits.

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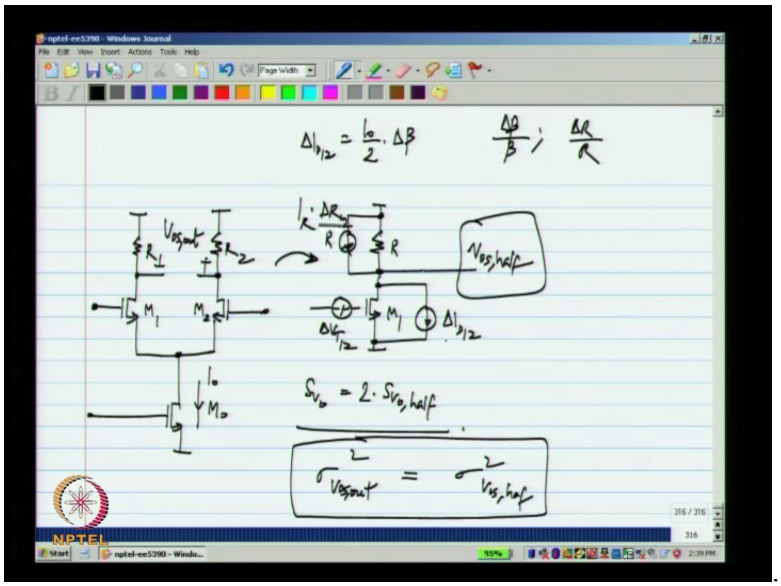

Similarly as far as the offset is concerned let us consider the offset here the offset in presence of mismatches will be some dc voltage V os and here I am calculating it for the output it can be referred to the input by dividing by the gain. So, that is the output offsets now can we calculated that from the single ended equivalent circuit it turns that we can first of all we simply insert the mismatch between transistors 1 and 2 that is the transistor corresponding to this single transistor in series with the gate of amount.

If you have some current mismatch that can be inserted here, here delta id 1 2 is the absolute mismatch in the absolute current and that is equal to I naught by 2 times delta beta delta beta is the mismatch in current factor between these 2 there is no threshold voltage mismatch. The current mismatch in the between 2 transistors would be simply the quiz and current times were change in data value. Similarly the effect of any mismatch in the register can be also represented by an equivalent current source or a voltage source.

So, the mismatch current will be equal to the quiz and current flowing in the register which is in this case I naught by 2 let me assume this current is I naught times the mismatch in the resistance. Now what we will be given will be delta beta by beta and delta R by R and so on for beta and R and so on it is specify the relative mismatch from that we can calculate delta beta and delta R and multiply that by I naught by 2 here and there to get the equivalent current sources.

Now how can it be represented by an equivalent current this comes from a simple application of substitution theorem or what is known as composition theorem I will not go into the details [vocalized-noise], but the mismatch in every component can be their represented like this. So, finally, because all this voltages the small signal output voltage will be of some value let me call that V os, half. It turns out that the variance of the output offset in the differential circuit exactly equals the variance of this output voltage we get in the half circuit.

Now in case of noise we get a factor of 2 and in case of offset we do not get that because this offset already represents the relative mismatch between 2 identical devices it is assume that this is delta V T 1 2 represents the mismatch between M 1 and M 2 similarly delta id 1 2 represents the mismatch between current factors of M 1 and M 2. Similarly, this delta R it is not just the error in the value R compared to the nominal value, but the mismatch between if liable these R 1 and R 2 R 1 2.

So, because of this we do not get the factor of half and this is the way the mismatch normally specified as the process people measure a large number of pairs of identical devices and characterize the mismatch between them. So, what you have in the process data sheets is the mismatch between 2 nominally identical devices.

So, again by simply doing the half circuit analysis you can find out the offset voltage we consider the design of opamp in some detail the opamp had differential input and a single ended output, we needed at the differential input to take the error between the desired and feedback signals, but the output goes single ended with respect to some ground. Now what we would like to is to move on to fully differential opamps because we have already seen the advantages of fully differential signals.

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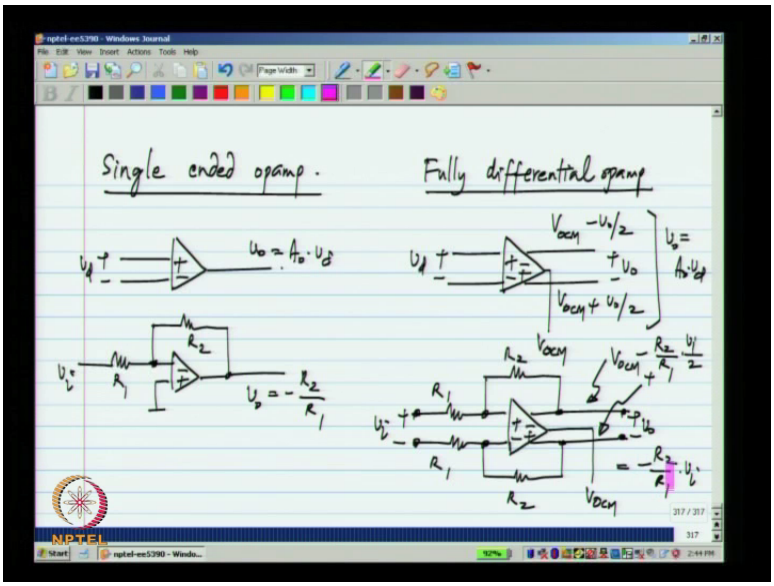

This is the single ended opamp this is the input voltage and that is the output voltage and in the small signal regime it is some dc gain times V d if V d is a dc. Now what is the fully differential opamp the input is differential and the output is also differential the differential voltage let me call it V o and each of the individual voltages with respect to the ground would be some V cm plus let me call it V ocm to denote it is output common mode voltage plus V o by 2 sorry this is the negative output [noise]. So, it is minus V o by 2 and this is V ocm plus V o by 2 and what is V ocm it is the common mode of the output it is usually some constant dc quantity and that will be an input to the opamp I will show it like this.

So, you can specify the output common mode voltage of the opamp by providing a corresponding voltage to the opamp and these voltages will be internal to the opamp, we will see how this will used and we design this circuit at the transistor level. Now how do we use this opamp for example, we make an inverting amplifier like this 1 V os minus R 2 by R 1. Now the fully differential version of this circuit would be the input is the differential voltage here and the output differential voltage will be minus R 2 by R 1 times where and I did not mentioned this earlier V naught in this will be A naught times V d, if V d is the dc otherwise it will be a of s where a of s is some transfer function the transfer function of a opamp [noise].

So this is the fully differential version again you can easily analyze that by assuming that the inputs the opamp or a virtual short if the opamp behaves like an integrator or if it as a very high gain then these 2 inputs will be at the same voltage and the output will be minus R 2 by R 1 times V i and if you look at the individual voltages let me assume that the output comma more voltages set to some voltages V ocm this will be V ocm minus R 2 by R 1 V i by 2 and these other side will be the same thing except with the plus sign. So, the output will be fully differential.

So, this is how make fully differential circuits and also please note that once you have a fully differential circuits this minus sign loses it is significance if I measure the output voltage with the upper terminal being positive and the lower being negative I get minus R 2 by R 1 times V i. If I flip the notation of V naught I will get plus R 2 by R 1 times V i [noise]. So, simply by a flipping the wires I can get either positive or negative gains.

So, that is actually a simplification in the realization of differential circuits there are many occasion where when you make a single ended circuit you need to realize gains of minus one simply to invert the polarity of the signal whereas, in a differential case you can invert the polarity of the signal by simply crossing the wires. Now how do we come up with fully differential circuits for any circuit with opamps which as one of the input terminals of the opamp be ground it is very easy.

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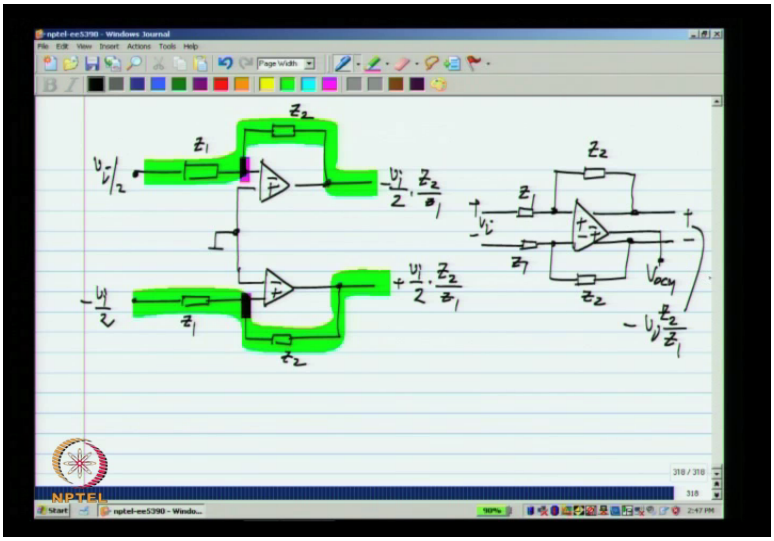

Let me just show the inverting amplifier example again.

But I will show impedances just to make it look more general. So, we have this now let me copy over and draw the same thing upside down z 1 z 2. Now, these are 2 single ended circuits if I have V i by 2 I get V i by 2 z 2 by z 1 the negative of that and if I have minus V i by 2 I get this voltage at the output and these 2 voltages are connected to ground.

Now you see that there is virtual shot between these 2 terminals and these 2 [noise]. So, effectively the voltage and that point are the same if the opamp are ideal. So, what we do the fully differential opamp is to essentially lift these of the ground that is ignore this part and have only these parts of the circuit. The total input voltage will be the total difference voltage here V i and the total output voltage will be V i times z 2 by z 1.

And I will not always show this explicitly, but the output common mode voltage is set to some V ocm this means that the 2 output voltages will be V ocm plus V i times z 2 by z 1 by 2 and V ocm minus V i times z 2 by z 1 divided by 2 [noise]. So, this is quite easy to do for any circuit in which the opamp has one terminal to ground if the opamp does not have either terminal at ground you cannot do this, but usually we can make all the circuits that we want with circuits of this type. So, we would not worry too much about that.

Now how did we make a single ended opamp with a certain unity gain frequency omega u.

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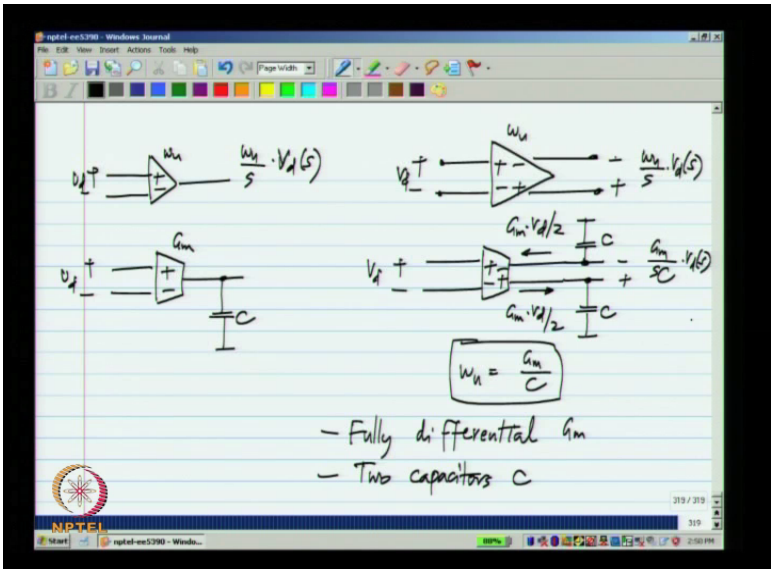

We used a transconductance or a voltage controlled current source G M and passed it is output current through a capacitor C. Now when we want to make a fully differential opamp the principle is the same let us say the unity gain frequency is omega u then the total output voltage will be omega u by S V d of S that is what we would like ideally the opamp is an integrator.

What we need in this case is a fully differential trans conductor and what is the meaning of that if I apply a voltage V d there is a terminal at which it draws a current G M times V d and there is a terminal wire it pushes out the current G M times V d V d by 2 and you pass each of these currents through capacitors C then the output voltage will be G M by a C times V d of S and of course, the unity gain frequency of those opamp is G M by C [noise]. So, first of all we need a fully differential transconductance G M and we need 2 capacitors and this is always the case the physical structure the schematic of a fully differential circuit will be symmetrical it has to be we need 2 integrating capacitors C how do you realize the differential G m.

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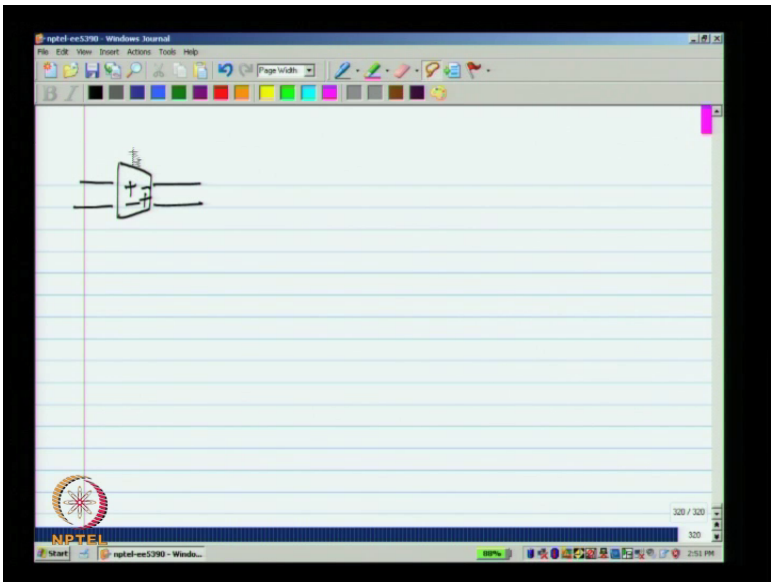

It turns out we can do it in a very similar way that we realized the single ended transconductance.

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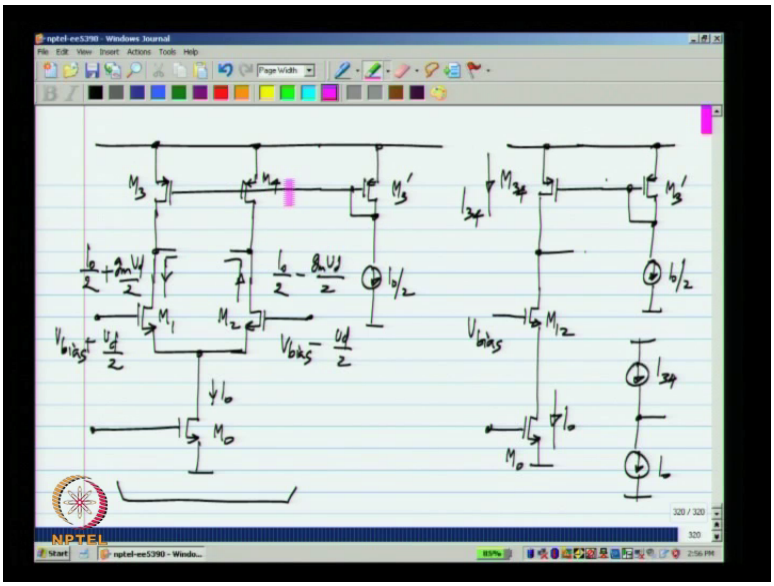

If you take a differential pair and apply a differential voltage to it what we get are incremental current which are equal and opposite. So, here we get total current of I naught by 2 plus g m V d by 2 and here it is I naught by 2 minus gm V d by 2. Now this is exactly of the form that we required here except that there is also the bias current I naught by 2 [noise]. So, if we subtract of the bias currents I naught by 2 from these 2 arms what we will be drawn from here and what will be pushed in out of that note will be G M V d by 2.

So, this is exactly circuit that we require we need a differential pair and we need current sources I naught by 2 [noise]. So, what is the difficulty now we can try to implement this directly [noise], but [noise]. So, let us say I take 2 pmos transistors and bias them with a current mirror let me assume this transistor are all identical M 3 prime M 3 and M 4 and bias them with I naught by 2 what will happen, it is a very easy to see when I make the common mode half circuit of this that I take the this half of the circuit and fold it over the other half [noise].

Let me assume that is there is no signal at this point now clearly you see that this is like having 2 current sources that are connected together nominally this current source equals I naught that is the current in M 3 and current in M 4 put together [vocalized-noise], but in general it will be something else I will call at I 3 4 and if I 3 4 is different from I naught either this voltage will keep on rising until M 3 4 goes in to triode region or it will

keep on falling until M 1 2 and M 0 going to triode region [noise]. So, this you recall it looks like having 2 current source I 3 4 and I naught like this. We know that with ideal current sources we cannot even make this connection unless I 3 4 happens to be exactly equal to I naught there is no way to guarantee that the total current from the upper transistors M 3 and M 4 equals the current from the lower transistor M naught ok.

So, if you do build the circuit you will almost certainly find output to be very close to the V dd rail where the pmos transistors are in try out region or very close to ground rail where the nmos transistor are in triode region. So, we cannot do this and we also know from biasing circuits that is where we bias the transistors that a given bias current I naught that we will never be able to set the 2 currents sources independently and have their values to be equal to each other.

Now the only way to do it is by setting one of them using negative feedback for instance we can adjust the gate voltages of M 3 and M 4 such that the their total current output equals the current of M naught and we have to do this with negative feedback ok. So, let us see how to that so, well I can said what happens is if the total current in M 3 and M 4 is larger than current from M 0 these voltages will keep on rising. Now if the total current is smaller this voltage will keep on falling what I want is for the sum of a these 2 voltages to be sum constant such that the all the transistors M 1, M 2, M 3, M 4 are in such saturation region.

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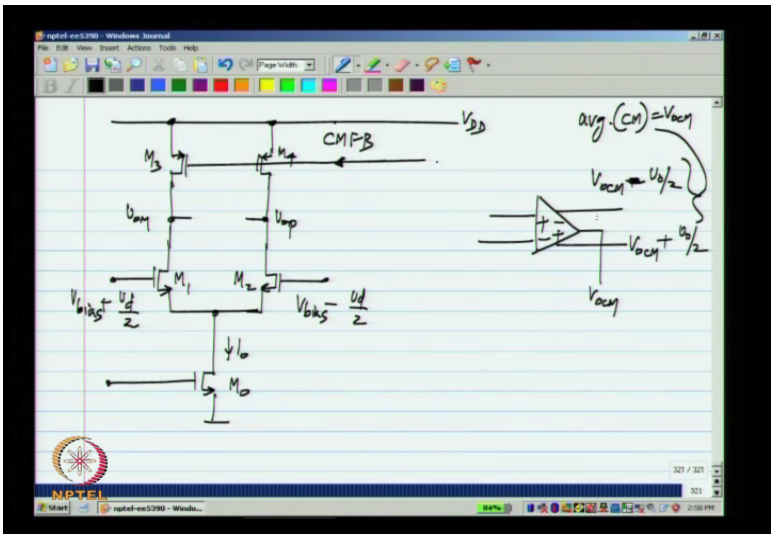

So, let me call this V op and V om we cannot using this kind of biasing this has to come from feedback which is usually call the common mode feedback or CMFB. Now what should this feedback be based on we should based on the average value of V op and V om, we do not want to react to V op and V om individually like that said we need an opamp and opamp output must be able to vary which not that the opamp output voltage must be fixed then the opamp is completely useless.

What we want is that, the average of the 2 output voltages V equal to constant V ocm these 2 voltages have an average of a common mode value equals V ocm [noise]. So, what should I do in negative feedback as usual I have to compares the actual value with desired value and adjust the actual value until it becomes equal to the desired value. Now here what is the actual value that is the output common mode voltage of the opamp?

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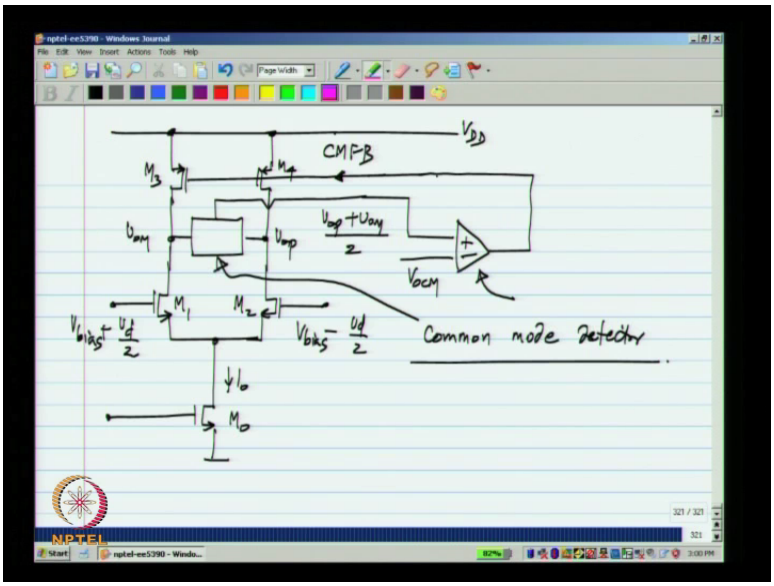

I need detect the output common mode voltage let me call this the common mode detector. So, it is output voltage will be nothing, but V op plus V om divided by 2 then I have to compare it with the desired output common mode voltage V ocm and feed it back to the gates of M 3 and M 4 in the right direction, in the right direction means that if the output common mode is too high what should happen is that what; that means, is that the current in M 3 and M 4 are low lower than the current from M 0.

So, then the current in M 3 and M 4 must decrease similarly if the output common mode voltages are very high; that means, that the current in M 3 and M 4 is more than the

current from M 0. So, the current in M 3 and M 4 must decrease ok. So, when the current in M 3 and M 4 decreases M vom and V op will be pull down similarly when this output voltage is too low the current in M 3 and M 4 must increase so, that the output voltages increase so, you will see that to decrease.

The value of currents in M 3 and M 4 we need to increase the output voltages. So, if the voltage is very high the common mode feedback voltage must be increased if uh the output common mode very low the common mode feedback voltage must also be decreased [noise]. So, the polarity of the opamp used in the common mode feedback is given by this, we can also determine science by breaking the loop and making sure that what comes back negative and so on whatever I described is just that what in different words.

So, this is the general common mode feedback circuit we need to have a common mode detective [noise]. So, that you detect the actual output common mode voltage you compare it with the desired common mode voltage V ocm and you control one of the current sources with that in fully differential circuit you will always have scenarios. So, where we have some current source coming from the top and something coming from the bottom and the 2 have to be made exactly equal the way to do that is to control one of them using negative feedback.

Now we will see how to implement this negative feedback there is wide variety of common mode detectors as well as ways to close the feedback loop first of all let us consider common mode detectors.

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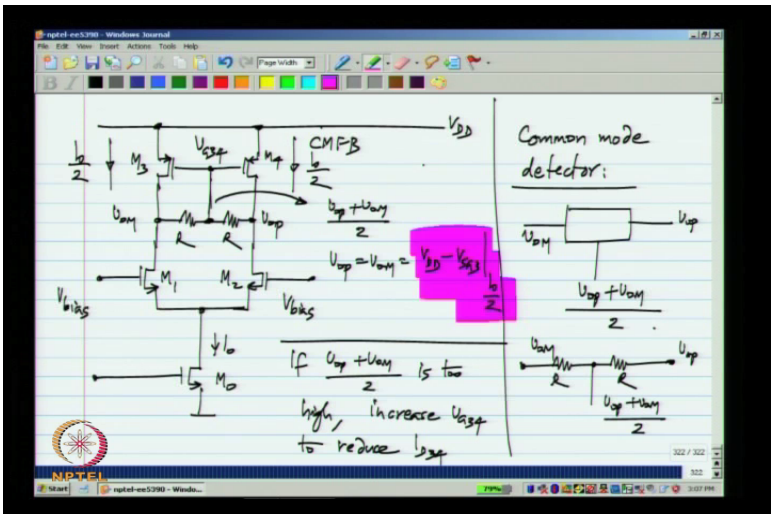

We want to take in V om and Vop and obtain an output V op plus V om divided by 2, how can we do this, the simplest way of getting the average of 2 voltages is to use a resistive divider V op and Vom. So, will get V op plus Vom by 2 if this 2 registers are equal [noise]. So, that is potential candidates for the common mode detector. So, let us use that here we will see what the implication of this is later.

Let me label these gate voltages Vg 3 4 and next thing is how to close the feedback loop, as I said the director common mode voltage V op plus V om by 2 is too high; that means, that the current M M 3 and M 4 is too high and we have to go on increasing the value of V G 3 4. So, that the current in M 3 and M 4 goes on reducing and the output common voltage reaches the desired value, similarly if the detector common mode voltage is too low you have to continuously reduce the value of V G 3 4 [vocalized-noise].

So, that the currents in M 3 and M 4 will increase and the output common mode voltages reaches the desired value and vice versa. Now there are many ways of completing the loop we can use an integrator or an opamp between this point and that point. So, that we get the feedback action that I just described, but the most simple realization of this is to observe that if V op plus V om by 2 is too high V G 3 4 also must increase that is it must go in the same direction as V op plus V om by 2.

Similarly the incremental gain required from this point to that point is positive [noise]. So, as you can see here if this voltages detector common mode is too high the common mode feedback also must be high, similarly if this is too low the common mode feedback

also must be low. In the simplest way to arrange that is to connect the 2 together now if you recall how you derived the diode connector transistor where the transistor biased at a constant current we detect that current difference of the drain and fed it back to the gate where many ways of feeding it back, but the simplest realization was to tie the gate to the drain.

Now this is similar, but in this case it is not a single transistor we detect the common mode voltage of 2 transistor and connected directly to the gates of the 2 transistors. Now you can analyze what happens first of all let us assume that there is no differential input that these 2 voltage have to be equal to each other vice symmetric [noise]. So, no current flows through R and this voltage equals the output voltage plus V om by 2.

Now when the feedback circuit is settled the current in this has to be I naught by 2 and the current in this is also I naught by 2 and also the gate voltages of these equals their voltages of drains of M 3 and M 4 ok. So, the output voltages will be equal to V DD minus V SG of M 3 or V SG M 4 at a current of I naught by 2 it has to be equal to this is if this voltages higher than that means, that the current here is too low and the voltages V op and V om will pull down if this voltage is lower than what I mention here then current in M 3 and M 4 is higher than I naught by 2 and this voltage will be pulled up [noise].

So, in this case the output common mode voltage we will get stabilized to this particular value, now in this the is nothing, but the output common mode voltage V ocm in this particular circuit we dint provide a V ocm from outside it is built into the constants of the mos transistor [noise]. So, once you have the threshold voltage [noise] and the current factor and the current values you can calculate the output common mode voltage.

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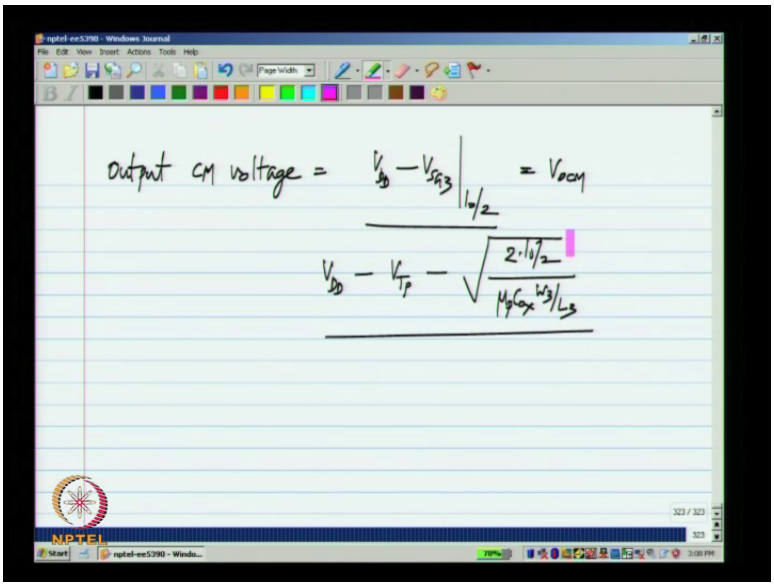

This is V ocm now we do not have freedom in setting the Vocm arbitrarily it depends on the threshold voltage and the parameters of the mosfet because V SG 3 is nothing, but the threshold voltages of the pmos transistors minus square root of 2 times I naught by 2 divided by mu p C ox of W 3 by L 3, now by choosing that dimensions of the transistor you can play around a little bit with the output common mode voltage, but you have too much freedom to do so.

But in many cases this circuit works perfectly well, now what happens if you apply a differential input let us I have plus V d by 2 and minus V d by 2 here what happens in that case is that there will be an incremental voltage V op and an equivalent opposite incremental voltage in V om. Now because the voltage at this node is the average the 2 voltages and the increments are equal and opposite the voltage V G 3 4 does not change at all ok.

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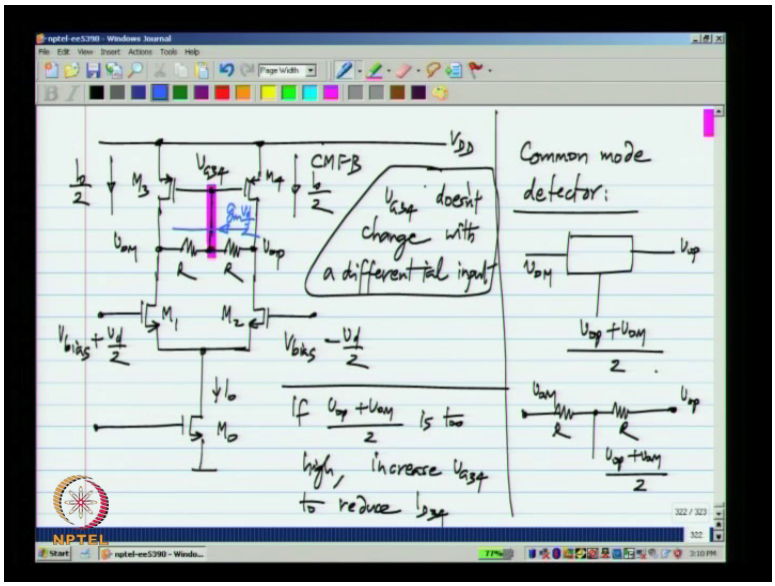

V G3 4 does not change if you have a fully differential input. So, what it mean the that M 3 and M 4 will continued is apply the same current as before and the differential current the extra current that is drawn from M 1 and the extra negative current that is drawn from M 2 will flow through R [noise]. So, there will be a current G m Vd by 2 in that direction ok.

So, the upper transistor M 3 and M 4 behave like constant current sources and because of negative feedback their sum is adjusted to be exactly equal to the value of the rail current source I naught and we need the negative feedback because there will be no other way to adjust their values to be exactly equal to the rail current source [noise]. So, a fully differential opamp needs common mode feedback and another way to think about it is that we really have 2 output voltages in a fully differential opamp the positive and the negative output voltage and we need to feedback loop to fix the individual voltages.

Now as usual it is better to think of differential and common mode voltages instead of individual voltages because what we desire is that differential voltage and what we want to suppress or we want to volt constant is the common mode voltage. So, this kind of an opamp any which why you think about it needs to independent feedback loops now we do not think of it as a 2 independent feedback loops controlling each output voltage we think of it is one feedback loop controlling the differential output voltage this is the feedback loop that controls the functionality [noise].

So, if you look at this particular circuit in the single ended case the feedback loop form by the impedance is z 1 and z 2 control the output voltage similarly here the feedback loop found by z 1 and z 2 control the differential output voltage. Now we need another feedback loop and that feedback loop operates only on the common mode output and it helps at the common mode output voltage. Now what is the effect of the common mode feedback on the differential circuit we added some components here and we have to investigate, what it is effect is let me redraw the circuit.

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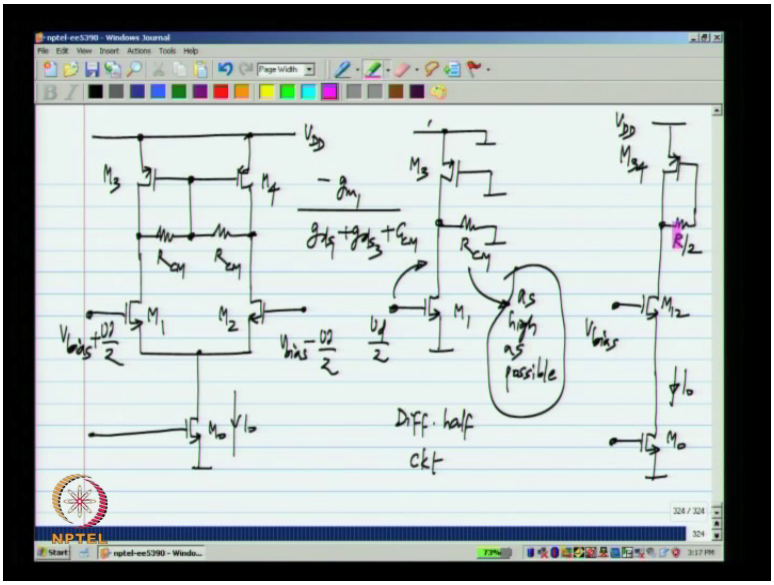

This is my fully differential of opamp or the simplest realization of the fully differential opamp and the differential half circuit is given by only one half of it by grounding all the nodes along the line of symmetry this is the differential half circuit and the common mode half circuit is obtained by folding the 2 halves together which gives me M 3 4 and R by 2 and M 1 2 and M 0 and here we just have V bias [noise].

This is the this is small signal ground that is V DD now first of all in the differential half circuit what we wanted was only this M 1 which is the trans conductance and M 3 which is the load conductance or the load current source. Now we see that we also have an extra element which is R, what is the effect of that it is very easy to see the R here appears in parallel with the g ds of M 3 and g ds of M 1 ok. So, the voltage gain from this point to that point will be the g m of transistor M 1 divided by gds 1 plus gds 3 plus this conductance g just to make it the explicit that we put it there for common mode

feedback let me rename that R cm and a reciprocal of that is G cm and you can see that this G cm reduces the dc gain of the opamp. Normally we would have got g m 1 by g ds plus g ds 3 which by the way is exactly the same gain that we get for a single ended single stage opamp ok.

Now, one thing is also notice is that the analysis of dc gain in this case the fully differential opamp is a lot easier than what we had to do for the single ended opamp this is because the half circuit concept makes it very simple to analyze we have only 2 transistors here with the resistor and by inspection we can write down the expression for the gain. Now this common mode deducting resistor R cm used in the common mode detector hence up reducing the gain.

So, you have to use as higher value has possible you have to make this to be as high as possible and just for completeness let us also look at the common mode half circuit shown on the right side. Now you see that this M 3 4 is diode connected with a resistance R by 2 in the feedback loop because the gates do not carry any dc it makes no difference at all to the dc picture [vocalized-noise]. So, this makes the connection of this type of common mode feedback circuitry to diode connection very explicit.

Now in this case in the common mode picture you see that you have a current source I naught which is pumping the current into a diode connect transistor M 3 4. So, the current in the M 3 4 will be set to a value equal to I naught it is a quite obvious if you did not have this feedback loop the current in M 3 4 could be different from I naught and this voltage would either rise or fall [noise], but now it will be set to a value equal to V DD minus V sd of M 3 4.

Now this brings us to another way of thinking about common mode feedback circuits I just now said that we need to stabilize the output common mode voltage as well now this is like having to stabilize 2 output voltages quite instead of stabilizing the 2 output voltages separately we stabilize the differential output using the differential feedback loop which determines the function of the circuit and we set the output common mode voltage to a constant value using the common mode feedback circuit. Now another way to think of the common mode feedback circuit is as follows.

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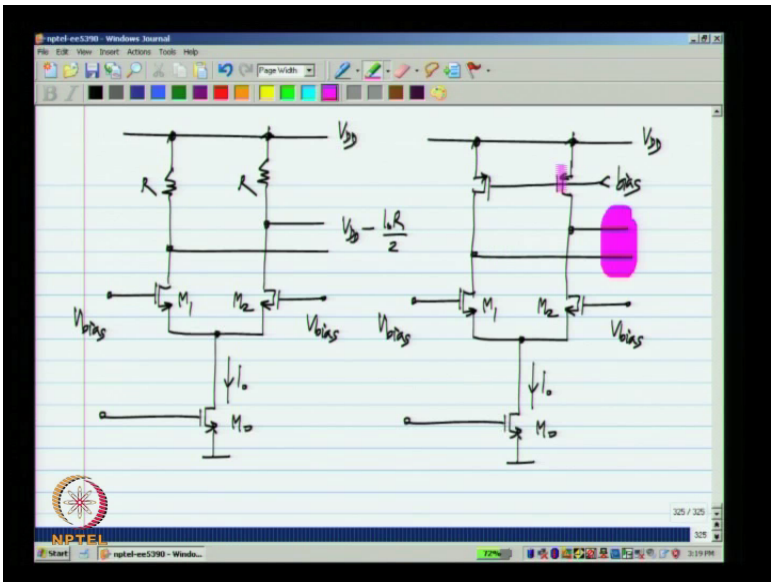

First of all when we had only a differential pair with the resistive load now what happens is that the output common mode voltage gets set to V DD minus I naught R by 2 where this is the current I naught. Now there is no problem at all setting the output common mode voltage it gets set to be V DD minus I naught R by 2 whereas, if we replace the resistances by current sources with some bias here we will not be able to tell what the output common mode voltages what is the voltage here we will not be able to tell because small differences in the current in the upper transistor and the current in the lower transistor I naught will cause this voltages to go up or down severely.

This is because as long as the load resistance is rather small the output common mode voltage will be set very accurately whereas, if the impedance of the load becomes very high as in a current source there is a lot of uncertainty because the small difference in current going into a large impedance can give you a large change in the output voltage [vocalized-noise].

So, in a way what their common mode feedback circuit is doing is shown in this figure on the right it basically presents a small impedance in the common mode in the common mode the transistor M 3 4 is diode connected whereas, in the differential mode you see that the gate of M 3 is grounded. So, there is no feedback at all in the differential mode around M 3 [vocalized-noise]. So, the goal of the common mode feedback circuitry can

also be thought of as providing a load resistance which is very low for common mode and very high for differential mode.

Ideally the common mode feedback circuit should not affect the differential mode circuit at all, but in reality it does to some extent as we see here it presents a load resistances R. In the next lecture what will do is look at different kinds of common mode feedback detectors and the look at some choices which will not affect the differential picture and consequently we will not affect the differential gain. In summary we need to have an extra feedback loop in fully differential circuits that is to stabilize the output common mode voltage.

Now in order to do this we need to be able to deduct the output common mode voltage and feed it back to some current source in general in any high gain circuit there is a current source on the bottom driven by the signal perhaps and there is a current source on the top perhaps providing a constant current this is invariably the case you go back to any of the opamp circuits we have studied so, far you will find that this is the case. Now the need for the current sources is obvious they give you a very high incremental output resistance and consequently give you very high gain.

Now a very high gain also implies that output voltage is very sensitive to small changes in current that is the definition of the gain in fact. So, if you do not match the upper and lower current sources accurately the output common mode voltage will not be stabilized accurately. So, you have to stabilize one of the current sources using negative feedback you cannot have 2 current sources in open loop one on top of another to do this we detect the common mode voltage compared to the desired common mode voltage and feed it back to the common mode current sources.

The in the simplest realization we did not do the comparison explicitly we simply fed it back directly ah. So, the output common mode voltage will not be something that we set [noise], but it is related to the properties of the transistor [noise], but none the less that is how common mode feedback in general words now the common mode feedback circuit provides a very low impedance in common mode and very high impedance in differential mode.

In the differential mode there should be no feedback at all if the common mode feedback circuit is designed properly. In our case the common mode feedback circuitry is affecting

the differential picture because the common mode detector is made using resistors in the next lecture we will see how to make common mode detectors which will not affect the differential picture.

Thank you.

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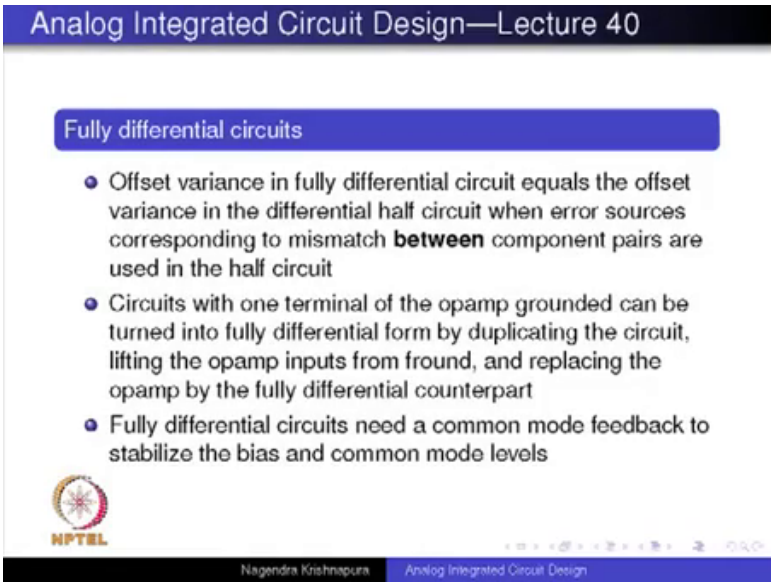

[noise]