Analog Integrated Circuit Design
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Lecture - 38
Common Mode Rejection Ratio

Hello and welcome to lecture 38 of Analog Integrated Circuit Design we have been looking at opamps at the transistor level and some detail we saw how we can make a single stage opamp and improve the DC gain by adding a second stage and a third stage. So, now we had already discussed all these things at the control source level, now we also know how to make it at the transistor level. We also saw that the different stages of the opamps will be biased properly only when DC negative feedback is applied around the opamp.

This is something that we knew already that an opamp was always be used in DC negative feedback now you can see why if you do not do that one or more of the stages inside the opamp will not be biased correctly. Now, in this lecture we will mainly talk about one particular aspect of the opamp and also many another circuits that is the common mode rejection.

Now before we go there I will briefly touch upon how to get even higher gains let us say with the two stage opamp it is a very simple technique it is a combination of things that we have seen already; we look at that and then look at common mode rejection of different circuits and why it is important and so, on.

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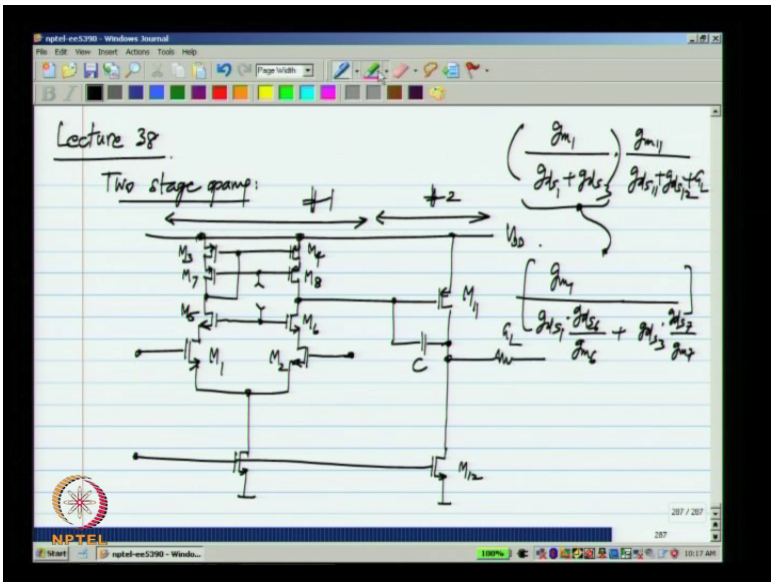

Now, our two stage opamp look like this, this is the first stage and that is the second stage and this is the output, now if you want to have an opamp with a higher gain then we can of course, go for a three stage opamp, but that needs a more complicated frequency compensation scheme and so on we need to make sure that each of the smaller loops is stable.

Now, a simple technique to increase the gain of this opamp is to simply replace the first stage instead of using the simple differential pair single stage opamp we can use a cascaded single stage opamp, for example, I can use a telescopic cascade opamp I will not show all the biasing details here. So, assume that these voltages are appropriately set to keep all transistor in saturation.

Now, what happens is the gain of the first stage is higher originally we had a total gain of plus G L which is the conductance of any load that you connect now this part of it will replaced by. So, it will be replaced by the expression for the gain of the cascode amplifier this number is going to be much higher than that one. So, the overall gain also is going to be correspondingly higher. So, this is the simple way of increasing the gain d c gain of the two stage opamp and the integrating capacitor or the compensating capacitor exactly the same as before.

So, similarly we can use a triple cascade or a folded cascade as the first stage now whether you choose to do this or not depends on the available hydrom the input common

mode range that you require and so, on, actually it is becoming very common to do this because as you go to deep submicron processes the value of g m by g d s of a single transistor whether short channel length is rather small. So, you need to have higher gains and very convenient way of getting reasonably high gain is to use the cascoded first stage followed by a common source second stage.

Now, we will move on to a very important topic with a opamps and many other circuits in fact, which is the common mode rejection. Now we have dealt with this earlier I showed the example of an inverting amplifier and a non inverting amplifier now the amplifier was assume to react not only to the difference between the input voltages, but the opamp also reacts to the average value of the input voltage or the common mode input voltage.

In this case we saw that there is a distinct difference in the behavior of the non inverting amplifier and the inverting amplifier and that is because the non inverting amplifier has a very large input common mode voltage for the opamp whereas, the inverting topology has a very small a common mode voltage swing. Now, let us look at the common mode rejection of the opamp that we have design and also we look at another circuit for which will calculate the common mode rejection and see what the bad effect of having a poor common mode rejection as.

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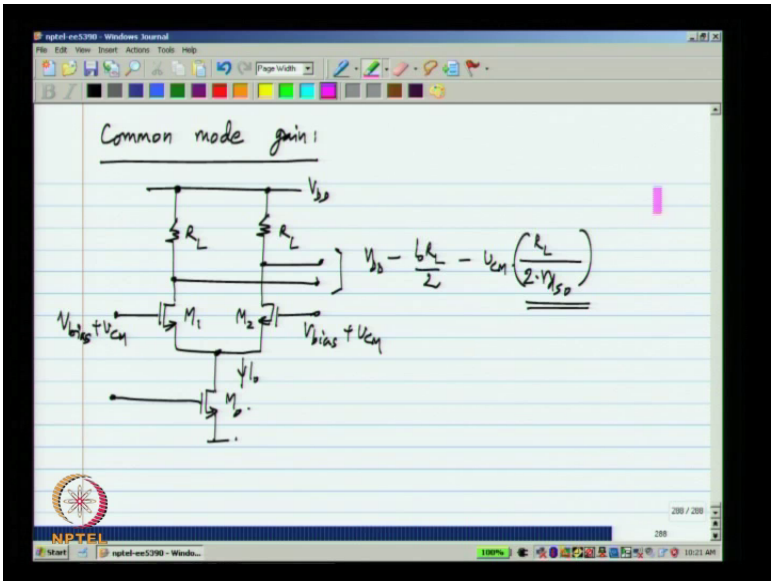

We have already looked at a common mode gain of a stage like this loaded by R L we know that if we apply a small single common mode voltages to the two sides; the outputs will rise up together and the common mode gain will be this is approximately the common mode gain I have ignored the g m s of M 1 and M 2 are assume that the output resistance of M naught is so, large that the common mode gain can be approximated by R L by 2 time rds 0.

So, we can improve the common mode rejection by improving the rds of the tail current source M naught and that is basically mainly what decides the common mode gain and consequently the common mode rejection ratio.

Now, the single stage opamp we have it is a slightly different topology.

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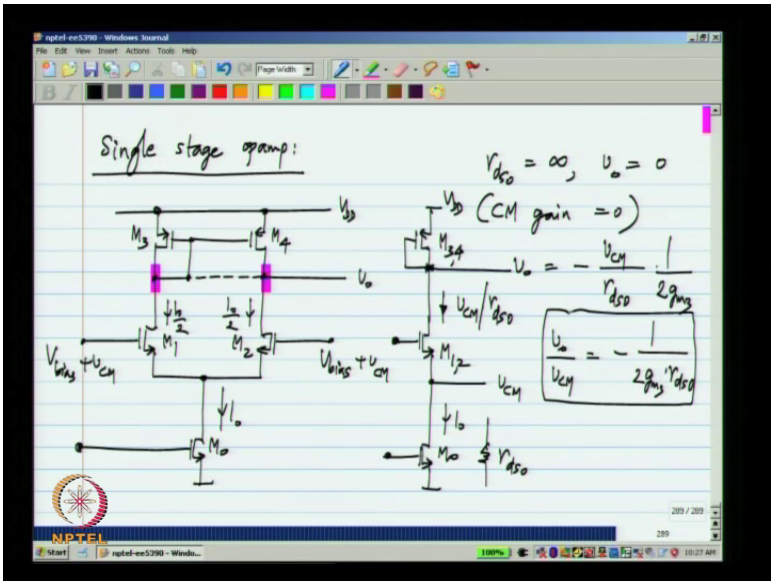

We do not have resistors, but we have a current mirror load, let us say again we apply only a common mode small signal input that is identical inputs to the two sides of the differential pair. Now how do we figure out the what the output voltages first of all we know that when the circuit is perfectly symmetrical that is M 1 and M 2 are identical M 3 and M 4 are a identical the voltages here and there will be exactly identical.

We have argued earlier by contradiction that if this voltage was difference from the other you will find some inconsistency, because you can consider the currents in M 1 and M 2 and the effect of V ds upon them and similarly the currents in M 3 and M 4 and the effect

of their V ds upon them and you will find that the only consistent solution is to have V naught equal to that voltage.

Now, when you apply equal voltages to the two inputs V cm and V cm the same thing still applies. In fact, we can think of this is simply changing V bias we have not changed anything at all. So, that is one thing now also the currents will divide equally between M 1 and M 2 if the current here is a certain value of I naught the current here will be I naught by 2 and the current there will be I naught by 2.

Let us say the current source M naught is ideal that is the this I naught does not depend on the voltage across M naught in that case even if you apply the signal here this voltage will change the voltage at the tail node will change, but the currents do not change. So, that, voltages at the drains of M 3 and M 4 will remain as they are. So, as before if rds 0 is infinity the output voltage will be 0 that is the common mode gain will be 0.

But of course, in reality this current source will be imperfect and we will have some change in the voltage, what happens is when you apply V cm this voltage will change and how do we evaluate the changes and. So, on the easiest way to work this out is to make use of the fact that the drain voltages of M 1 and M 2 are identical. If these two voltages are identical what you can do is to simply tie them together and analyze the circuit this is the very common technique of analyzing circuits.

So, I am going to do that and the circuit will become a lot simpler, so, if I do that what happens is M 1 and M 2 are in parallel and M 3 and M 4 are in parallel and I will rewrite the circuit with M 1 2 which means that it is a combination of M 1 and M 2 and we have M 0 as it is and here we have M 3 and M 4 in parallel and there drain is connected to the gate because you see that all these three are connected together and V bias plus V cm is applied there, now as we saw before the transistor M 1 2 behaves like a source follower. So, any signal at the gate appears at the source with a gain of almost unity.

Now, we know that this answer is different when you have body effect and also when you have a finite resistance rds 0 4 M 0 I let you work that out workout the exact result here I will approximate the voltage of the source by V CM. Now if this is V cm and the transistor M 0 as a as an incremental resistance rds 0 the incremental current here in this transistor will simply be V cm divided by rds 0 and that incremental current flows into the gm of M 3 and M 4 in parallel.

So, the output voltage will be nothing, but minus V cm by rds 0 and the impedance looking into the diode connected transistor will be the combine gm of M 3 and M 4 which will be 1 over 2 gm 3. So, V naught by V cm is simply equal to minus 1 over 2 gm 3 rds 0. So, couple of things to not just like before the quality of the current source decides the common mode rejection, but also the situation is better than before by using the active current mirror load what we have got is an enhanced common mode rejection.

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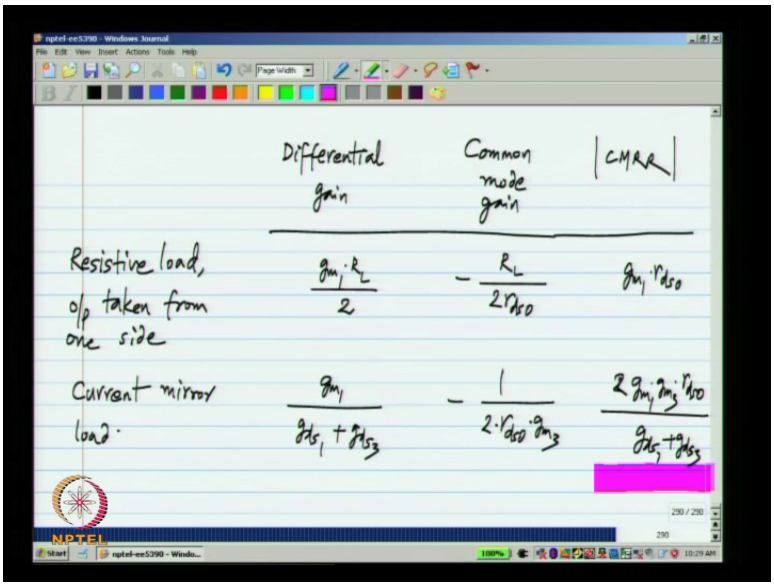

Now let us say we have a differential pair with a resistive load and output taken from one side the differential gain will be gm 1 R L divided by 2 and the common mode gain will be R L by 2 rds 0. It will be negative and if you have a current mirror load the differential gain will be gm 1 by gds 1 plus gds 3 and the common mode gain will be minus 1 over 2 rds 0 gm 3 and the contrast is obvious.

If I calculate the CMRR which is the ratio of differential gain to the common mode gain and I will just show the absolute value of that which is gm 1 times rds 0 in this case, you see that R L by 2 appears in the differential gain and also in the common mode gain whereas, with the current mirror load in the differential gain we get 1 over gds 1 plus gds 3 and in the common mode gain we get 1 over gm 3.

The common mode load impedance is much smaller than the differential load impedance. So, that gives a further enhancement of CMRR. So, this will be 2 times g m 1 gm 3 rds 0 by gds 1 plus gds 3. So, this common mode rejection of the differential pair

with the current mirror load is much higher than that of a differential pair with a resistive load now, this is a good thing. So, this means that it does not respond as much to the common mode.

Now when you add a second stage, that second stage does not differentiate between common mode and differential inputs because the first stage is already converted the differential input to a single ended output. So, at the output of the first stage once you have a signal it cannot be distinguished whether it comes from a differential input signal or a common mode input signal.

So, the second stage will react in the same way to the common mode input to the opamp and it differential input to the opamp so; that means, that the common mode rejection ratio will not change. So, the common mode rejection is determined only by the first stage this is a common characteristic all opamps and with an active current mirror load the common mode rejection ratio is much better.

Now while synthesizing the opamp topology we came up with the current mirror as a convenient way of providing a bias for the current I naught by 2. So, it is actually a lot more than that is not merely providing a bias it is also providing an enhance common mode rejection.

Now, what is the effect of common mode rejection on the operation of the opamp we have already seen what happens with inverting and non inverting amplifiers, now we are look at another example about operating with different supplies and common mode voltages for the amplifiers and see what happens, I earlier said that any opamp can be operated with the single supply or a dual supply.

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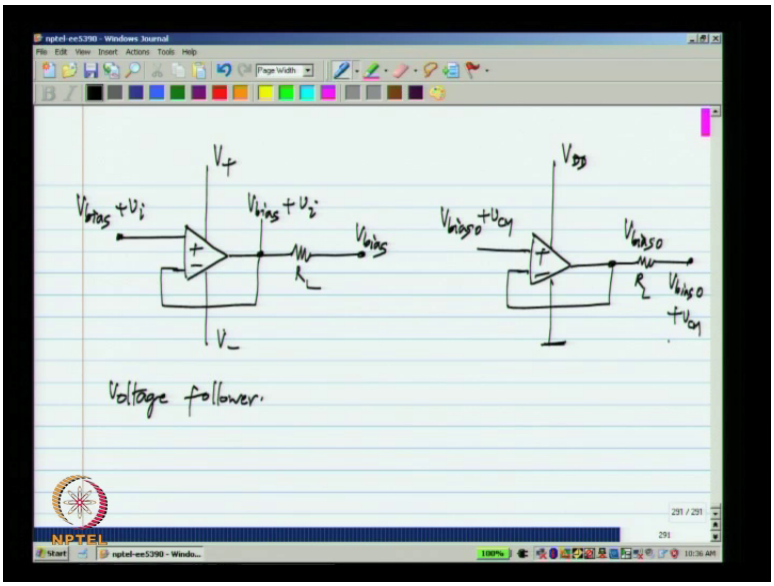

Now let me take a very simple amplifier which is a voltage follower now what does it mean to say that I can have a single supply or dual supplies first of all what it means is I can have any value of V bias here and V bias is there and I can apply an input signal and output here will be at the same V bias plus V i.

Now, this is true if the common mode rejection of the opamp is infinite. So, regardless of any value of V bias the output will be equal to V bias and any increment that you apply will come out exactly as you applied. Now in case of cmos opamp so, we talk about a single supply operation which is some V DD and 0 and we apply bias V bias the load is connected to the same V bias.

Now what is it mean to say that the opamp has a finite common mode rejection what it means is, that the output voltage will change depending on the common mode value. So, what it really means is just for simplicity let me remove the load resistance because of a finite common mode rejection as I change the value of V bias the output will change, now how do they change ideally if I apply any value of V bias there V bias should come out because this is a unity gain follower and let us assume that the opamp does not have any offsets and so on in reality what happens is different.

Now, let us assume that there is some value of V bias V bias 0 for which the output is exactly equal to V bias 0. So, let us assume that there is some voltage for which the output of this is exactly equal to that one this is the ideal operation of the voltage

follower. Now, let me change the value of V bias, you can think of this is changing the value of V bias or changing the input, have put the load back just to emphasis that the other side of the load is connected to V bias 0. In this case again no current flows through R L and the situation is exactly as before if for V bias 0 the output will be V bias 0 and the opamp does not supply any current.

Now, let me change the value of V bias 0 that I will think of is applying some common mode voltage. So, I will apply a common mode voltage to this and a common mode voltage to that one. Now what should happen is that the output should be at the exact same incremental voltage as before, the common mode rejection ratio is extremely important in many circuits.

Now in the cases that we have taken so, for it depends on the topology of the opamp now what happens if you have a finite common mode rejection ratio is that if you change the input common mode voltage of the operation the opamp behaves differently. So, the output offset for instant depends on common mode input of the opamp. Now, earlier we said that the opamp can be operated either with a single supply or a dual supply and the behavior will be exactly the same.

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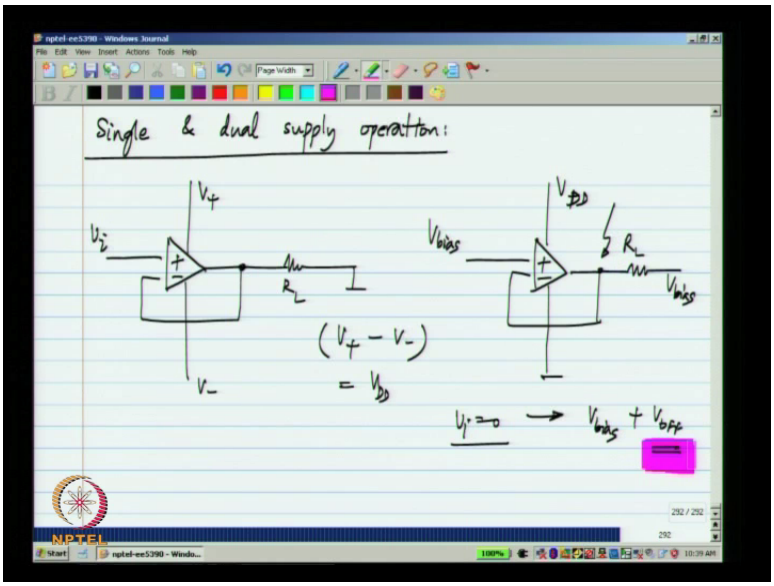

Let us say we have any circuit for simplicity I will take voltage follower I said that we can operate with a 0 common mode voltage and only an input that is 0 bias voltage and only an input or let me call this V DD and 0 and have a bias voltage for both the input

and output and if I apply an increment here. I will get the same exact same output in the 2 circuits provided that the supply voltages are the same that is V plus minus V minus the total supply voltage equals V DD minus 0.

Now, reality somewhat complicated because so, for we have not discuss the influence of V bias at all we only said that this value of V bias has to be within the input common mode range of the opamp we know that there is some input common mode range for the opamp and that is decided by the input stage now with and V bias can be anywhere within that range.

So, in reality what happens is if the value of V bias changes because of the non 0 common mode gain of the opamp the output will change in somewhere. So, let us say I do not have the input now as I go on changing the V bias the output will change in somewhere. Now when I do not have an input that is like saying I have V i which is equal to 0, when I have V i equal to 0 what should the output be it should be V bias, but there will be some offset voltage from V bias.

Now what does it mean to say that I have a non 0 common mode gain when I change V bias the output will change so; that means, that I have changing output offset voltage. So, if you think of a dc voltage follower what happens because of the non 0 common mode gain of the opamp is that the output offset will change. When you have a dynamic signal like a sine wave now in every part of the sine wave we will have a different offset and this is like having a distortion.

Now, this is a very important thing. So, it is not true that the input can be biased anywhere within the common mode range now depending on the common mode rejection ratio as you change the input bias voltage the output will change. Now to minimize this effect the common mode rejection ratio has to be as high as possible.

Now, in general this common mode rejection is something that bothers you whenever you intend to take the difference of two signals, but you also end up responding to the average of the signal. Now a voltage is always measured between two points and you always want to take the voltage between two specific points. Now there are many cases in which the voltage across those two points is rather small, but the average of these two voltages with respect to ground is very large.

Now, why is the average voltage relevant because in general we will not have any circuit that responds only to this voltage ok.

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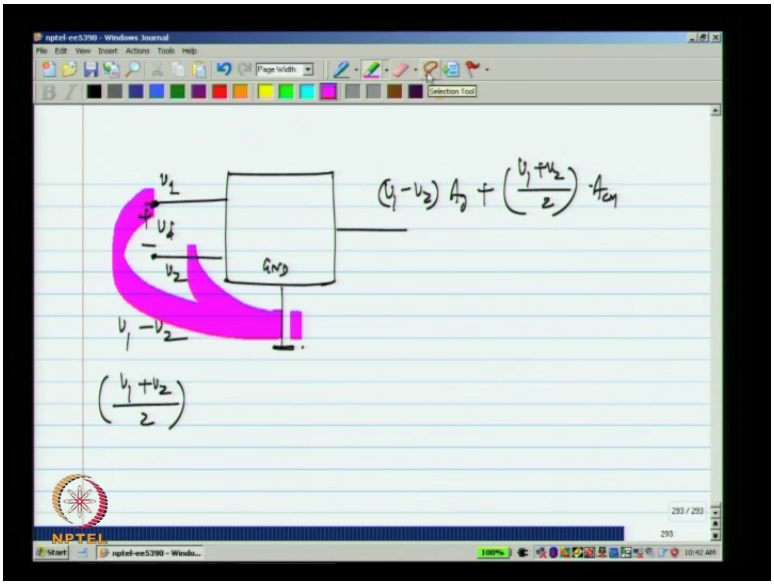

Now all circuits will have some common reference point which is the local ground of the circuit and what you really respond to is individual voltage is V 1 and V 2 with respect to ground. Now you design circuit. So, that it respond predominantly to V 1 minus V 2 and it does not respond to V 1 plus V 2 by 2 as we have discussed earlier we can think of the voltages V 1 and V 2 individually or as the difference and common mode voltages.

Now, because it always responds to the two individual voltages V 1 and V 2, we cannot always guarantee that the output response will be of the form V 1 minus V 2 times something ok. So, usually what will happen is you it will be V 1 minus V 2 times the differential gain plus V 1 plus V 2 by 2 times some common mode gain notice that this is exactly the same as writing some alpha 1 V 1 plus alpha 2 V 2, but since we usually want the differential response to be large and the common mode response to be small it makes sense to write it in this form.

So, the real problem is when A cm is non 0 and this V 1 plus V 2 by 2 happens to be large. Now, what I will do is I will discuss an example circuit for which this common mode rejection is very important and this also serves as a kind of an example for calculations of mismatch. Now, this is not related to the common mode rejection of the opamp itself, but the common mode rejection of some circuit which is supposed to

respond to the difference voltage. That is the difference between two input voltages and it is known as a.

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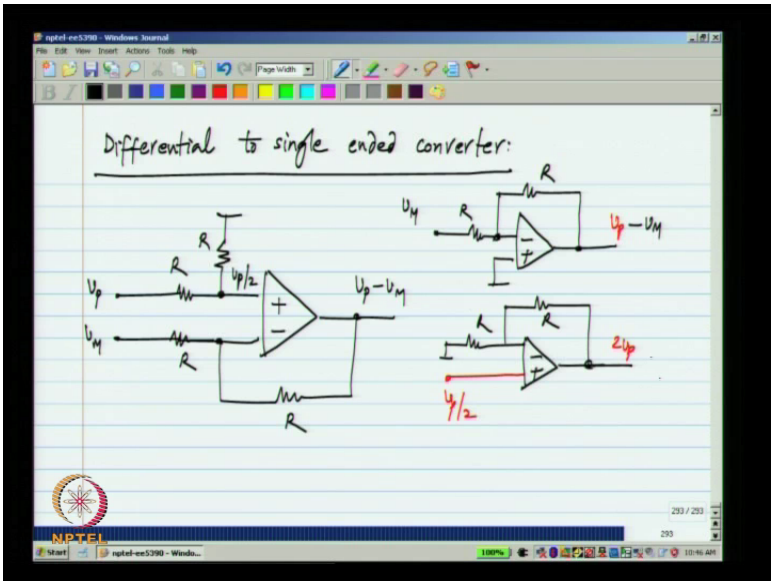

There are many cases in which you have two inputs V p and V m and you want extract V p minus V m, now how do we do that let us say I had V m alone and I wanted to get minus V m what could I do, I could use an inverting amplifier of gain minus 1. So, that is why I make this R and R I know that the output will be minus V m and this is the opamp ideally it the keep these two voltages the same and the output will be exactly equal to minus V m.

Now, what I want is not just this one, but V p minus V m that is V p must appear with some positive gain, now we also earlier discuss the relationship between inverting and non inverting amplifiers and how they are really the same circuit, but with input supplied to different places. So, let me take the same circuit and use the non inverting version instead the circuit is the same accept that I have applied the input here.

Now what do I get I know that the gain is 1 plus this resistance divided by that resistance remember for gain K we use to have R and K minus 1 R over here and K minus 1 R equals R. So, K equals 2 so, here I get 2 times V p, but what I wanted was V p now if you want a smaller voltage that is quite easy. So, what I have to do is not apply V p here, but apply V p by 2.

So, how do I get the V p by 2 from V p easiest thing in the world I just use the resistive divider and I combine the operation of these two circuits I combine these two circuits. Now from V m to the output is an inverting amplifier from V p to here it is a resistive divider and from the thereto there it is a non inverting amplifier of gain 2. So, here I get V p by 2 so, at the output I will get V p minus V m.

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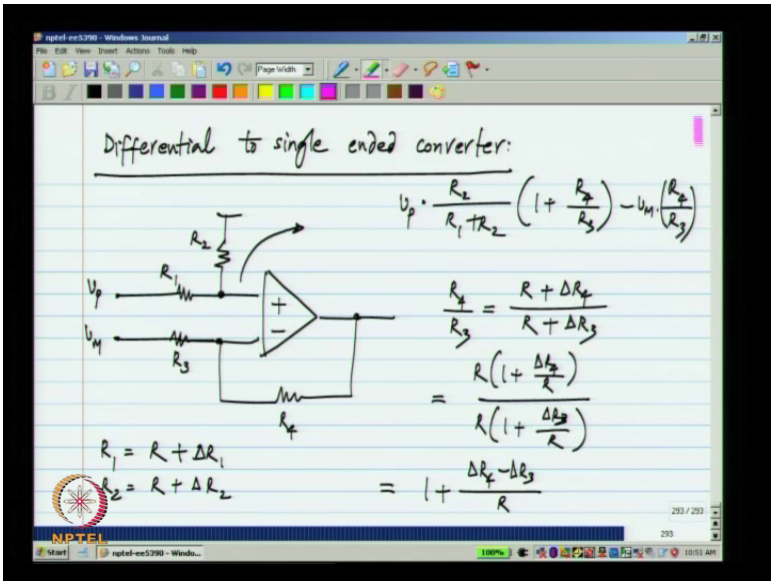

Now, this is the circuit that is used very often to convert the difference voltage into a single added voltage. So, if we have two large voltages V p and V m and you want to take the difference between them you can use this circuit and you can see that the output will be exactly equal to V p minus V m. So, what is the catch here?

Now, let us assume that the opamp is ideal. So, we are not now talking about the common mode of the opamp we know that if the opamp has a finite common mode rejection ratio or a non 0 common mode gain the output will respond to the input common mode, the input common mode here is nothing, but V p by 2 and the output will respond to that in addition to giving V p minus V m. So, that is one problem.

So, I let you work out the details of that please take it as an exercise consider an opamp with a common mode gain A cm and a differential gain A d and calculate the output. So, you will find that the common mode gain will have some effect on the output of the opamp and by reducing A cm or reducing in particular reducing A cm by A d you will improve the behavior.

So, I will not look at that I will look at a something else that can also give you a finite common mode rejection ratio or a non 0 common mode of gain. Now, what is that have you see the resistive divider as well as the non inverting amplifier both depend on the resistors ratios the attenuation of the resistive divider as well as the gain of the non inverting amplifier.

Now, in reality we are four different resistors for physically different resistors. So, there values will be different. So, this will be R 1, R 2 and this will be R 3 and R 4 of course, nominally all of them equal R, but in reality there will be some difference R 2 is R plus delta R 2 and so on.

So, now what will be the output of this circuit again please take it is a exercise and a calculate it for yourself I am going to write down the answer here, what we get here at this point will be V p times R 2 by R 1 plus R 2 and from there to the output we have a gain of 1 plus R 4 by R 3. So, that is the gain from V p and the gain from V m of course, is minus R 4 divided by R 3. Now if R 4 by R 3 happens to be 1 and R 1 by R 2 happens to be 1 this will be exactly equal to V p minus V m, but in reality we know there will be different from each other.

So, let me consider let us say one of these ratios R 4 by R 3 this will be R plus some value and it will be R plus some other value. Now delta R 4 and delta R 3 are differences from the nominal value R, now I can write this as all have done is to take R out and expanded out the ratios and I will also use the fact that delta R 4 by R and delta R 3 by R are quantities much smaller than 1.

So, what I will get will be 1 plus delta R 4 minus delta R 3 by R and these delta R 4 minus delta R 3 is nothing, but the mismatch between these two resistors and divided by R you get the normalized mismatch between the two resistors and as is obvious this expression depends only on the relative mismatch between pairs of resistors.

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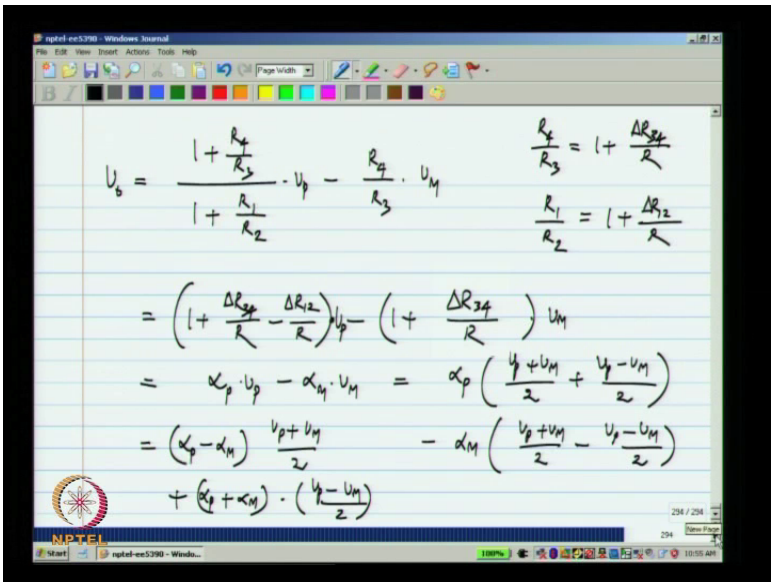

So, V out which is 1 plus R 4 by R 3 divided by 1 plus R 1 by R 2 times V p minus R 4 by R 3 times V m. Now R 4 by R 3 I said was 1 plus delta R 4 minus delta R 3 divided by R similarly R 1 by R 2 will be 1 plus delta R 1 minus delta R 2 divided by R. So, here we will have 1 plus delta R 4 minus delta R 3 divided by R divided by 1 plus delta R 1 minus delta R 2 divided by R, minus 1 plus delta R 4 minus delta R 3 divided by R this times V p minus this whole thing times V m.

I do not want to keep on writing delta R 4 minus delta R 3. So, I will rewrite this as delta R 3 4 divided by R that is the normalized mismatch between R 3 and R 4 similarly this is delta R 1 2 divided by R. So, if I substitute that that is what I am going to get now I am going to once again use the fact that this delta R 3 4 by R and delta R 1 2 by R are quantities much smaller than 1. So, this entire thing reduces to so, that is what it is going to be.

So, the output is of the form of some alpha p V p minus alpha m V m and alpha p is not exactly the same as alpha m. Now this can be written as alpha p V p plus V m by 2 minus V p minus V m sorry plus V p minus V m divided by 2 minus alpha m V p plus V m by 2 minus V p minus V m divided by 2. I have just resolved the signals into the differential and common mode components. So, which gives me alpha p minus alpha m times the common mode voltage V p plus V m by 2 plus alpha p plus alpha m times V p minus V m by 2.

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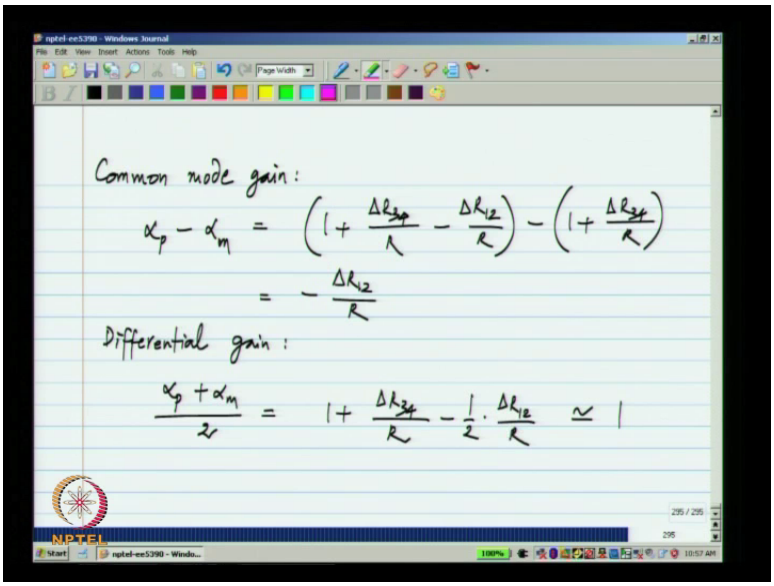

So, the common mode gain of this circuit is alpha p minus alpha m which is equal to 1 plus delta R 3 4 by R minus delta R 1 2 by R minus alpha m which is 1 plus delta R 3 4 divided by R and it turns out to be simply minus delta R 1 2 divided by R and the differential gain which is alpha p plus alpha m divided by 2 this is the number that multiplies V p minus V m and that is equal to 1 plus delta R 3 4 by R minus 1 by 2 delta R 1 2 divided by R.

Now, it is quite close to 1 it is different because of the resistor mismatch, but right now we are interested in the effects of the common mode. So, we will ignore the inaccuracy in the differential gain and say that this is approximately equal to 1. So, the common mode rejection ratio is nothing, but 1 divided by that 1. So, we will simply work with the common mode gain. So, the circuit has a non 0 common mode gain ideally it should have given an output V p minus V m in reality it gives some constant times the common mode voltage plus 1 times V p minus V m.

Now, what is the effect of a this, this a common mode gain is quite small it is a relative mismatch between register 1 and 2 it is delta R 1 2 divided by R. So, what happens because of this now what happens in reality is that let us say we consider a case where you are trying to distinguish a small difference between two large voltages.

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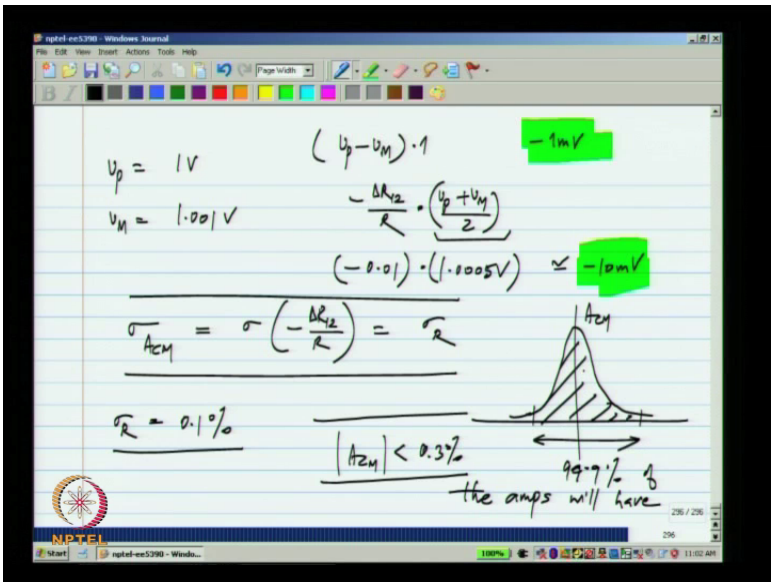

So, let us a inputs are 1 volt and 1.001 volts. So, the output will be V p minus V m times 1 this part is minus 1 mill volt plus some resistor mismatch times V p plus V m by 2. Now V p plus V m by 2 is approximately 1 volts it is 1.0005 volts so in fact, let me write that here. Now how much is delta R 1 2 by R it depends on the physical size of the resistors that you use.

Now, let us say that we have 1 percent mismatch which sound small, but let us see what happens. So, let us say delta R 1 2 by R is 0.01 just I will take some particular number. Now what happens here we will have approximately minus 10 millivolts. So, the contribution of the difference is 1 millivolt the contribution of the common mode is 10 millivolts it is much more than the difference and it is going to drawn out any difference voltage that you are trying to measure.

Now, it also turns out that this kind of circuit is used in many precision applications when let us say in thermocouple amplifiers and so on, when you have a small voltage difference and you are trying to detect only that difference. Now, because of register mismatches the effect of common mode is lot more than the effect of the difference voltage and everything is completely washed out.

So, the only solution is to choose resistors that have a very small mismatched between them now there are some other advance techniques that deal with this kind of circuits which need very good matching, but right now we will assume that we have to use this

circuit as it is. So, the only way is to make the resistors so, large that the mismatch becomes very small.

Now, also one more thing now when we measure mismatches we specify either the standard deviation or the variance. Here I just calculated the output and it comes out to be some delta R 1 2 by R which is the amount of mismatch for a particular instance of this amplifier. What we should rather specify is the standard deviation of the common mode gain and that is nothing, but the standard deviation of delta R 1 2 by R and that is nothing, but sigma R itself which is the standard deviation of relative mismatch.

Now, what does this mean and let us say we make sigma R to be something better than what we had earlier so, let us say 0.1 percent. Now, what this means is that the common mode gain will also have a standard deviation of 0.1 percent and if you plot the distribution of common mode gain over let us say a number of amplifiers; let us say you make a million amplifiers and plot the distribution the distribution will be Gaussian because the distribution of sigma R is Gaussian and 99.9 percent of the amplifier will have a common mode voltage whose magnitude is less than 3 sigma R or in other words 0.3 percent.

Now, whether this is good enough or not depends on the application. So, let us say we are interested in measuring a minimum difference voltage of 1 millivolt.

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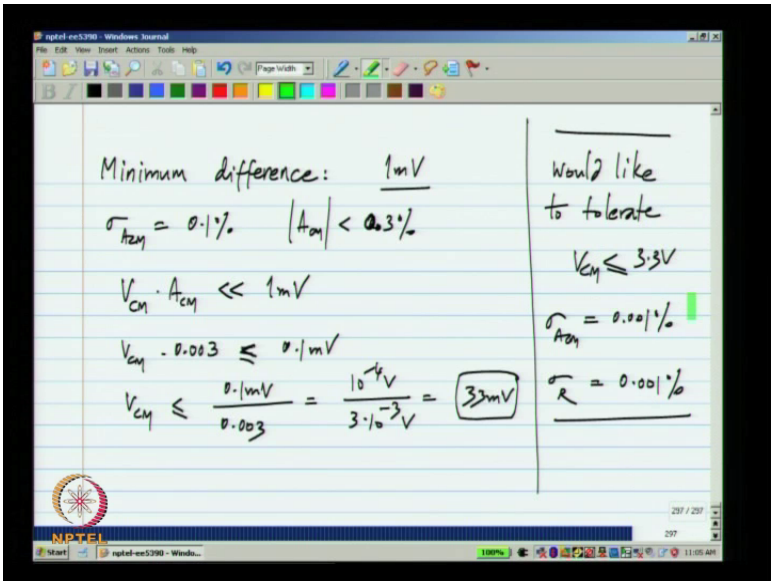

Now let us also assume; that our sigma A cm is 0.1 percent so; that means, that for 99.9 percent of the amplifiers the common mode gain magnitude will be less than 0.3 percent. Now, there is nothing secret about this 99.9 percent we will just assume that if there is only 0.1 percent of the amplifiers that fall beyond this will throw them away and use only the once that are within this range. Now or this amplifier to be usable the effect of the common mode that is V cm times A cm has to be much smaller than the smallest difference which is 1 millivolt.

Now, A cm I will take it to be 0.3 percent which is the 3 sigma value as we know the Gaussian distribution has an infinitely large amplitude, but we will use 3 sigma as the amplitude. So, V cm times A cm which is 0.3 percent which is 0.003 has to be much less than 1 millivolt. So, I will simply say it is one- tenth of this value so, that is 0.1 millivolt. So, let us say less than or equal to 0.1 millivolt so, V cm that will give you approximately 33 millivolts.

So, while this amplifier ideally gives you only the difference and completely rejects the common mode with the mismatch that we have it can only tolerate a common mode voltage of about 33 millivolts. Now let us say we have 2 tolerate common mode input voltage of 3.3 volts, that is we would like to tolerate common mode voltages of 3.3 volts this means that the sigma A cm has to be correspondingly smaller.

So, this 3.3 volts is 100 times larger than 33 millivolts. So, the sigma A cm has to be 0.001 percent or because the sigma of the common mode gain is the same as the resistor mismatch that has to be 0.001 percent. So, if you have to be able to tolerate a very large common mode voltage the, you have to use very very precisely match resistors.

Now, this is just an example circuit where the common mode rejection as important I showed this just to put the reason for common mode rejection in context and this is a very common application that you have two voltages and you have to take the difference, but the two voltages are with respect to some ground and the circuits always respond to the individual voltages or in other words the difference voltage as well as the average voltage.

Now, in general also it turns out that the response to the common mode can be strongly influenced by the matching circuits which ideally give you a 0 common mode gain can

give you a non-zero common mode gain in presence of mismatches. So, this will see further in the following lectures.

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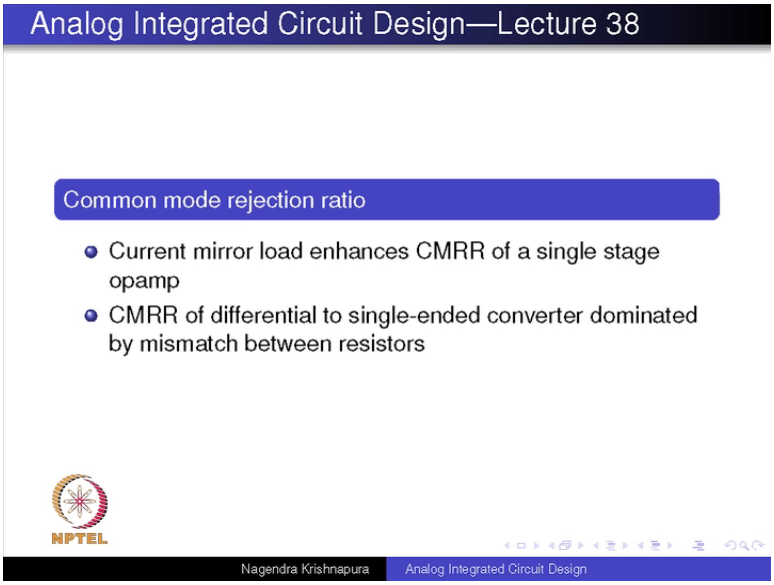

Thank you.