Analog Integrated Circuit Design
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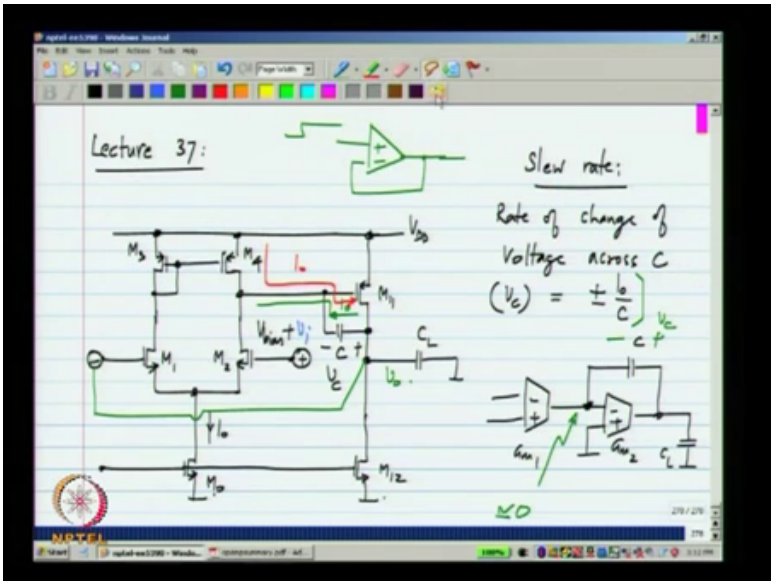
Lecture – 37
Two Stage Opamp, Three Stage and Triple Cascade Opamps

Hello and welcome to lecture 37 of Analog Integrated Circuit Design. We were discussing the two stage Op-Amp, we have calculated the small signal parameters offset and noise. We also saw that offset is contributed by a mismatch between transistors in the first stage; as well as the biasing condition of the second stage. If we make the current density in the second stage transistor equal to the current density in the load transistors of the first stage, the systematic offset can be avoided.



Now, we will calculate the slew rate and the signal ranges that is input common mode range and output signals range of the two stage Op-Amp. This is the two stage Op-Amp plus input minus input and the output and this is the integrating capacitor C. Now we have to assume that there is some load here and the load will be connected between the output and ground if it is a capacitor load if it is a resister load we will see later what to do with it. We will assume that there is only a capacitor load for now and that is why the tile current of the input stage is I naught. The slew rate as usual is limited by the amount of current flowing into some capacitor which limits the rate of change of voltages inside the Op-Amp.

As before if we test the Op-Amp then unity gain configuration that is I make this circuit and apply a step and look at the maximum rate of change of the output voltage. The input is V bias plus some step V I; now we know that for larger and larger values of V i the incremental current in M 2 becomes larger and larger for a very small values of V i; the total current here will be I naught by 2 plus G m 1 times V i. As V i increases the current in M 2 becomes larger and larger, but the increment cannot go beyond I naught by 2 that is the total current in M 2 can only be I naught at that point; 0 current will be flowing through M 1. And all of that I naught will flow from the integrating capacitor C that will be equal to I naught for large values of positive V i.

Now, similarly for a large values of a negative V i; V i that is large in negative all of the current will flow through M 1 and nothing will flow through M 2 and there is a current I naught that can go in that direction. So, what is the rate of change of the output voltage? First of all rate of change of the voltage across C this voltage V c that is equal to plus minus I naught by C. Assuming that a current I naught will flow through the capacitor. Now what will be the output voltage? Remember if you recall the representation of the two stage Op-Amp at the level of trans conductors; this is what we have G m 2 G m 1; C and C L.

Now, the second stage is supposed to be a current controlled voltage source and it becomes a current controlled voltage source because the voltage at the negative input of G m 2 is very small. If G m 2 becomes very large if the second stage has an ideal Op-Amp; this voltage will be at 0 ok; so, this voltage is approximately 0. So, V c is simply the output voltage itself V c equals V naught. So, this is not only the slew rate of the voltage across the capacitor, but it is also the slew rate of the output. So, it looks like the slew rate is similar to what we were get in a single stage Op-Amp.

But we have to consider other things here; let us say that V naught which is V c is changing at some rate.

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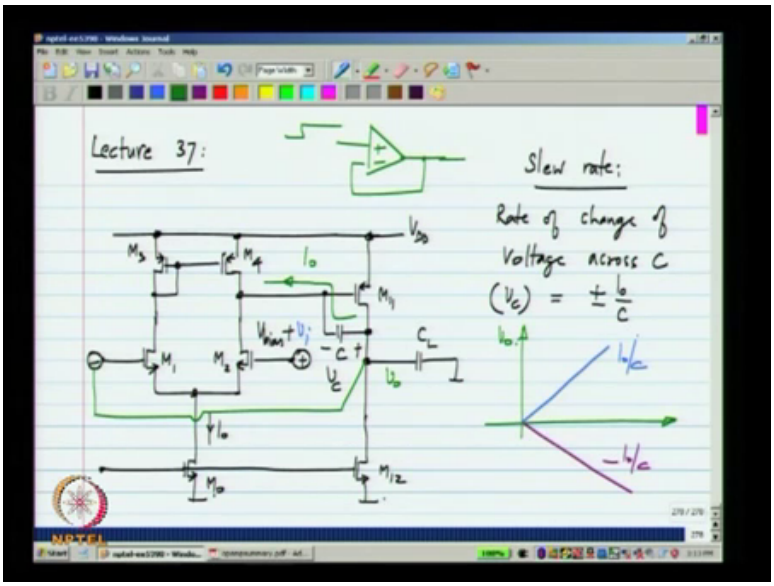

V naught is changing at a rate of I naught by C; now what does it mean? The voltage across C L which is V naught is also changing at this rate. So, the current through C L is the slope of this voltage times the capacitance. So, the current through C L would be C L times I naught by C. Similarly if the output voltage was reducing; if the output voltage was doing something like that with the slope of minus I naught by C, there would be a current in the other direction.

Also of a value C L times I naught divided by C. Now let us examine these two cases separately; first let me take the first case where a current I naught is drawn in this way so; that means, that the output is ramping up at plus I naught by C.

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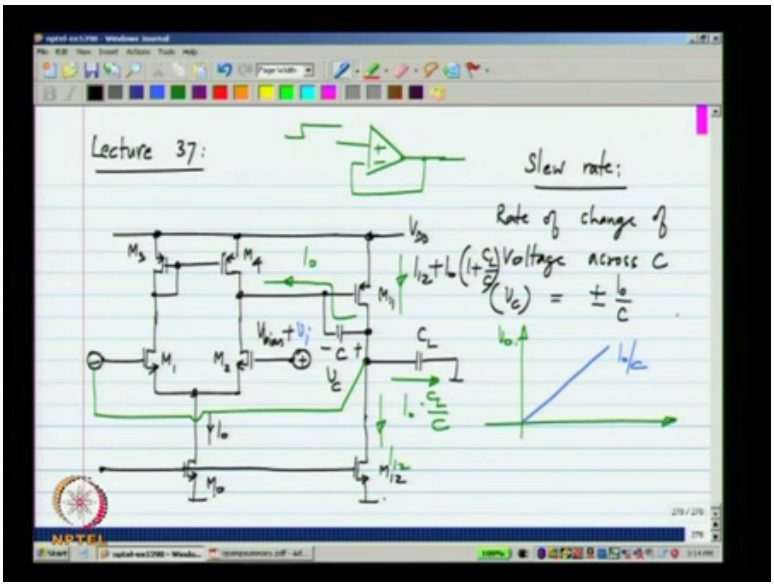

And; that means, that a current of I naught times C L by C is flowing through the load capacitor. Now what does it mean? Through M 11 we need to have a current equal to the current in M 12 which is some bias current I 12; plus the current through C plus the current through C L.

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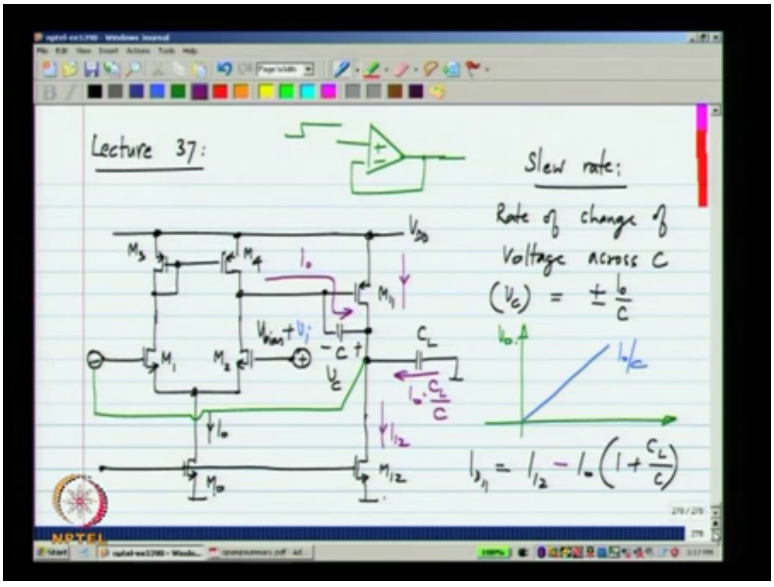

So, this is I 12 plus I naught times 1 plus C L by C ID 11 will be I 12 plus I naught 1 plus C L by C. Now is it possible to have that value? Because in quiescent condition; the voltage here would be such that the current through M 1 equals I 12.

Now, as V i increases this voltage reduces slightly and that increases the current in this. Now the total current here is limited by how far the voltage can go, but we will assume that it is not limited. So, the current in M 11 can increase in the positive direction ok; so, in this direction current in M 11 can increase while it is I 12 it can easily become this value by lowering of the gate voltage. Now this may be a little confusing earlier while calculating the output voltage; I assume that the voltage at the gate of M 11 is hardly changing. So, this is just an approximate calculation for current in M 11 to increase, the voltage here has to decrease.

So, but we just to be able to calculate the output voltage we assume that this is fixed for calculating the output voltage. Now while lowering the gate voltage of M 11 the current in M 11 will increase. So, it is indeed possible to have this current in M 11; now let us see what happens in the other direction; that is why that is I naught and that is I naught C L by C and this is some I 12. So, the current through M 11 will be I 12 minus I naught times 1 plus C L by C.

Now, is it possible for this to attain any value? Clearly not in the quiescent condition I 12 is flowing through M 11 and when you we reduce V I; I naught flows this way I naught flows that way and the output voltage will reduce. Then the current in M 1 will reduce now the smallest that the current in M 11 can be is 0 ok; the current in M 11 will reduce and the smallest value of the current in M 11 is 0. So, what does it mean?

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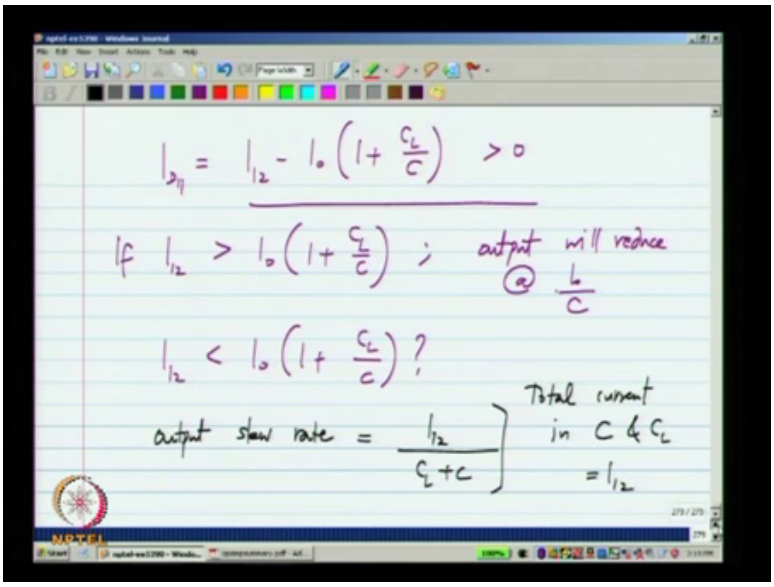

ID 11 which is I 12 minus I naught; 1 plus C L by C must be greater than 0. Now if this is the case if I 12 is greater than I naught times 1 plus C L by C, the output will reduce at the rate of I naught by C.

But what happens if I 12 is less than I naught times? 1 plus C L by C what happens in that case? Is that as we apply a negative step to V i and make the size of the step larger and larger, more and more current will flow into the integrating capacitor. Now before all of a current I naught can flow through this the transistor M 11 will cutoff because I 12 minus the current in this minus the current in C L will become 0 ok; the current in C L will always be the current in C times C L divided by C because the output is changing at the same rate ok; the voltage is across the two capacitors are changing at the same rate. So, M 11 will cut off before the input differential pair can switch completely.

So, in that case the output slew rate will be I 12 divided by C L plus C this is because the total current in C and C L must be equal to I 12 when M 11 cuts off when this cuts off some current is flowing there and some current is flowing there and the sum of the two equals I 12. If that happens then the rate of change of the output will be I 12 divided by C L plus C.

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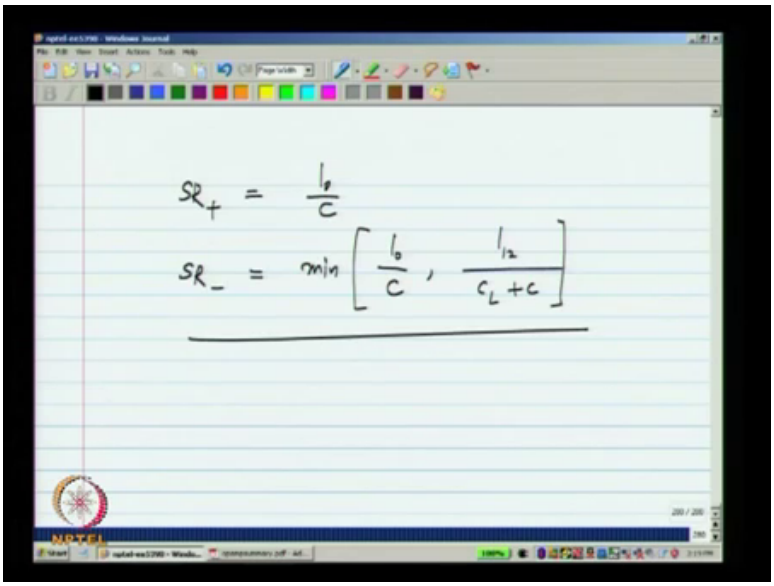

So, in the two stage Op-Amp the positive slew rate is I naught by C and the negative slew rate is whichever is smaller of I naught by C and I 12 by C L plus C. So, there are

two mechanisms of a slewing; either the input differential pair can cutoff in which case maximum current out of the first stage will be equal to I naught.

Alternatively the second stage can cutoff in which case the maximum current through C plus C L would be I 12 ah. Now which of this is limiting depends on the value of I 12 and I naught. So, it is possible for the negative slew rate to be either I naught by C or I 12 divided by C L plus C. So, this is comes out of a some simple calculation this is actually an approximate calculation because we assume that at the input of the second stage we have 0 volts, but this is good enough for practical purposes.

So, this also means that if the current in the second stage is very small; then we will end up with the rather small slew rate in one direction. And it is also possible for the slew rate to be different in the positive and negative direction. Now the next thing is the signal swings a last thing we have to determine here is the signal swing.

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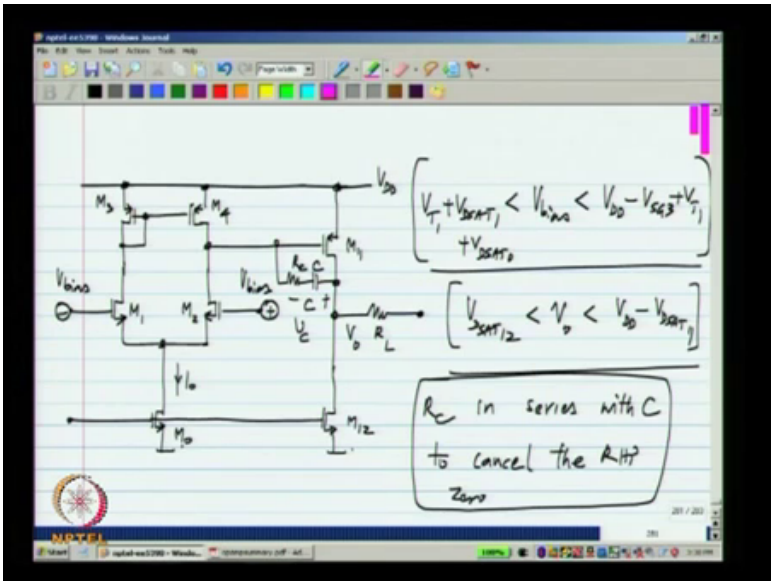

Signal swing limits let me remove this feedback loop; now what are the limits on the input bias voltage V bias? We have evaluated the this many times; if the input voltage V bias increases, the input transistors M 1 and M 2 can go into triode region. And if the input V bias reduces the tail current transistor M 0 can go into the triode region.

So, the limits are exactly the same as before; the maximum value would be the drain voltage of M 1 plus one threshold voltage. And the minimum value would be the old

drive voltage that is required across m naught to keep it in saturation region plus the regions of M 1; that will be V T 1 plus VDSAT 1 plus VDSAT 0 we can see that it close very close to V D D, but somewhat far away from the ground. And what is the limit on the output? As V naught increases there comes a point where the voltage across M 11 is too small for it to remain in saturation region. So, V naught has to be less than V D D minus VDSAT 11.

Similarly, as V naught decreases the voltage across M 12 becomes smaller and smaller and at some point it will go into triode region and that will be VDSAT 12. So, you can see that this kind of output structure where we have a single transistor connecting to the supply voltage and a single transistor connecting to ground will give you the maximum possible swing limit. It can go within VDSAT of the upper rail and within a VDSAT of the lower rail which is ground. Now in general this is the maximum swing that is possible in an integrated circuit this is the maximum possible swing in a transistor circuit.

Now, there are some special circuits where the voltage can go above the supply rail or below the lower supply rail; we will not consider that. In general we have to leave at least one VDSAT room on top and bottom.

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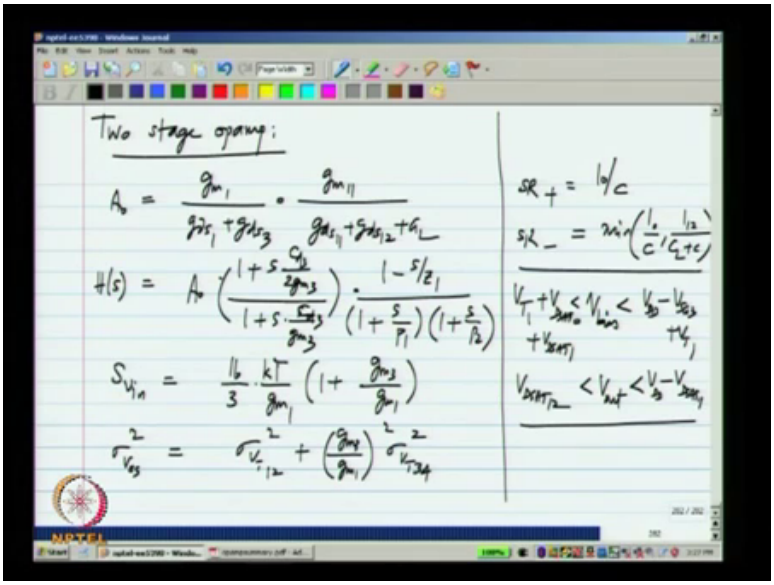

So, to summarize the two stage Op-Amp has a DC gain which is the product of the first stage and the second stage gain. And the important thing is that even if you have a

resistive load G L with a very high conductance; it affects only the second part of this term and the first one can remain very large. So, that is how we will be able to operate the Op-Amp with resistive loads; and the frequency response can be written as m m 1 the transconductance of the first stage and the 0 and pole which appear due to current mirroring. And the right half plane 0 this should be the DC gain a naught the right half plane 0 and the dominant pole and the non dominant pole.

Now, these we have spent a lot of time evaluating; I am not going to write down the expression. The dominant pole appears at the output of a first stage and the non dominate pole at the output of the second stage and the noise and offset are contributed mainly by the first stage. So, a input referred noise voltage spectral density is that and the input referred offset voltage is that one and we also calculated the slew rate and the swing limits.

So, what does the two stage Op-Amp offer is that the other Op-Amps that we studied so, far do not. First of all it has a higher DC gain it is of the order of a m m by gds square if it is a capacitive load. And even with a resistive load the first stage can be designed to have a substantial amount of gain ok; the noise and a offset are contributed only by the first stage. So, it is similar to what we would get in a differential pair and the slew rate it depends on whether the first stage or the second stage limiting it, it can be similar to what we get in a single differential pair stage.

And finally, the signal ranges the range of the input bias voltage and the output voltage are the largest we have seen so, far. The input bias range is the same as what we would get in a simple differential pair stage. And the range of the output voltage is the largest that is possible that is within a VDSAT of the upper rail and a VDSAT of the lower rail ah. Before we go further quick clarification on how we connect the load to the two stage Op-Amp; as I mentioned earlier we are operating with single supplies. So, the input signal and the load must be connected to some bias voltages.

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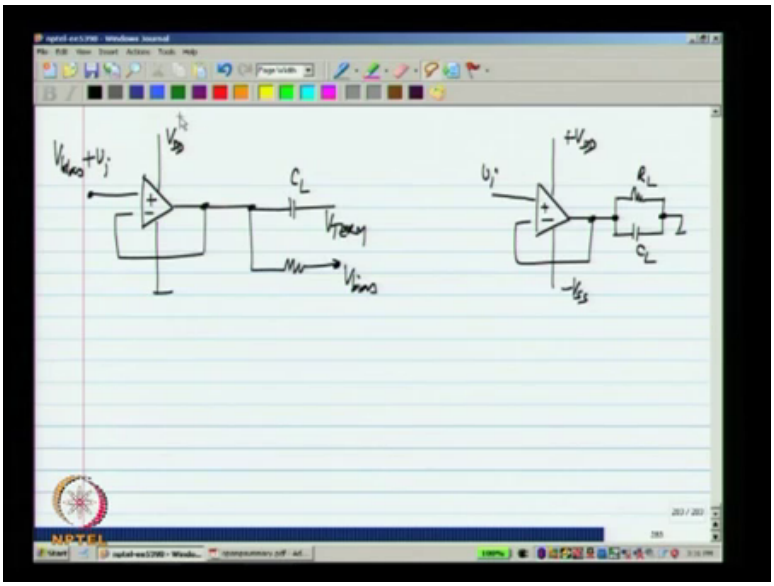

The V D D on top and the ground on the bottom; so, the input will be some V bias plus V i; I have taken a voltage follower as an example, but it can be any circuit. And the load that we have must also be connected to V bias ok; so, what happens is if V i is 0 the input is at V bias, the output is at V bias due to feedback. So, no current will flow through R L in fact, this is a very similar situation to having the conventional picture of the Op-Amp with a dual supply. And the load going to ground as was explained earlier simply by shifting all the voltages in this circuit, we get that circuit.

Now, if we have only a capacitive load it is not necessary to connected to V bias; we can connected to any voltage. Because even if we have some DC across the capacitor it is not going to draw any current; so, if we have only a capacitive load it can be connected with connected to any voltage. So, this V term can be anything, but if we do have a resistive load if the voltage on the right side is anything other than V bias; even in quiescent condition some current will be flowing out of the Op-Amp. What this means is; let us say I have a resistor here R L and this is at some V bias that is different from the quiescent output voltage, then a current will be flowing through that that has to be supplied by the transistor M 11.

So, that is not a good way to operate its best to connect the resistive load such that the quiescent output current is 0. So, when we do have a resistive load we connected up to V bias ok; now what else is there with these Op-Amps we have discussed the single stage

Op-Amp and the two stage Op-Amp; we can make a three stage Op-Amp by just following this procedure. I will not discuss that in a great detail, but I will just put on the topology here.

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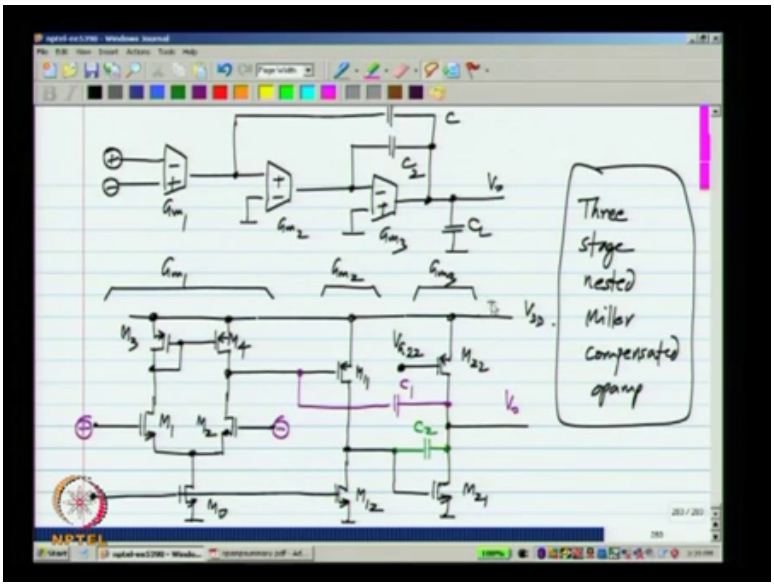

We know that at the signal level; what we need are three stages; this is the input of the Op-Amp and that is the output. We can think of it as the input G m 1 driving a current controlled voltage source with a transadmittance SC or a transimpedance 1 over SC and the current controlled voltage source is made using this two stage Op-Amp.

And the two stage Op-Amp itself can be thought of as G m 2 driving the current control voltage source with the transadmittance of SC 2 a transimpedance of 1 over SC 2. Now how would we go about implementing this? It is a simple extinction of the two stage Op-Amp that we have let us say we continue with the same topology. Now this forms the second stage G m 2.

So, this is G m 1 and it is required to take the difference between two inputs and provide an output current and G m 2 is single ended in that one of its inputs is at ground. And G m 3; now we have the freedom to chose either an N MOS stage or a P MOS stage just for a variety let me make this an N MOS amplifier ok, where this P MOS is biased at some fixed voltage.

Now, as usual that is derived from some current mirror. So, this is G m 3; now we have to connect the integrating capacitors that will be C 2 and this will be C 1. Now here I am not showing refinements like a possibly connecting resisters in series with C and so, on. So, this is the output this is the negative input that is the positive input of the Op-Amp.

Now exactly as we did before you can analyze this. In fact, the transfer function has already been analyzed and you can do the exact analysis including the 0s and so, on. The principle is the same the non dominant poles and 0s must be sufficiently outside the unity loop gain frequency so, that the system is stable and well behaved.

Now, at the transistor level the more stages you go to the more degrees of freedom you have now. One obvious one is now whether to choose a N MOS trans conductors or a P MOS trans conductor in the third stage. I have drawn it for the N MOS transconductor, but other way round is equally possible. Now you can also analyze all the other parameters like the noise, offset, slew rate, swing limits and so, on.

And for it is very obvious that the swing limits will be similar to that of the two stage Op-Amp. The input bias voltage limits or the same and the output voltage can be within one VDSAT of the supplies. The slew rate can also be calculated; it is also limited by the current in the first stage going into some capacitor and there is a possibility of the current in second or third stages limiting the total slew rate.

Now, as far as noise and offset are concerned as with any multistage amplifier they are dominated by the contribution from the first stage. And the expressions will remain exactly the same as that for the two stage Op-Amp or the simple differential pair single stage Op-Amp. Now one thing I did not mention earlier let us say we have a two stage Op-Amp. One of the refinements we can do to this to make it more stable is to add a resistance in series.

So, that the right half plane 0 is cancelled it is implemented exactly as we did in the signal level that is at the level of the transconducters the value of R C has to be equal to 1 over G m 11 in this case; 1 over G m of the a transistor M 11.

So, now to ensure that may be difficult if you use a real resistor. So, the resistor that you put there has to be matched to the reciprocal of the G m of the transistor M 11. And

sometimes what you can do is to implement the resistor also as a MOS transistor in triode region so, that the matching across process and a temperature corners is good.

Similarly if you want to tailer the 0s in series with C 1 or C 2 or both we can connect resistors in a three stage Op-Amp this is a three stage nested Miller compensated Op-Amp. Let me copy over this circuit just illustrate a couple of more details.

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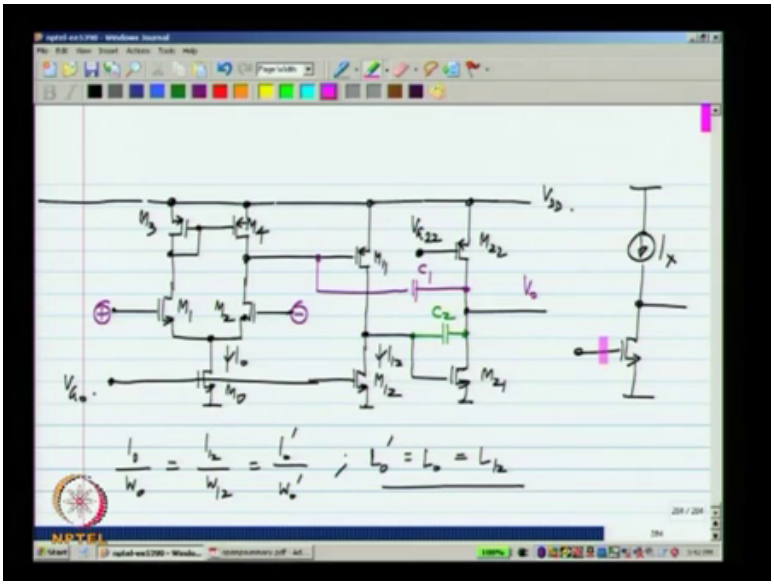

So, first of all as I have been mentioning several times the gates of a M 0 and M 22 and M 12 and so on are not connected to fixed voltages, they are always derived from current mirrors. Let me call this M 0 prime and this is I 0 prime ok; as usual whenever you make a current mirror, you make the lens of all transistors the same and the widths are in the ratio of the currents that you found.

So, let us say this is I 0 and this is I 12; that means, that I 0 by W 0 should be I 12 by W 12 which should be I 0 prime by W 0 prime and L 0 prime and L 0 and L 12 should all be equal to each other.

Now, let us say that we did not want to make a the length of M 0 and M 12 equal to each other. Then the best thing to do is to not use common biasing line for M 0 and M 12, but bias the separately from another diode connected transistor. Similarly V G 22 has to come from some diode connected transistor ok; which also is the same in length. And the width ratio is such that the current ratio is as required. So, that is how we bias the Op-

amp, but it is very cumbersome if we show every transistor in the circuit. So, it is very frequently not shown; these current mirror devices are not shown and we show only that much.

Now, the other thing is we have a current source going into the drain of the transistor and there is no other path for the direct current a DC. Similarly M 22 is a current source that is feeding into the drain of M 21. Now how is this bias properly because normally if I have something like this. So, that is a I X and this is a MOS transistor. Then what is going to happen? How much will be the current through this transistor? Unless there is feedback around this transistor; we cannot say that the current in this will be equal to I X the transistor is a unilateral device it is only by adjusting the VGS that we can change the drain current.

We cannot apply a current to the drain directly and expect the VGS to be established automatically. We have to provide a feedback from the output from the drain side to the input side to VGS. So, that the correct VGS is established for whatever bias current we want to have. Now in the Op-Amp the way we have drawn it the current sources are going directly into the drain and nowhere else. Obviously, as we know the Op-Amp can be used only inside a feedback loop.

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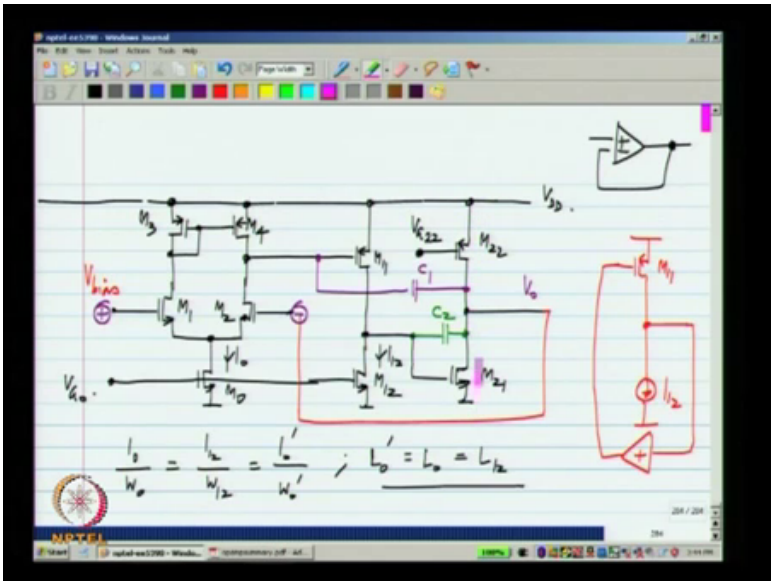

Let me again for illustration consider a unity gain fall over what happens in that case? I will have a connection from there to there and the plus input let us say is biased at some V bias.

Now, if you think of let us say this M 11 M 12 stage let me redraw that here. So, this M 12 is a current source; so, I will show it as a current source this is I 12. There is feedback through this M 21 and through the input differential pair. Now if you see from here to there is an inversion this is a common source amplifier and from there to the drain of M 2 there is an inversion. So, what we have is some amplifier with a positive incremental gain; feeding back to the gate of M 11 and we know that this is exactly what we need.

If the voltage here increases; that means, that the current in M 11 is too much and the gate voltage should be increased; so, that it reduces and vice versa for smaller current.

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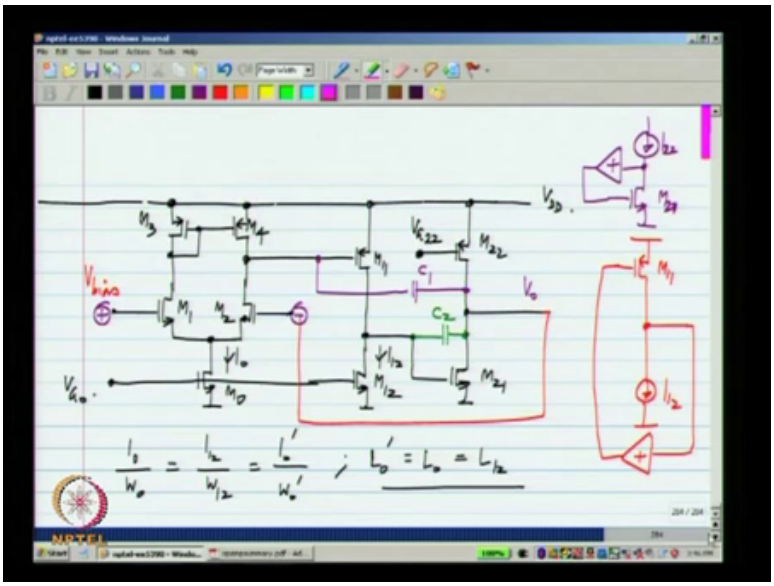

Similarly if you think of a M 22 and M 21; M 22 is a current source I 22 and this is M 21. So, that again the gain from here to there is negative and gain from there to there is negative it is a common source amplifier. So, we have a positive incremental gain amplifier connecting that way. And we know that if we do that M 21 is a negative feedback and a current of I 22 flows through that.

So, if there is DC negative feedback around the entire Op-Amp; each of these stages will be in feedback and everything will be biased correctly. If you operate the Op-Amp in

open loop there is no guarantee that the bias current will flow through the transistor because we have to establish the VGS for these transistor for the correct current to flow.

Now while discussing Op-Amp; so, we would already have heard that we have to use them in negative feedback and this is the reason. If are not in negative feedback and you apply a 0 differential input voltage there is no guarantee that the Op-Amp will be biased properly. In fact, because of mismatches and so, on there is almost a guarantee that the transistors will all be in some triode region.

One of the transistors will always be in triode region; so, that is about DC negative feedback around the Op-Amp. Now let us say the two stage Op-Amp gives you a gain of the order of G m by gds square. Let us say we want an even higher gain what should we do? We can go for a three stage Op-Amp and we can go for a four stage Op-Amp and so, on that is possible that is one of the ways of a doing it. Also there are other ways if all we want to do is to improve the DC gain; what did we have?.

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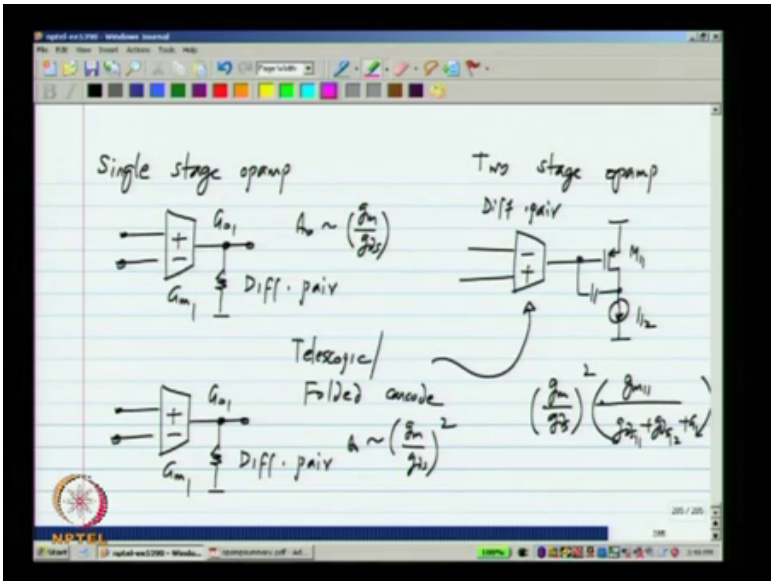

We have a single stage Op-Amp of some G m 1 and this is just the differential pair; it has some G o 1 and the DC gain is of the order of G m by gds of a single transistor.

We can also refine this by going to telescopic or folded cascode ok; what that will do is you have a similar topology, but the gain will be of the order of g m by gds square. Now when we have a two stage Op-Amp, we use the simple differential pair here followed by

a second stage that is M 11 with a current I 12; what we can instead do is to use the telescopic or the folded cascode in that stage. If we do that what happens is the gain of the first stage increases, it will be of the order of g m by gds square and the second stage will have a gain of g m 11 by gds 11 plus gds 12 plus GL. So, by increasing the first stage gain, we can increase the gain of the overall Op-Amp.

So, we can still stay with two stages which means that the compensation scheme; the scheme to be make the Op-Amp behave like an integrator is the same as in a two stage Op-Amp. But the difference is; so, we can stay just two stages and have a higher gain by making the first stage a telescopic cascode Op-Amp or a folded cascode Op-Amp. Now this is the very commonly used technique as the what was happened is that as we go to finer and finer technologies that is with shorter and shorter channel lengths ah; the problem is that the g m by gds of transistors is becoming smaller and smaller this is simply because the length is becoming smaller.

Now, you can make the length higher and get a higher value of g m by gds, but that reduces the speed. So, if you stay with shorter channel length the way to increase the gain is to go for a cascode first stage and a second stage so, that with two stages you get a very high gain. So, that is very much possible and that is also quite frequently done; now another possibility is that we use not just 1 cascode, but 2 cascodes usually such a thing is called a triple cascode.

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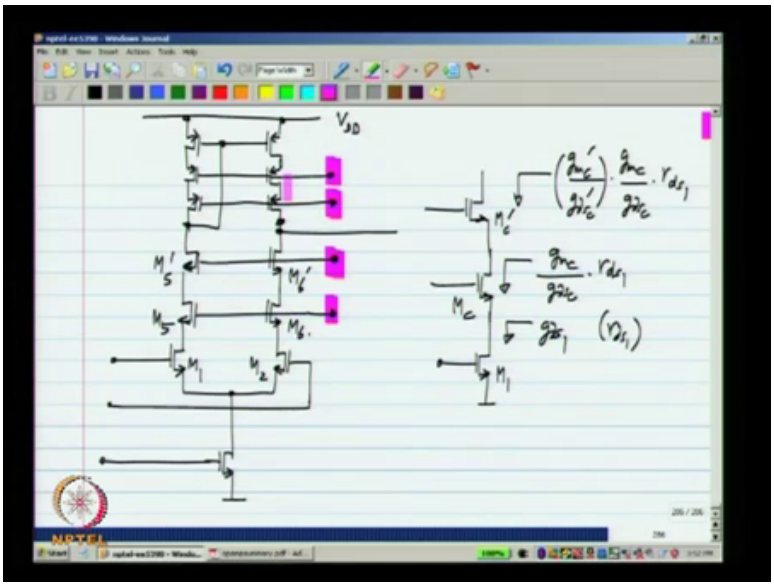

I will show it for the telescopic cascode topology; now to just to illustrate the principle; I will show also a just common source amplifier. Looking in here that is why this is M 1 I will have gds 1 as the output conductance or rds 1 as the output resistance; if I cascoded with MC the output resistance will be gmc by gdsc times rds 1. I could cascoded with one more transistor that is why M C prime the output resistance will be gmc prime by gdsc prime; gmc by gdsc times rds 1.

So, it is even higher; so, the same thing can be done with the Op-Amp as well. So, this is a diff pair with two cascodes ok; we had M 1, M 2, M 5, M 6 earlier and that is why I call it M 5 prime, M 6 prime. And similarly on top I need to have a current source with two cascodes ok; there is no point improving only one side when both sides are contributing to the output conductance.

So, I should have a current mirror which is also triple cascaded; so, we need to establish the bias voltages of all these points. So, that all transistors remain in saturation and of course, a similar thing can be done with the folded cascode as well also an additional constraint is that we have now stacked more transistors so; that means, that things will be constrained even more than before.

So, we can have more and more cascodes, but you will have a lesser and lesser swings, but when you have a two stage Op-Amp the swing at the output of the first stage does not have to be very high; so, it is possible to do this. So, some times when you want even higher DC gain you could go for something known as a triple cascode in the first stage and as second stage. So, there are lots of a alternatives and lots of possibilities this is one of the reasons why you should not try to remember topologies without understanding what is going on behind them. Because I have some basic topologies I can combine a number of them in very different ways to get seemingly very different alternatives.

But once you understand the underlying principles they are all the same. So, we started with a single stage differential Op-Amp; we went to telescopic and folded cascodes that is one way of increasing DC gain. We can go to a two stage Op-Amp that is another way of increasing the gain. So, in some ways the two stage Op-Amp and the telescopic of folded cascode will have the same DC gain; if you have only a capacitive load you have a resistive load you cannot use only a cascode stage because that only increases the output resistance, but does not increase the transconductance.

Now, if you want a further increasing gain you can go for a three stages or four stages or you can go for a triple cascode telescopic stage or a triple cascode folded cascode stage. Alternatively you can combine the two you can have a telescopic cascode stage followed by a second stage or a folded cascode stage followed by a second stage and so, on ok; the possibilities are endless and it is up to you as a designer to pick which is the right one for you. If you understand the tradeoffs very well you will be able to do that. Now as usual in design you have a number of parameters and you will not be able to put down all the parameters on paper and then turn some equations and get the dimensions of all transistors.

So, it is very important to understand what to change if something is deficient. Let us say you design a two stage Op-Amp and you find the DC gain to be too little; what can you do? You have to increase the gain of the first stage that is an easy possibility. So, you increase the length of transistors in the first stage or you go for a cascode first stage those are all the possibilities.

Similarly let us say you find that the input referred noise of your two stage Op-Amp is too much; then what will you do you know that the noise is being contributed only by the first stage. So, you have to manipulate the first stage in some way and you would not like to affect the transfer function at all.

So, you do noise scaling for the first one, you do impedance scaling or noise scaling for the first stage; now that will increase the transconductance of first stage so; that means, that you also have to change the integrating capacitor. So, that your Op-Amp behaves in exactly as same as before. So, you may have to change different things by keeping some other things constant. So, if you understand the basic principles very well you will be able to do this quite easily. Now this is a quick summary of a the Op-Amps as we have studied them; so, far this is the differential pair Op-Amp.

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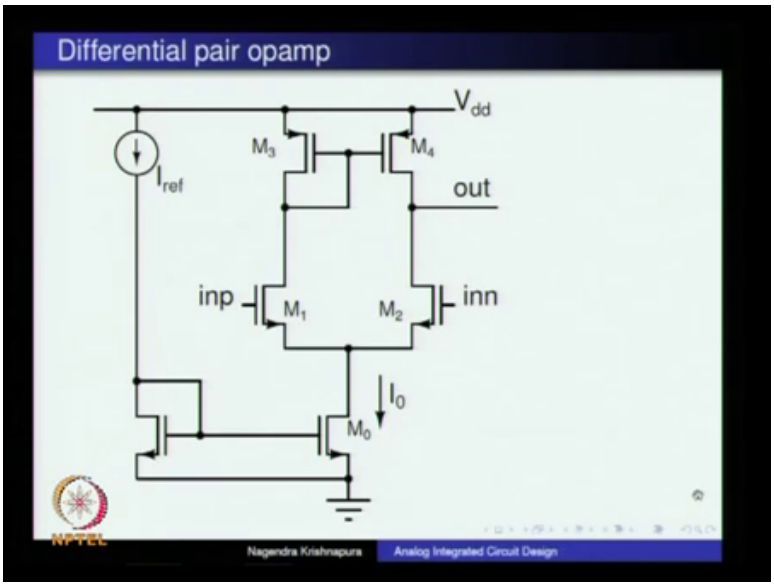

Now, the output resistance can be calculated using this.

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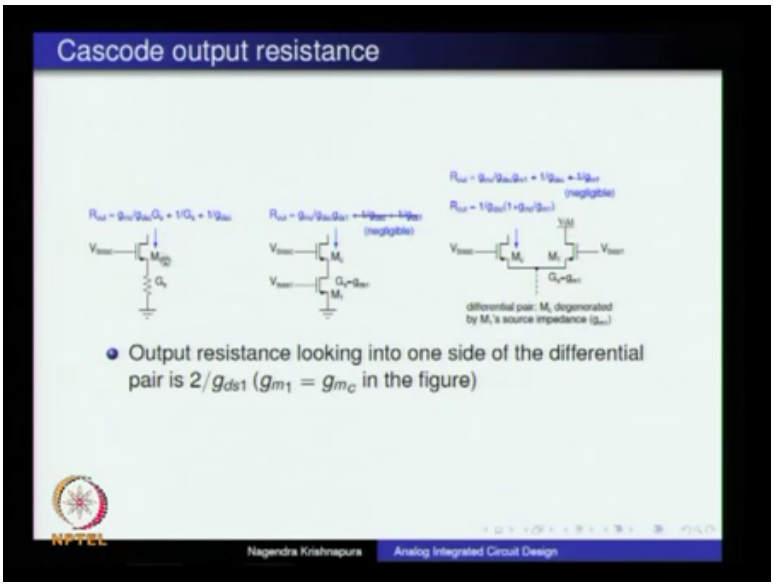

We know that the output resistance of the cascode is given by this formula when we have a resistor with conductance gs and the source of the transistor mc. So, if we have another transistor it will be gds 1 instead of gs and finally, if we have a differential pair it is as though this transistor M 1; the impedance looking at the source is at the source of this transistor M c. So, the rout is 1 over gdsc times 1 plus gmc by g m 1. And if gmc

happens to be equal to G m 1 this is simply two a gdsc or the output resistance is 2 times rdsc.

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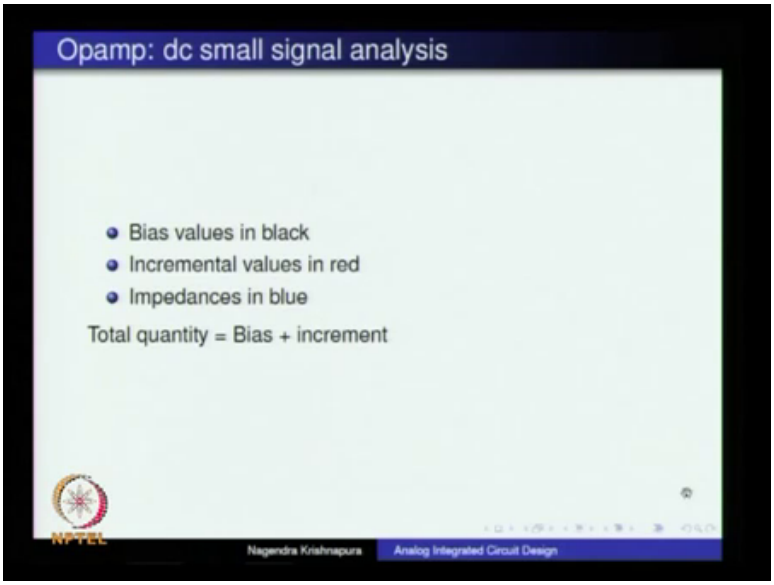

And the following slide show all Op-Amps with bias values in black the incremental values in red and the impedances in blue. The total quality of course, is bias plus increment; so, we said that this and that voltage are equal by symmetry that is how we started the analysis. So, if we terminate this with V D D minus VGS 3 nothing will flow there.

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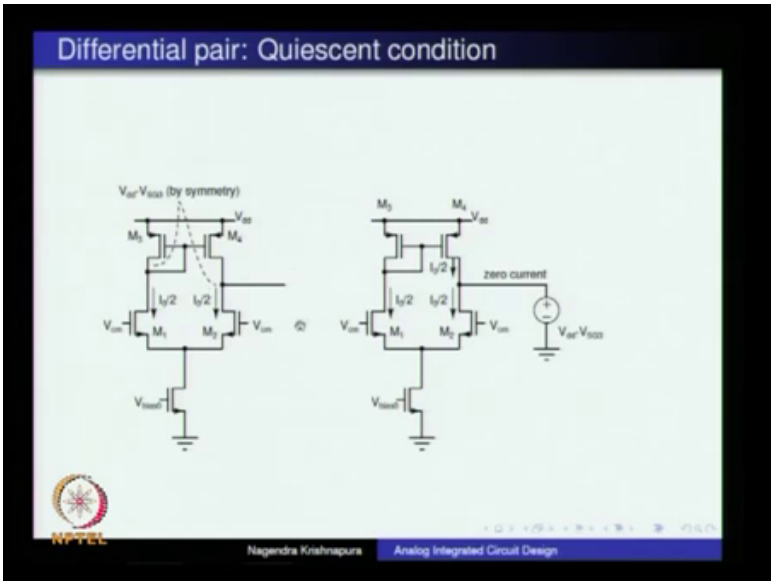

And I naught by 2 will flow through all these four transistors where I naught is the tail current.

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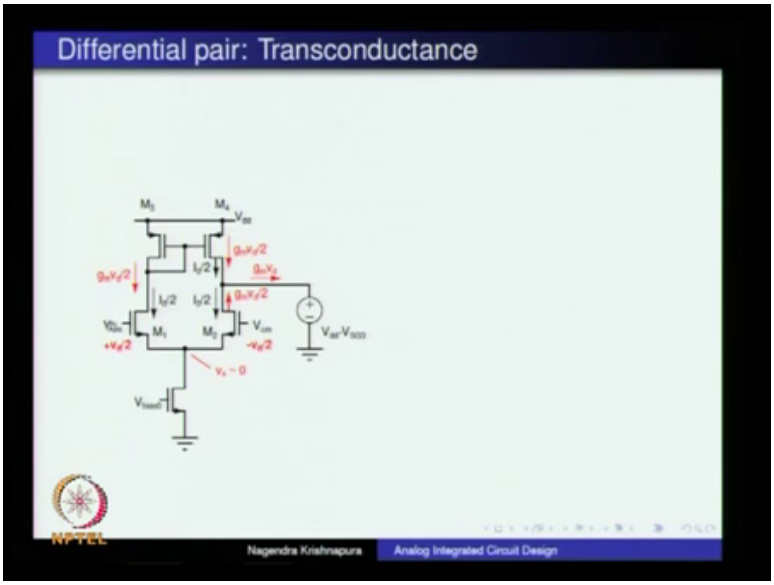

And to calculate the transconductance we have this incremental voltages v d by 2 that causes the currents gmvd by 2 here and gmvd by 2 in the opposite direction. So, net current of gmvd will flow to a output. To calculate the output conductance this is what happens if we apply a test voltage v t; we will have vt times gds 1 by 2 flowing this way and that will also get mirrored. So, v t times gds one by two will flow there plus v t times gds 3. So, that is how we get the output conductance to be gds 1 plus gds 3.

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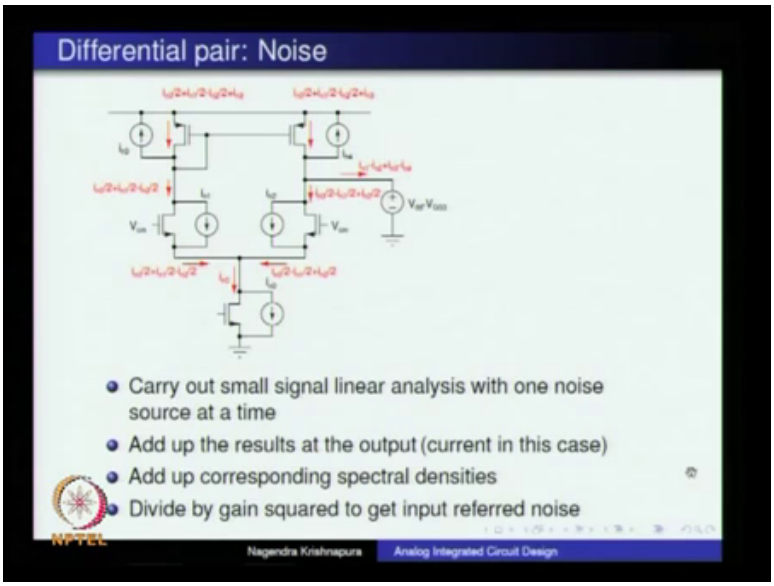

So, similarly we can calculate the noise and the other parameters; we will continue with that in the next lecture.

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