Analog Integrated Circuit Design
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Lecture - 36
Two stage opamp

Hello and welcome to lecture 36 of Analog Integrated Circuit Design. We have been looking at opamp topologies and how to improve the DC gain, and so far we investigated the couple of topologies that increase the DC gain by increasing the output resistance of the transconductor. Such an approach is not useful when we have a resistive load, because the total output conductance will be dominated by the load, and for a given transconductance we will only have a given DC gain.

To increase the DC gain we will have to increase the transconductance and this enormously increases the power dissipation ok. So, we have to go to multistage topologies, which inherently give a lot higher DC gain even with resistive loads. So, that is what we will discuss in this lecture when discussing the opamp at the control source level, this was the basic opamp.

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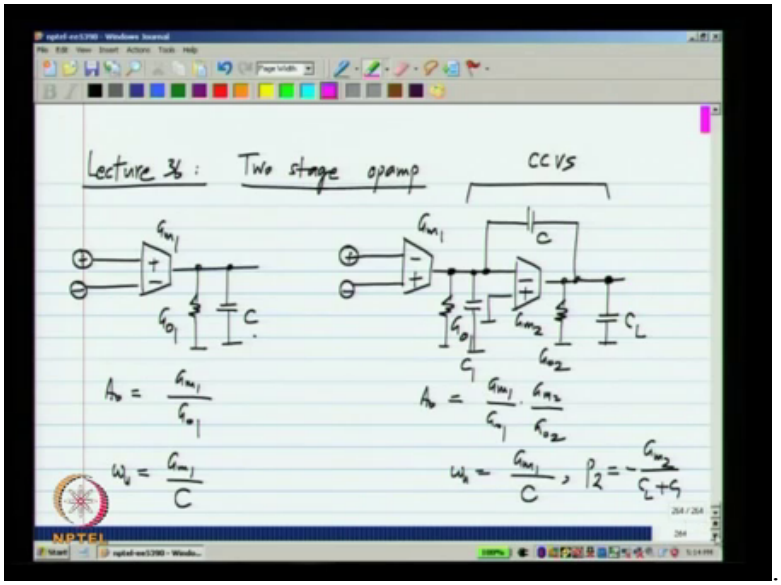

Now, we said that the problem is the output conductance of this transconductor, to obtain a better I to V conversion. The problem here is not all of the output current to the

transconductor goes into the capacitor; some of it goes into this G out. To do better, use a current controlled voltage source using a feedback circuit ok. The advantage here is that, because of feedback the input node is at a small voltage, so the current that goes to G out is quite small ok. Most of the current ends up going into the capacitor C.

So, this is a much better integrator than this one and of course, the transconductor that we use for the current control voltage source, also will have an output resistance G o 2. So, this topology we saw that has the higher DC gain. The circuit on the left side has a DC gain of Gm 1 by a Go 1, and the circuit on the right side has a DC gain of Gm 1 by Go 1 times Gm 2 by Go 2 ok, and both of these integrators have the same unity gain frequency, Gm 1 by C. Now, we also analyze this in great detail, when we have this capacitance C 1 and a load CL, we saw what happens, so we end up with two poles and A 0 and we also evaluated the conditions under which we get sufficient place margin etcetera etcetera ok.

So, we know that for instance the non dominant pole is that approximately at minus Gm 2 by CL plus C 1, because Gm 2 is in feedback we get a more complicated expression, I am going to write that soon. So, we have all the things that we need to understand this topology. All we have to do is to implement this at their transistor level. Now how do we go about doing it first of all you see that the input part of it is this is the same as before.

We have a transconductance which was driving a capacitor, now it drives a current control voltage source. We have already spend some efforts coming up with topologies for this, so we will use our single stage opamps for the transconductor, a single stage opamp is nothing, but a transconductor and that will use in place of Gm 1, and we have to realize this transconductance Gm 2 and connect the integrating capacitor across it that we will do, see how to do and complete the circuit.

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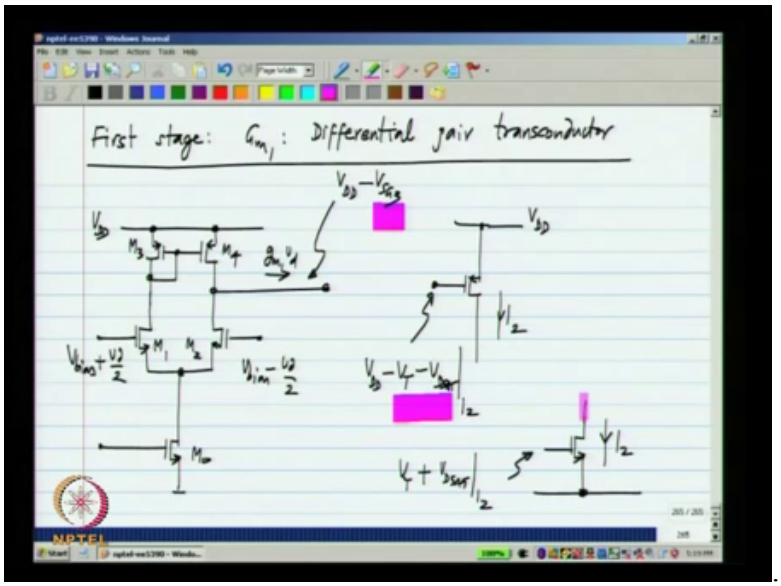

So, basically Gm 1 will be made by using the differential pair transconductor, this is what we have and this is Gm 1. We know that if we have V bias plus Vd by 2 and V bias minus Vd by 2, there is a current Gm 1 Vd that tends to flow out, if there is some proper termination on this side ok. Now what do we need here, we need another transconductor ok, voltage control current source around which we connect the integrating capacitor. Now what is the transconductor that we need to use here?

There is a variety of choices, but we will try to use the simplest that is possible and we are recognize that a transistor by itself is a voltage control current source or a transconductor ok. A common source amplifier for instance is nothing, but a voltage control current source loaded by a load resistor ok. So, that is what we will use. Now we can use either PMOS or NMOS transistor. We know that the quiescent output voltage here is VDD minus VSG 3 ok.

So, typically especially for large values of VDD, this is lot closer to VDD than to ground. Now let us say you want to have a PMOS how much source amplifier or a PMOS trans conductor biased at some current, I 2 let us say. Then the gates needs to be biased at VDD minus Vt minus Vd sat corresponding to a current I 2. Instead if you had a NMOS transistor, biased at let us say the same current I 2, the voltage would have to be Vt, the threshold voltage plus Vd sat at a current of I 2, and you see that the output voltage of the first stage is lot more suitable for biasing a PMOS transistor than an NMOS transistor ok.

If VDD minus VSG 3 as to be equal to Vd plus Vt plus Vd sat, there is some constraint between VDD VSG 3 Vt and so on. On the contrary if you want to make this equal to VDD minus Vt minus Vd sat VSG 3 has to be equal to Vt plus Vd sat and VSG 3 itself is the threshold voltage of the PMOS transistor plus some over drive. So, all we need is to have the same overdrive for this transistor as well as that transistor and the entire circuit we will get biased ok.

So, its lot easier to interface a PMOS stage to a NMOS differential pair compared to an NMOS second stage. So, for this reason we will use a PMOS second stage with an NMOS first stage; that is NMOS differential pair first stage. Now, the other topology is also possible, you can use an NMOS second stage with an NMOS differential pair and that is sometimes used when the supply voltage is very low and you can satisfy this constrains, but usually an NMOS differential pair will be followed by a PMOS common source amplifier. I say common source amplifier, what it is really is a voltage control current source that will use as an amplifier.

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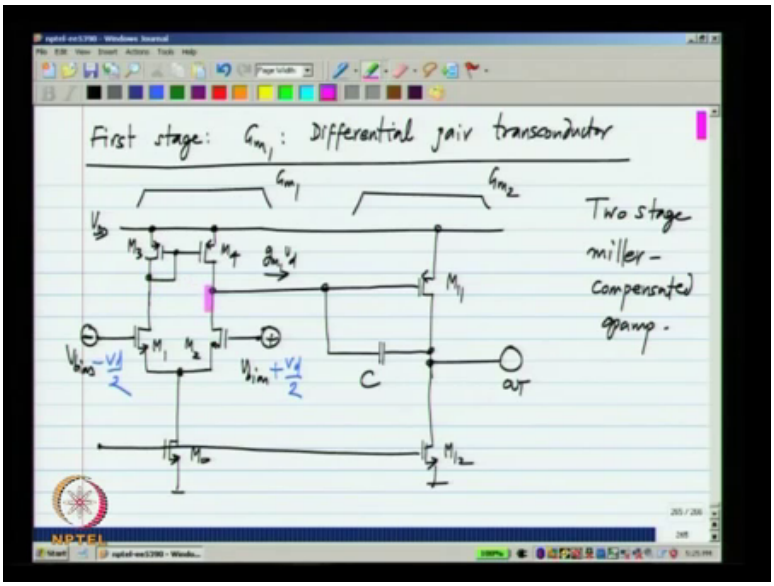

So, my second stage Gm will be that, and I would want as higher DC gain as possible in this as well, so I will not loaded by a resistive load, I will be loaded by an active current source load ok. Let me call this M 11 and this is m 12 ok, I can connect it like that and the gate of M 12 is bias from a current mirror, I will assume that if the bias is derived from the same place that we derive the bias of M naught from. By adjusting the size of M

12 compared to M naught and the diode connected transistor we can get any current that we want, we have.

Now, this is Gm 2, this is Gm 1. The first stage is the differential pair, because we also have to take the difference between the desired and the actual quantities; that is done in the first stage that is why it is a differential Gm. The second stage is simply a single ended one, because it has to take the output of the first stage. Across this we need to connect the capacitor C, this is the integrating capacitor C and we have done.

This is the output, this is the positive input and that is the negative input; that is obvious from these polarities, this is negative and that is negative, so the gain from there to the output is positive. So, this is our two stage opamp. If you recall it was also called the miller compensated opamp. Now we already know the small signal parameters of such a topology ok, let me put this down again.

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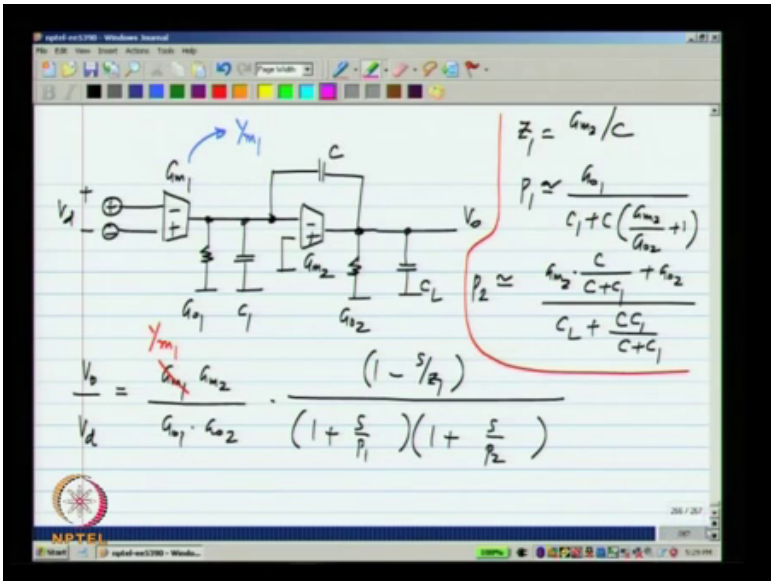

I will show only the output conductance, but if there is a load resistance that can be absorbed into the output conductance Go 2, this is Gm 1 ok. Now what is the transfer function that we have for, this for V naught divided by the difference voltage Vd or the error voltage Ve. We had the DC gain Gm 1 Gm 2 by Go 1 Go 2 and we had a right of gain 0 and we had a second order denominator which we approximately resolved into to first order factors S by P 1 and S by P 2 and the 0 G 1 is at Gm 2 by C, pole P 1 is at Go 1 by its approximately at Go 1 by C 1 plus C times Gm 2 by Go 2 plus 1, because some

other terms which we can neglect and the second pole is approximately at Gm 2 with this feedback fraction C by C plus C 1 plus Go 2 divided by CL plus a series combination of C and C 1 ok.

So, we know all of these things we have to find this for our transistor level opamp. So, the first thing we need to do, is to simply identify the values of these different components C 1 CL and C that we already know Go 1 Go 2 etcetera. And also one more thing to keep in mind is that in this log diagram we assume Gm 1 to be an ideal transconductor. In reality we know that from our analysis of the simple differential pair between the input is here.

Let us say I apply plus Vd by 2 and minus Vd by 2 and the output current; that is coming out of the first stage transconductor, there is a pole under 0 that is because of the mirroring ok. So, this Gm 1 has to be replaced by Ym 1 which is the trans admittance that includes the pole and the 0. So, if we do all of that we will get the frequency response of our miller compensated 2 stage opamp at the transistor level. Let me copy over this picture.

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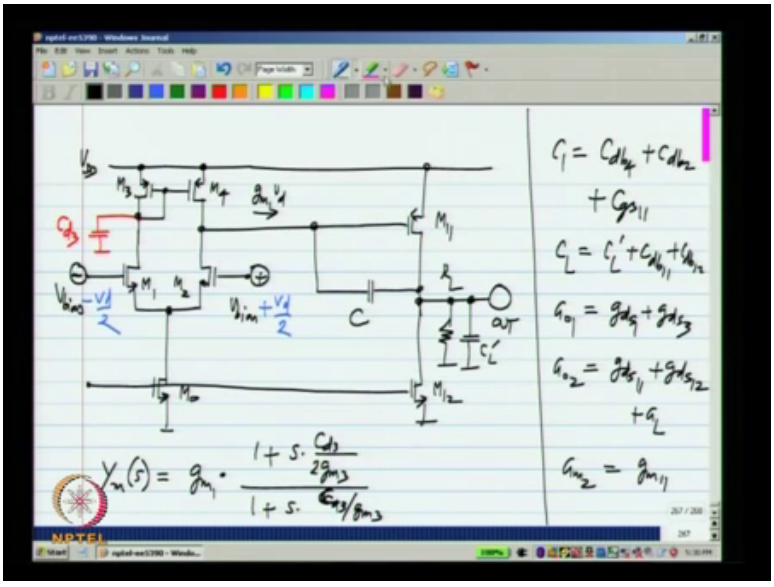

So, first of all what is C 1? C 1 is the total capacitance or the output of the first stage and that consists of parasitic capacitances from every transistor that connected. There are M 4 M 2 and M 11, as usual I will neglect the values of Cgds, because the transistors are

operating in saturation region, so C 1 will be Cdb 4 plus Cdb 2 plus Cgs 11 ok. So that is what we have this one, that one and that one. Remember VDD is small signal ground.

Similarly what is CL ok, the total CL will be whatever load capacitance we connect CL prime plus the parasitic capacitances due to M 11 and M 12. So, we do not usually calculate all these exact values by hand, we resort to the simulator, but we need to know how each of those values influences the total capacitance or the total parameter, and which consequently effects the pole value. Now what is Go 1? Go 1 is the output resistance of the first stage and that will be equal to gds 1 plus gds 3.

This again we have evaluated and Go 2; that is the total conductance at the output of the second stage will be gds 11, which is due to this transistor M 11 and gds 12 due to the current source transistor M 12. Whenever you bias something with the current source, a current source contributes an incremental resistance which appears in parallel ok.

Now, if you have a load resistance RL to easily get the results, we simply absorbed that into the total conductance at the output of a second stage ok, the value of C the integrating capacitors known for everything is known, and also the trans admittance of the first stage, it is nothing, but the DC transconductance of the first stage times 1 plus SCd 3 by 2 Gm 3 divided by 1 plus S Cd 3 by Gm 3, as we found out while discussing the single stage opamp.

There is a parasitic capacitance Cd 3, here contributed by m 1 m 3 and m 4 and because that is on only half through the current we get a pole under 0. So, the total transfer function will consist of not this Gm 1, but Ym 1 which as a pole under 0 and the 2 poles here and the 0 over there ok. So, all we have to do is to substitute the terms and find out what each of these things is.

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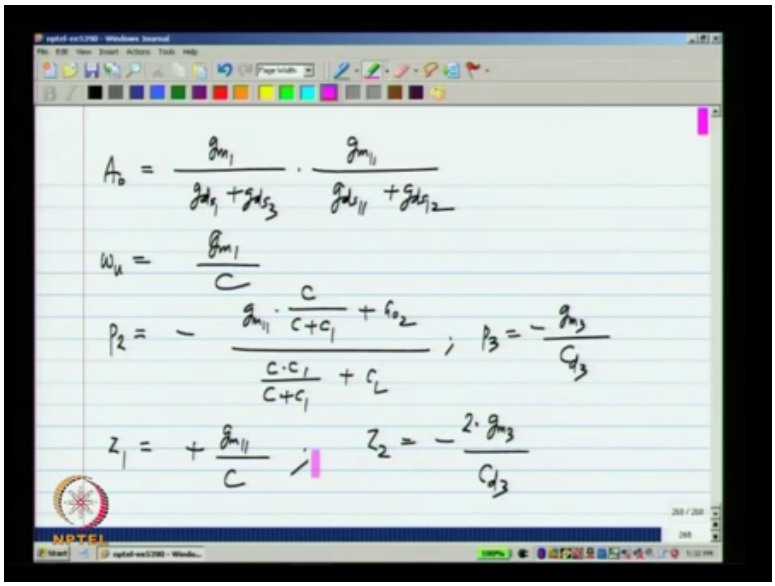

The DC gain is the product of the DC gains of the two stages which is Gm 1 by gds 1 plus gds 3 times gm 11. Remember gm 11 is gm 2 ok, I will write that down as well, gm 2 is nothing, but gm 11 the transconductance of this stage gm 11 by gds 11 plus gds 12 and the unity gain frequency should be gm 1 by C ok. This is what we have calculated and we will place the non dominant poles and zeros beyond the unity gain frequency.

Now the non dominant pole that we have calculated is minus gm 11 C by C plus C 1 C 1 value can be substituted from the expression over here ok, plus the total output conductance Go 2, whatever that is usually that is negligible C is combination of C and C 1 plus the total CL, this is one of the non dominant poles. In addition to this we also have the non dominant pole due to the first stage which is gm 3 by Cd 3 ok.

Of course, its in the left half plane and there is a right half plane 0, that we are quite familiar with from our earlier analysis and that is at gm 11 by C. There is also a left half plane 0 due to the first stage which is at minus 2 times gm 3 by Cd 3 ok. So, overall we have a dominant pole which is very close to the origin of and we have these non dominant poles and zeros, we have two a non dominant poles and two non dominant zeros ok, and we should position this, so that our phase margin is a healthy value of, let us say 40 degrees or 60 degrees or whatever we desire.

Now a couple of things, first of all these expressions are general and any external load that you have either load resistance or load capacitance can be absorbed in to these things

ok. All you have to do is to manipulate the value of CL or Go 2. Now what happens to the DC gain, why is this better for a resistive load compared to the single stage opamps. When we have resistive load, it is only the DC gain of the second stage that is affected ok, the first stage gain is not affected.

Now, we can offer to have a low gain in the second stage, because we have two stages of gain, let us say the second stage is designed for a modest gain of only 10 or even 5 and we get the bulk of our gain from their first stage. So, this way, even with a very heavy resistive load we can get a high DC is gain without increasing the trans conductance significantly. What I mean is.

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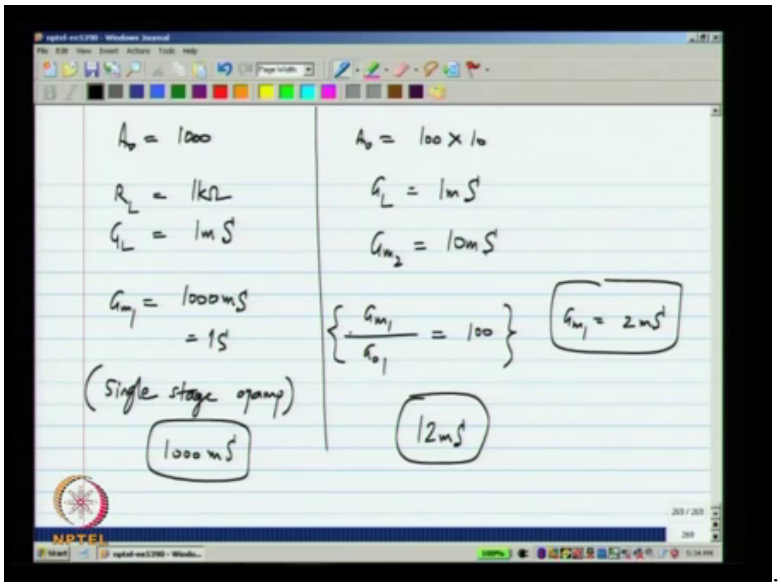

Let us say I want a DC gain of thousand ok. Now let us say my load resistance is 1 kilo ohm or equivalently the load conductance is 1 milli siemens. If I tried this with the single stage opamp, the transconductance would have to be thousand millisiemens or 1 seimen ok, this is with a single stage opamp. Now let us say we partition this into the 100 from the first stage and 10 from the second stage. So, again we have the same RL and GL which is 1 millisiemens.

Since the second stage has to offer a gain of only 10 by Gm 2, can be 10 millisiemens and my Gm 1 can be any value that I want, because I have to adjust the value of Gm 1 by Go 1 which is independent of the load to be equal to 100 ok. I do not know what Gm 1 is

going to be apart from stability considerations. I know that Gm 1 has to be significantly less than Gm 2, so let us say I will say Gm 1 is 2 millisiemens

So, clearly in this case we have to realize a total transconductance of 12 millisiemens and here the total is 1000 millisiemens. Now of course, how much power we burn to realize a given trans conductance depends on the topology, but just from the basics of mass transistors we know that if you want to a larger Gm, you have to have larger transistors operating at higher currents ok. So, to get 1000 millisiemens you have to burn significantly higher power turn to get 12 milli Siemens.

So, it is not possible to drive resistive loads and have high gains with the single stage opamp. Whereas, it is quite easily possible with a two stage opamp; that is the reason two stage opamps are very popular and very widely used. Now, these summarize the small signal DC and AC performance of the opamp and we have a higher DC gain and we have a number of parasitic poles.

And you know what to do with them? We have to place them sufficiently beyond the unity loop gain frequency of whatever feedback loop we operate that. Now, let us evaluate some other relevant parameters of this opamp; like the noise of sets slew rates on the swing.

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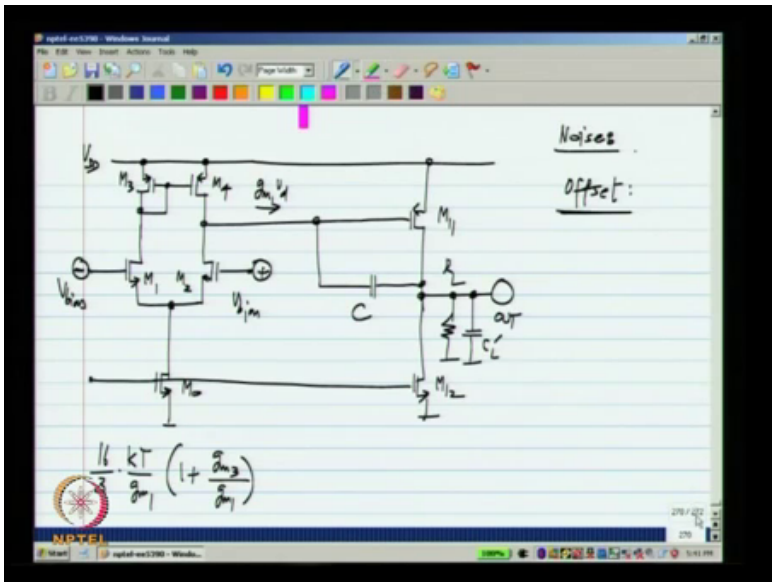

Now, first let us consider the noise. We know that the input referred noise of the single stage opamp alone is 16 by 3 kT by gm 1, where gm 1 refers to M 1 and M 2 1 plus gm 3 by gm 1. Now, let us say we have a two stage structure.

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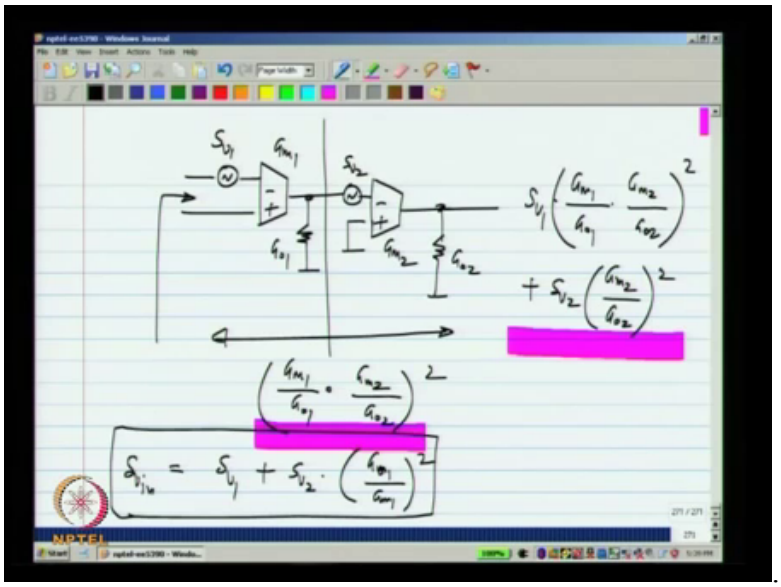

We already know the input referred noise of the first stage; let me call it as V 1 and this is Gm 1 Go 1. One thing I will do is, I will also ignore all the capacitors while calculating the input noise spectral density, so it will be valid only for low frequencies, but that is ok, that serves usually good enough estimate of the noise, so let us say this is a Gm 2.

Now, I do not have to recalculate the noise from the first stage, so what I will do is, I will calculate the effect of the second stage, either on its inputs or on its output ok. So, let us say I evaluate the second stage noise refer to its input and as I mentioned I will remove the capacitor C. What happens? I will have some Sv 2 ok. So, that is some voltage noises added over there.

So, what will be the total input referred noise, it is a quite easy to see so, one way to do that is to simply calculate the total output noise; first from Sv 1 we have a gain of Gm 1 by Go 1 times Gm 2 by Go 2 and this is a spectral density, so the total spectral density at the output due to Sv 1 will be Gm 1 by Go 1 Gm 2 by Go 2 square, and due to this Sv 2 the input referred noise of the second stage, we will have Sv 2 times Gm 2 by Go 2

square, and the overall gain we know is, Gm 1 by Go 1 times Gm 2 by Go 2 whole square.

So, if I want to represent this effect of both these noise sources with the single input source here, what I have to do, is to divide this by that one, so I will have Sv 1 adding directly, that is what we expect S v 1 simply adds to the input plus Sv 2 Go 1 by Gm 1 square. As I said many times when you have a cascade of multiple stages, the input referred noise will be the input referred noise of the first stage plus the input referred noise of the second stage divided by a square of the gain of the first stage input referred noise of the third stage divided by square of the product of first and second stage gains and so on.

And if these games are significant then only the contributions from the first stage will be significant, all others will be insignificant and that is apparent from this expression as well, because we have Sv 2 times Go 1 by Go 1 whole square, which means that Sv 2 is attenuated by a large factor 1, it is referred to the input Go 1 by Gm 1 is nothing, but the inverse of the DC gain of the first stage, which could be 50 or 100 or something so effectively, when we calculate the input referred noise all that matters is the noise of the transconductance Gm 1 ok.

The input referred noise of the two stage opamp will be exactly the same as the input referred noise of the, a simple single stage differential pair opamp ok. Any extra contributions from the second stage will be quite negligible.

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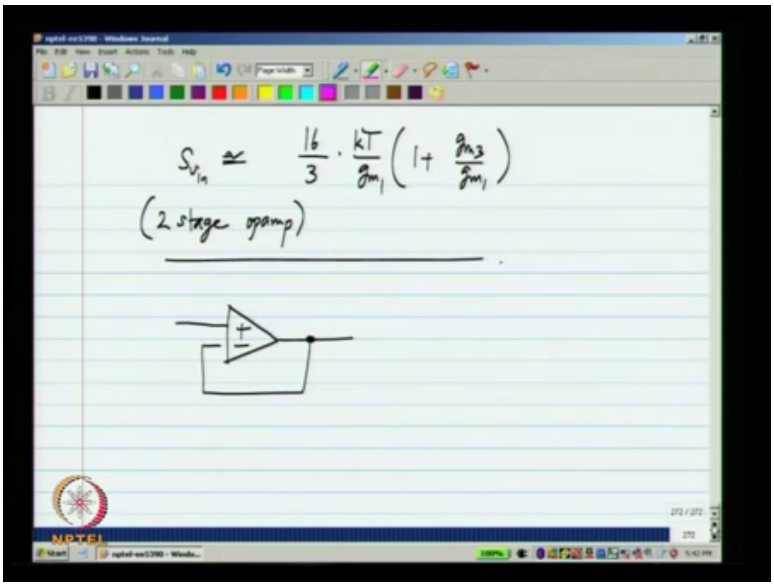

Now, the next thing we will consider is the input referred offset. Now what do we mean by the offset here. Let us take the example of a unity gain follower for instance. Now if I apply an input, the output should the exactly follow the input, but because of the offset there will be a difference between the input and output, so that is the offset.

Now we have already calculated the offset of the first stage right. Now just as with noise any mismatch contribution from the second stage will be divided by the gain of the first stage and will not matter when refer to the input.

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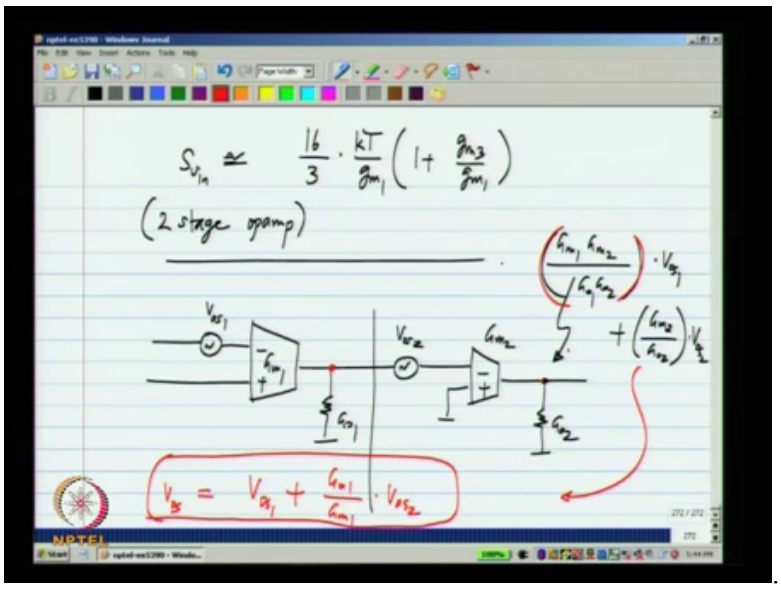

Again let me consider the two stage structure Gm 1, let us say I have some Vos 1 and we have Go 1 over here and I have Vos 2 offset is by definition DC and I do not have to include any capacitors in the calculation, I have Gm 2 and Go 2. So, Vos 2 is the input referred offset of the second stage, Vos 1 is the input referred offset of the first stage, so the total offset at the output will be Gm 1 Gm 2 by Go 1 Go 2 times Vos 1 plus Gm 2 by Go 2 times Vos 2.

Now, when we have refer this to a single offset source of the input we divide this by the overall gain which is this number, so Vos at the input would be Vos 1, because it is from the first stage, it adds directly plus Go 1 by Gm 1 times Vos 2 ok, just as with noise Vos 2 is divided by the gain of the first stage. So, when we compute the input referred offset the contribution of the second stage will be quite negligible ok.

So, again the offset of this, is the same as the offset of the single stage opamp ok, with the differential pair, that is the random offset of the two stage miller, compensated opamp is the same as the random offset of the first stage differential pair, which is of course, determined by the differential pair transistor and the load transistors.

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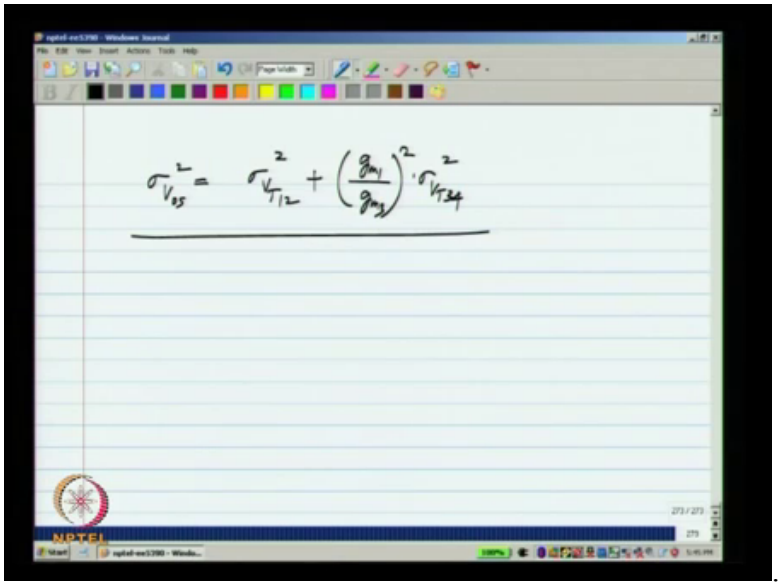

To the random offset variance will be sigma Vd 1 2 square plus gm 1 by gm 3 square times sigma Vd 3 4 square.

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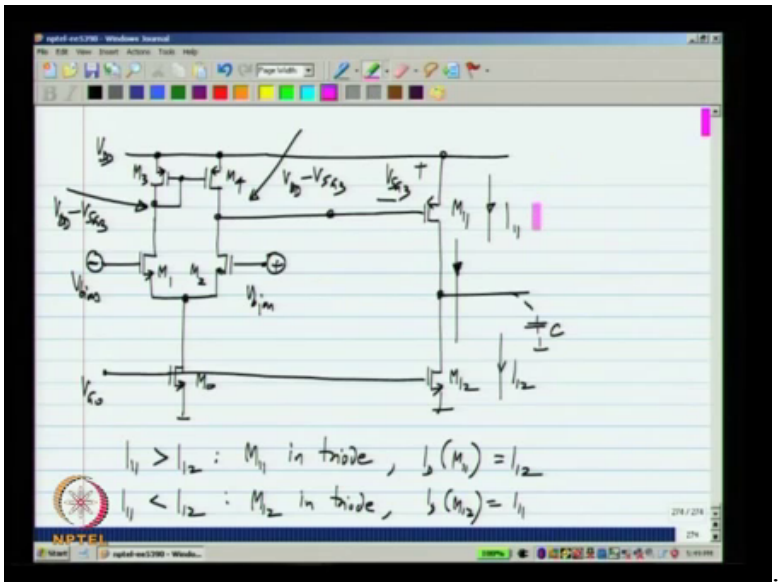

Now, in case of the single stage opamp; that is we are considering only this part, the operating point here was the same as the operating point there in absence of offset ; that is when the inputs are at V bias that drain of M 4 and M 3 are at the same voltage by symmetry, and because of the offset it will be different and the input referred offset can be calculated purely on the basis of random mismatch.

Now, in case of their two stage opamp let me just not show the load explicitly, but it can be there. What will be this value when the inputs are at V bias and there is perfect symmetry between two halves of the differential pair. Now this voltage and that voltage will be the same as each other by symmetry.

So, this is VDD minus VSG 3 and that is VDD minus VSG 3 as well, and let me call this voltage Vg 0 at a, the voltage Vg 0 M 12 tends to carry a current I 12 if it is in saturation region ok. This pair lost of volts only in saturation region and this current I 12 will be carried if it is in saturation region.

Now, if you look at this, we have M 11 which behaves like a current source and M 12 which behaves like a current source connected together ok. Obviously, the current in M 11 has to be equal to the current M M 12. Now can both of these be in saturation, it is possible if the voltage happens to be bias in the middle. Now what will be the current that M 11 carries if it happens to be saturation region. So, to imagine this, perhaps first of all we are discussing DC situation.

So, we can neglect the capacitor. So, let us say I connect the drain of M 12 to VDD and M 11 to ground ok. In this case these transistors will be guaranteed to be in saturation, and I have some current I 12 here, which is the intended bias current for a second stage. Now let us say with a gate voltage VDD minus VSG 3 or source gate voltage of VSG 3 M 11 carries some current I 11. Now what happens if we connect these two together, the current has to be the same ok, it does not matter what the M 1 tended to carry, if it was in saturation and M 12 tended to carry.

If it was in saturation when you connect them together like this, they have to be the same. If I 11 is greater than I 12; that is saturation current of M 11 is more than the saturation current of M 12. What happens is, let us say this voltage start from the somewhere in the middle. So, that board transistors are in saturation region, a net current of I 11 minus I 12 will flow into the parasitic capacitance that is at the output.

So, this voltage will keep on rising and finally, M 11 will reach the triode region and the current in M 11 will reduce to be equal to I 1 2. Similarly if I 11 happens to be less than I 12, the voltage will fall down and till M 12 is triode and id of M 12 equals I 11 ok. Now this is visualize very easily graphically.

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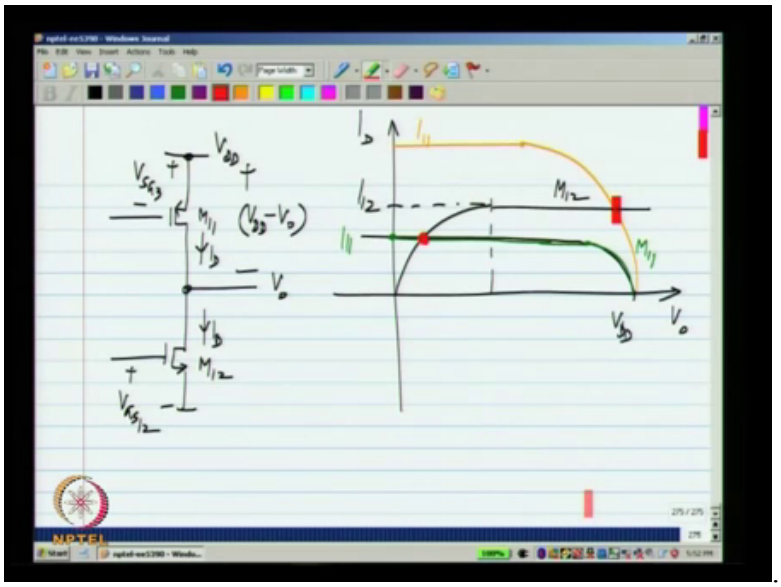

This operates with the certain VSG 3 and this operates with the certain VGS 12; ok and let us say the output voltage is V out. I will draw the id Vds characteristics. Let us say that is ID if I draw the id Vds characteristics of M 12, what I will get is, the usual output

characteristics of the MOS transistor, let me show it with the very small output conductance, this is Vo, Vo is nothing, but the Vds of M 12.

Now I will also draw ID versus Vo characteristics, I know that the VSD of M 11 is VDD minus V naught. So, ID versus Vo characteristic is nothing, but ID versus VSD characteristics, but with the curve flipped around at VDD. You would have done this calculation when you are calculating the characteristics of for instance A C MOS inverter. So, this is VDD VDD minus V naught is the VSD of that and that will look something like that.

So, this is what I call I 12, the saturation current of M 12. This is for M 12 and I can show this in a different colour and this is for M 11 and that is I 11. Now what will be the value of V naught, it will be the point of intersection. We can clearly see that if I 11 is smaller than I 12 then M 12 will go into the triode region. Similarly if M 1 ones characteristics happened to be something like that; that is I 11 happens to be more than I 12, then M 11 Go in to triode region.

So, one of these two will be in triode region, if I 11 is not equal to I 12. Now, let us connect this in feedback and then see what happens. Let us say you connect this in unity feedback ok. Now, here we are talking about the case where there is no mismatch between transistors.

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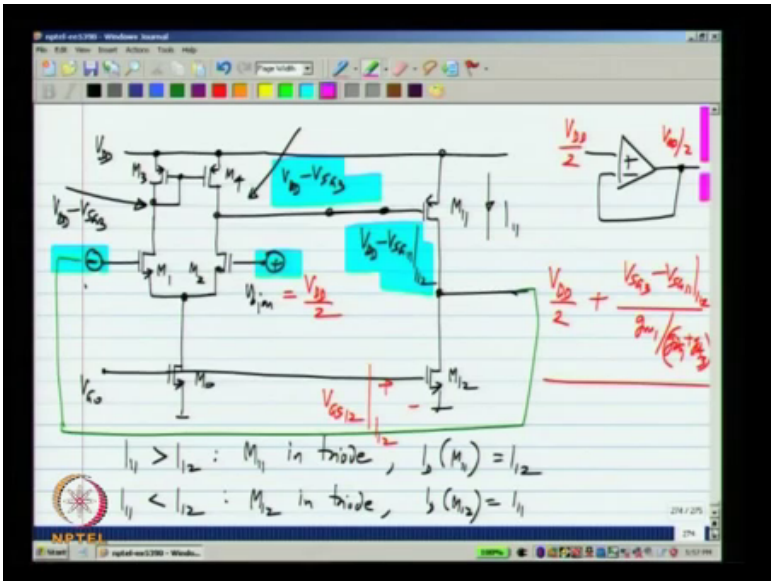

Let me connected up in unity feedback like that and apply V bias to that stage, and let us say V biases somewhere in the middle of the supply ok, let us say VDD by 2. Now what do we expect is the opamp is ideal, if this is VDD by 2 I would expect VDD by 2 over there ok. Now clearly the currents in M 11 and M 12 have to be equal to each other ok, that is just from Kirchhoff Law here. And also if this is around VDD by 2 and this is VDD board transistors will be in saturation region ok, you imagine large VDD. So, the Vds of M 11 and M 12 were very large.

So, they will be in saturation region. Now if their two transistors are in saturation region and their currents are equal, the voltage here will be VGS 12; that is required for current of I 12 ok, and the voltage here will be VSG 3; that is required for a current of I 12. Now we know that in the balance condition, the differential pair by itself would give you VDD by minus VSG 3. The voltage required at the gate of M 11 would be VDD minus VSG 11 for a current of I 12, whatever that is ok.

We say that the two currents are same of course, and they are both in saturation region. Now the differential pair will tend to given output of VDD minus VSG 3 when it is balanced. Let us say this VDD minus VSG 3 is not equal to VDD minus VSG 11 required for a current I 12. So, what happens when we connect these two together, the output of the first stage has to move from its natural value of VDD minus VSG 3 to the gate voltage required for M 11, to carry a current of I 12.

So, what I am saying here is, that the first stage differential pair would naturally carry some current, but it has to change from there different values, which will make that transistor M 11 carry a current of I 12. Now how will that happen? The only way for that to happen, is for the differential pair to have a non 0 input voltage ok, because if the input was 0, the output would be VDD minus VSG 3. So, this of course, means that there is a difference between this one and that one.

So, the output will not be at VDD by 2, but it V at VDD by 2 plus some delta V, and what will be the delta V, it will be the change required at the output of the first stage which is VSG 3 minus VSG 11 for a current of I 12 divided by the gain of that stage, which is Gm 1 by gds 1 plus gds 3. Please go through the reasoning carefully. What I am saying here is, that the first stage has some natural output voltage, when you connected up in a feedback loop with a second stage; the first stage output has to change.

So, that the second stage carries a current of I 12, which is what the supplied by the current source of the second stage ok. And because it has to change the input voltage of differential pair has to change, which means that there is an offset. Now this offset is not, because of random is mismatch between the transistors. This is because output voltage of first stage is not equal to the input voltage required by the second stage to carry a current of I 12 ok, and this is known as a systematic offset and the way to avoid this is quite obvious.

If we made VSG 3 equal to be VSG 11 for a current of I 12, then the first stage output does not have to change, when you are connected to the second stage and connected in feedback loop. So, it will make sure that there is no systematic offset VSG 3 for a connect of I naught by 2 is not equal to VSG 11 for a connect of I 12 ok.

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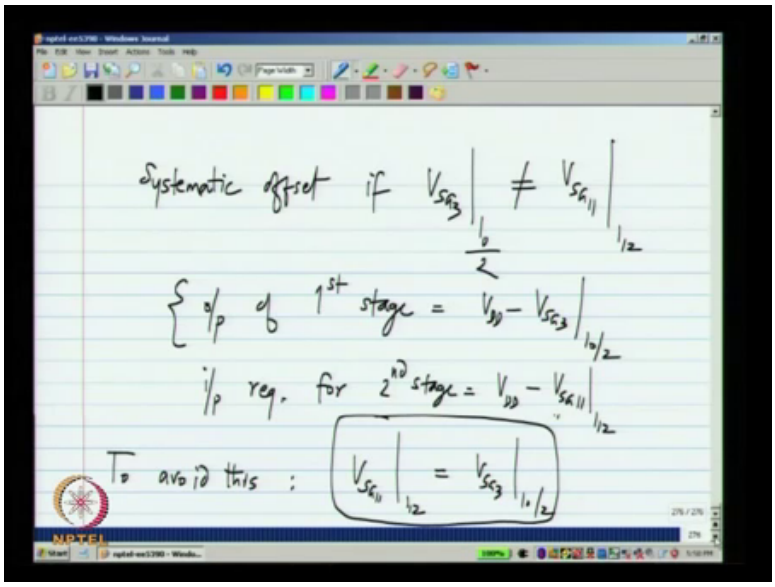

This is because output of first stage is VDD minus VSG 3 for a current I naught by 2, and the input required for the second stage VDD minus VSG 11, the current of I 12, and to avoid this you make deliberately VSG 11 for current of I 12 equal to VSG 3 for a current of I naught by 2 ok. Now, can we do this, we can certainly do that, because M 11 and M 3 M 4 are all PMOS transistors.

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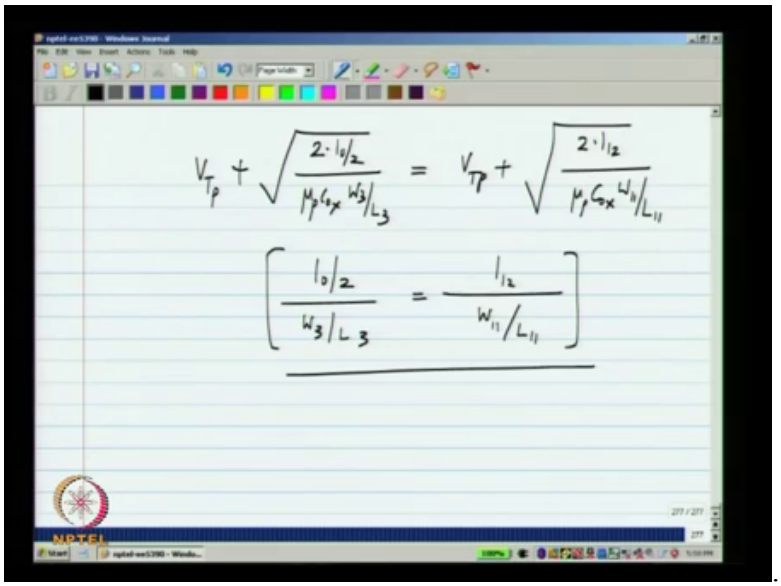

What we have to make sure is that VT, both have the same VT VT plus square root 2 times I naught by 2 divided by mu P Cox W 3 by L, 3 should be equal to VTp plus square root 2 times I 12 divided by mu P C ox W 11 by L 11 ok, what this means is; of course, I naught by 2 divided by W 3 by L 3 equals I 12 divided by W 11 by L 11 ok. This is usually refer to as the transistors M 3 and M 4, transistor M 11 operating at identical current densities ok, if you make lengths equal the width ratio will be equal to the current ratio between the transistor M 11, and the transistors M 3 and M 4.

Now this is done to avoid systematic offset, if you do not do this there will be a systematic offset which is equal to the difference in the VSGs divided by the gain of the first stage, it turns out that this is not always possible to do. Sometimes it is not easy to arrange this.

So, in cases where the gain of the first stage is very very large, the a systematic offset will be very small anyway and you do not have to do this, if the gain of the first stage is modest and you are looking for very small offsets, you go on and make the current densities of the transistor M 11; that is the second stage transistor equal to the transistors M 3 and M 4, and you will not have any systematic offset.

The offset will be governed only by random mismatch of the transistors in the first stage. So, what we have done is to take the two stage opamp and the realize it at the transistor level, it is quite convenient. You take the single stage opamp and follow it up with the

common source amplifier loaded by the current source; a very easy to calculate the small signal parameters and noise and offset and so on. Noise and offset I will contribute primarily by the first stage and systematic offset will be eliminated by equalizing the current densities. In the next lecture we will calculate the slew rate to swing limit etcetera of this opamp and compare it to the other opamp, so that we have discussed earlier

Thank you.