Analog Integrated Circuit Design
Prof. Nagendra Krishnapura
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 15
Two and three stage miller compensated opamps; Feedforward compensated opamp

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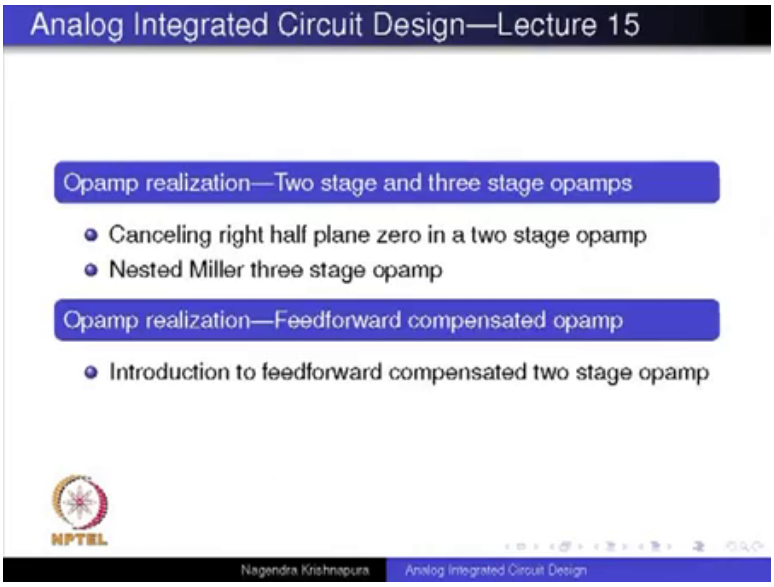

Hello and welcome to the 15th lecture of Analog Integrated Circuit Design. In the previous lecture, we discussed the Two stage opamp in great detail. So, where the poles and zeros were and tried to adjust the components. So, that we get the sufficient phase margin when the opamp is placed in feedback ok.

Now, do not worry about exactly what feedback loop the opamp is placed in; we assume that it is placed in a unity feedback configuration and then, go with the calculations. In reality, what you have to do is to find the value of k that is the feedback factor that you are trying to use in the actual circuit and then, do your loop gain calculations based on that one ok.

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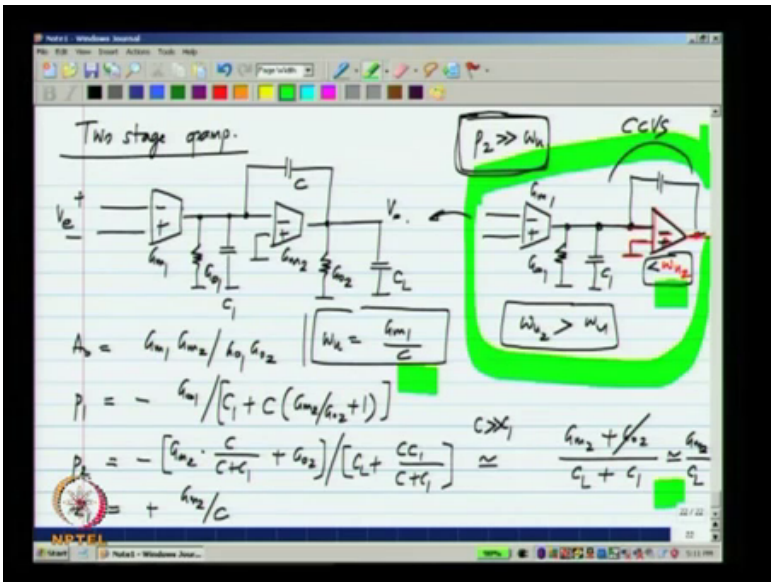

Just a quick recap. This is our Two stage opamp; the first stage Gm 1, has an output resistance Ro 1 or an output conductance Go 1 and there is a capacitance C 1 here which can be due to various sources. And the second stage, has a trans conductance Gm 2, an output conductance Go 2 and a total capacitance of C 1 which can be due to trans conductance itself and any load that is applied to the opamp and there is a capacitance C which is around the second stage. And this is the integrating capacitor that is the current from Gm 1 is supposed to pass through this and give the integrating function with a unity gain frequency of Gm 1 divided by C.

And we also evaluated the expression for poles and zeros and all that stuff of this one. The dc gain is the product of the 2 dc gains, the low frequency pole is at minus Go 1 that is this conductance divided by the total capacitance which is C 1 and miller multiplied C ok.

And the second pole P 2 is at total conductance is Go 2, but more predominantly the effect of Gm to in feedback and here, we have total capacitance which is C l plus C and C 1 in series ok. And the 0 is in the right half plane at Gm 2 divided by C ok. We also saw that the second pole can be further approximated by this is when C is much more than C 1 Gm 2 plus Go 2 divided by C l plus C 1 ok.

Now, Gm 2 is expected to be much more than Go 2. So, we can neglect this as well and usually C well also many times happens to be much more than Go 1. So, this can even be

further many times approximated by Gm 2 by C l ok. Now, what is a stability criterion after all? The unity gain frequency of this is of course, Gm 1 divided by C. As stability criterion says that the 0 and the pole has to be sufficiently beyond the unity loop gain frequency which is the same as the unity gain frequency of the opamp for a unity gain amplifier.

Now, the phase lag contributed by the 0 is simply a function of the ratio of Gm 2 by Gm 1 and that has to be maintained sufficiently high. So, that the phase lag is small. The phase lag due to the pole will be something and we would like P 2 to be much more than omega u ok.

Now, what does this mean? Remember, this opamp was derived from a structure like this ok. We wanted the output current of Gm 1 to go through a capacitance C and we found that the best way was to implement a current controlled voltage source ok. And this current controlled voltage source is implemented using a some op amp shown here in red and let us say it has a certain frequency omega u 2. We also know that if you take an opamp for the unity gain frequency omega u and you make a feedback circuit with it.

Then, the feedback functionality will be until a frequency of the unity loop gain frequency ok. Below the unity loop gain frequency, the feedback loop functions as it is supposed to. Above the unity loop gain frequency the loop gain becomes very small and clearly the feedback loop does not function as desired.

Now, what does it mean? The unity loop gain frequency of the second feedback loop turns out to be omega u 2 itself. So, omega u 2 has to be sufficiently larger than the frequencies of interest. Now, what is the frequency of interest? You can consider omega u itself to be the frequency of interest. What? By this what I mean is we are trying to make an opamp with a frequency with a unity gain frequency of omega u ok. That is this entire circuit should behave like an integrative up to a frequency of omega u. Now, the integrator itself is made by placing a capacitor around the second opamp. So, that we form a current controlled voltage source.

Now, this will behave like a current controlled voltage source only below a certain frequency omega u 2 which is the unity gain frequency of the second opamp. Now clearly the unity gain frequency of the second op amp has to be more than the unity gain frequency that we want to realize ok. This is not the case; then, clearly the entire circuit

does not behave like an integrator at all ok. So, the integrator has to behave like an integrator that is have 20 dB per decade roll off at least up to the unity gain frequency of the integrator ok. So, this is what we would guess just by looking at this sort of system block diagram.

Now, what is omega u 2? It is the unity gain frequency of the second opamp and it is Gm 2 by C l ok. Clearly then, Gm 2 by C l has to be much more than the unity gain frequency we are trying to realize which is Gm 1 by C ok. So, that is this frequency here must be much more than Gm 1 by C and that is exactly what this condition is saying also. This P 2 has to be much more than omega u.

The second pole P 2 appears because the opamp with which we made the current controlled voltage source itself has a finite unity gain frequency. If the unity gain frequency of this the second opamp was infinite. Then, we would not have the second pole and we would just have a single pole opamp ok. Is this clear? So, this gives you another intuitive way of figuring out why these conditions come about. It is extremely important when you get algebraic results to are that some intuition to it ok.

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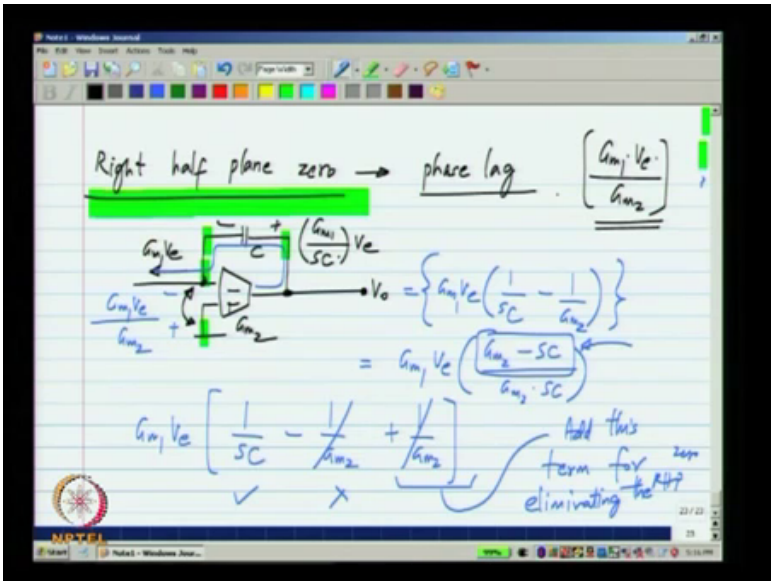

Now, the Right half plane zero, this causes phase lag.

Now, this is an annoying problem as well because of this the phase margin is deteriorated. Now if we did not have the right half plane zero, we would have the phase

lag only due to the poles and would have in a better situation ok. That is you have less phase lag because you do not have the right half plane zero. So, what we would like also is to investigate if there is a way of getting rid of the right half plane zero or maybe eliminating the effect of reducing the effect of the right half plane zer0 ok.

Now, in order to do this let us first figure out why the right half plane zero comes about. For this, I will focus only on the second stage of our opamp ok. We have a current Gm 1 Ve that is supplied by the first transconductor and that is passed through this current controlled voltage source which behaves as an integrator ok. Now, what I will do is I will neglect all the other components because I want to focus only on the right half plane zero and not worry about other details.

Now, what happens if we do this? This Gm 1 Ve will pass through the capacitor and it causes a voltage drop Gm 1 by SC times Ve and this is exactly the voltage that we want. But this is not the voltage that appears as Vo because that is equal to the voltage across the capacitor plus the voltage between this point and ground ok. And this will have a voltage. Now I have assumed that there is no load or anything like that.

So, this Gm 1 Ve this current process through the capacitor and has to come out of the transconductor. If it has to come out of the transconductor across this, there must be a voltage which is equal to the current through the transconductor divided by the transconductance value which is Gm 2 ok. So, the total voltage V naught equals Gm 1 Ve 1 over SC minus Gm 2 sorry minus 1 over Gm 2.

Now, this is what results in the right half plane zero. This is exactly the term we saw in the numerator earlier also and that is what gives you the right half plane zero and we want to get rid of this one. Now by looking at the expression for Vo, we can guess what we must do. To get rid of this the expression for Vo is the input current to the second stage which is Gm 1 Ve times 1 over SC which is the desired term minus 1 over Gm 2 which is the undesired term ok.

If we had only the first term here we would have an integrator of unity gain frequency Gm 1 by SC right. So, what can we do to get rid of this? We have to add plus 1 over Gm 2 in some way or the other. So, we have to add this term for eliminating the right half plane zero ok; if we do that then, this simply cancels with that and we will be left with only the integrate.

Now, how do we add that? So that means, depth to the output voltage that we originally have, we need to add a voltage equal to Gm 1 Ve divided by Gm 2 ok. That is the input current divided by Gm 2. As a very simple way of doing this.

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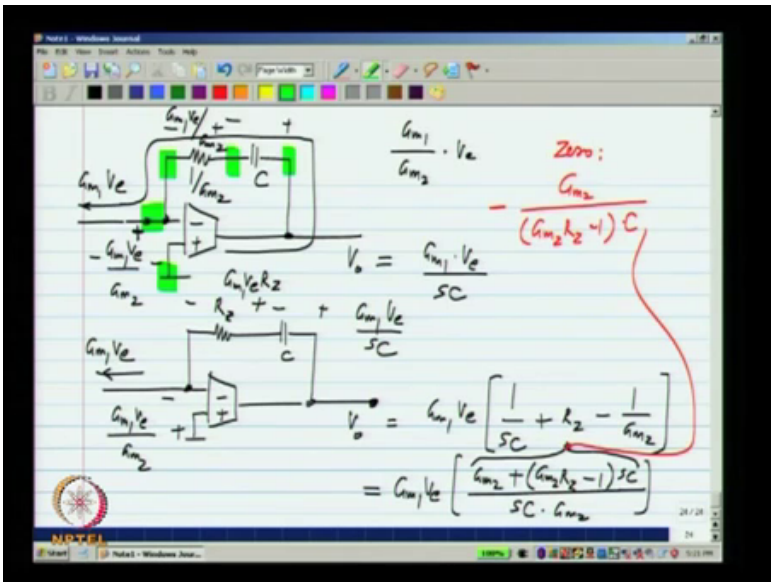

That is the voltage that is developed there, this is Gm 1 Ve and this branch the capacitor also carries a current Gm 1 Ve ok. So, I want the voltage to be the voltage across the capacitor plus this plus an extra term which is Gm 1 by Gm 2 times Ve. It is very easy to see that if I insert a resistor here which is equal to 1 over Gm 2, what will happen? Across this resistor I will have Gm 1 Ve by Gm 2 ok. So, now, if I sum these 3 voltages, the voltage across here plus the voltage between these 2 plus the voltage there, I will get V naught and V naught happens to be just equal to Gm 1 times Ve by SC ok.

This is fine. So, by placing a resistance in series with the capacitor, we can eliminate the right half plane zero and the value of the resistance has to be 1 over Gm 2 ok. Now, if the value of the resistance changes from 1 over Gm 2, what will happen is you will get some not an exact translation of the 0, but something else that we can also see.

So, let us assume that again the same circuit and I will call this Rz ok. The voltage at the input of the transconductor is Gm 1 Ve by Gm 2. The voltage across this is Gm 1 Ve Rz and the voltage across that is Gm 1 Ve by SC. So, the total output voltage is Gm 1 Ve times 1 over SC plus Rz minus 1 over Gm 2 ok. So, we will get Gm 1 Ve that and ok.

So, I will write this as Gm 2 Rz minus 1 times SC. So, the numerator there is a 0 and the 0 is that Gm 2 divided by Gm 2 Rz minus 1 times C and the negative of electron. So, this expression makes sense because first of all, when Rz is 0 that is the old case we have a right half plane zero at Gm 2 by C; when Rz is exactly equal to 1 over Gm 2 the 0 moves to infinity and when Rz is more than 1 over Gm 2 will have a left half plane zero ok.

So, in fact, you can move the 0 to the left half plane and the advantage of a left half plane zero is that it offers a phase lead instead of a phase lag which enhances stability ok. But, we cannot play this game very much; we will see soon why? But at least we see that we can move the 0 to infinity or otherwise manipulate the position of the 0 ok.

Now, this particular structure is very simple. I have eliminated C 1 C CL on the other side etcetera, etcetera. But the principle works in exactly the same way ok. We will see that soon. The principle of 0 cancellation works in exactly the same way and is also widely used ok.

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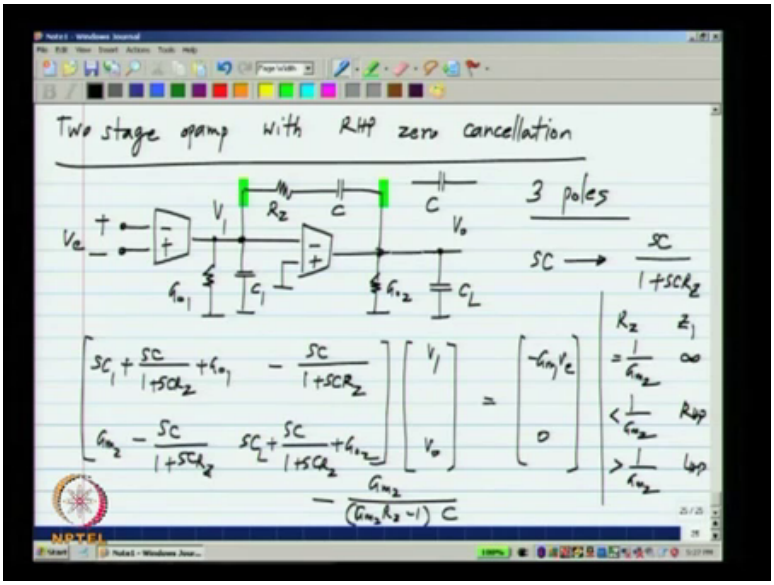

So, here then is the topology of the Two stage opamp with a right half plane zero cancellation. Now, the transfer function of this can be evaluated in exactly the same way as before by writing the node equations and before we do that we should again see, what is the number of poles and zeros we have? Ok. What do you think? Is it exactly the same as before? One difference from earlier case is that earlier also we had 3 capacitors, but the 3 capacitors were in a loop.

So, the sum of voltages of 2 capacitors was equal to the voltage on the other capacitor. So, we could only set 2 of them independently and the third-one was automatically fixed. Now, because we have this Rz in series with C, we can set all three of them independently. So, this really has three poles ok.

Now, this again is something that keeps happening in design that you should be aware of; whenever you try to fix some problem some other problem may come up. It may or may not be severe, but did something to be investigated. Here, what would we try to do? We tried to eliminate the right half plane zero because it was causing phase lag. We got some technique and then, when we finally, put it in the opamp we see that we may not have a right half plane zero, but we will have an extra pole, which also causes phase lag.

So, you have to evaluate it more thoroughly to see that the phase lag caused by the extra pole is not ruining the advantage you got by eliminating the 0 ok. Now I will not solve this completely, but I will outline the method. So, again we can write the node equations and I will write it in terms of the same 2 node voltages as earlier. V 1 and Vo V equals the source current vector.

Now, all we have to do is earlier between these 2 terminals we had just C which gives you an admittance SC. So, in the admittance matrix now wherever we have SC we have to replace it by the admittance of this whole thing. Which what? Which is, 1 over the series combination of Rz and the capacitor; In other words, this is SC 1 plus SC Rz ok. This is an easy way to do it we could define this to an node and write node equations, but that necessarily makes things complicated.

So, the equations turn out to be that is the total admittance loading the first node total admittance loading the second node. It is like that and then, here we will have ok. And finally, there will have, the source vector remains the same here we have minus Gm 1 Ve and 0 and by taking the determinant you can find the solution, you will find that the 0 will be at what we determined earlier that is minus Gm 2 by Gm 2 Rz minus 1 times C ok.

So, if Rz equals 1 over Gm 2, the Z Z 1 is at infinity; if it is less than 1 over Gm 2, it is in the right half plane and if it is more than 1 over Gm 2, it will be in the left half plane.

Now, we will also have a third pole and again by using a similar approximation as before that is earlier about to solve the quadratic equations we took 2 terms at a time and turned it into 2 linear equations, exactly the same thing can be done for the third order equation that we have.

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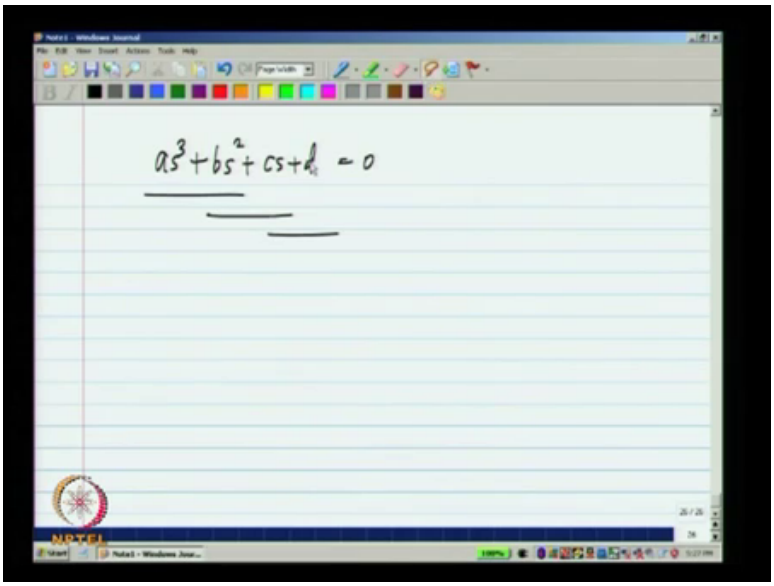

If you have as cube plus bs square plus cs plus d equals 0, you can take these two at a time equate that to 0; these two at a time equate that to 0 and these two at a time equate that to 0, you will get 3 linear equations and solution to this will be valid approximation to the actual solution only if the 3 poles are very far from each other. The magnitude of the 3 poles have to be very different from each other ok. If you do that you will find that the value of the first 2 poles are almost the same as before and you will also get a third pole.

Now, I will not do the algebra here, you can take it as an exercise and do it please make sure that you will you solve this completely by using the Cramer's rule or whatever your favourite method of solving the matrix equation is and then do the approximate solution of the third order equation and find out the poles. Now, I will just tell you an intuitive way of finding out the poles let me copy over this diagram.

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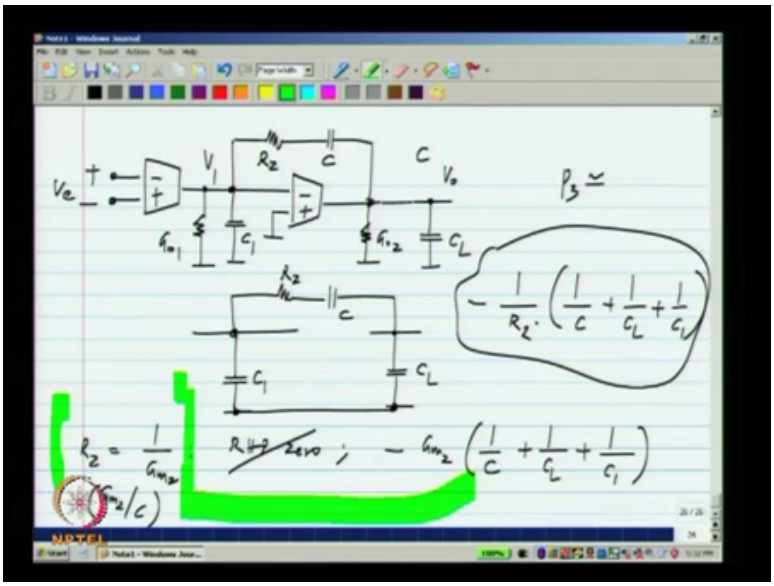

Now, the first pole will be associated with Go 1 and the total capacitance that we see. It will be almost the same as before. There may be some terms due to Rz, but they will not be dominant. Second one, will again be due to Go 2 and the capacitance associated with that and the third one, will be due to Rz and the capacitance is associated with that 1 ok. So, what do we have there? We will just have turns out Rz C CL and C 1 ok.

In a way, you have an R C circuit involving this Rz and these 3 capacitors in series because after all this is just ground and these two are together ok. So, the pole associated with this turns out to be minus 1 by Rz and the series combination of the 3 capacitors which is just 1 over C plus 1 over CL plus 1 over C 1 ok; that is approximate value of P 3 ok.

Now, if you do the third order equation and the approximations that I mentioned, you will get exactly this solution. Please verify that, please just do not take this for granted and also try to understand how I got this value here. Now, what did we have? What is the effect of putting Rz there? We can eliminate the right half plane zero and what we will end up with a pole ok.

The right half plane that we let us say we choose Rz to be exactly 1 over Gm 2 ok. Then, the right half plane zero it goes away. But, will have a new pole. What is that? It is given by that one, the pole is at minus Gm 2 because we chose Rz to be 1 over Gm 2 1 over C

plus 1 over CL plus 1 over C 1 and where was the right half plane zero that we eliminated? It was at Gm 2 by C ok.

Now, comparing these 2 you see that the pole that you introduced is at a higher frequency compared to the 0 that you eliminated. So, we are still safe. The 0 that you eliminated removed some phase lag the pole that you introduced introduces some phase lag, but because the pole you introduced is at a higher frequency it introduces less phase lag ok.

Now, that is why it is not a very wise thing to make Rz very large because you may think that oh by making Rz very large, I can move the pole into the left half plane and then even produce phase lead. But, what happens is you will also have this additional pole which will cause external phase lag and you will have a complete washout and the extreme cases when let us say Rz is infinity then you will not have this capacitor here at all. You will have these poles very close to each other earlier we saw that when this branch was not there, when C was not there.

There was some pole frequency here and something else there and when you introduced C they moved further apart which is good for stability. Now if you make a Rz equal to infinity, that is very large then you will go to the original case where the poles are relatively close to each other which is very bad for stability ok. So, it is not a wise thing to make R C very large. It is to make it try and cancel the RHP be 0.

Now, later you will also see that you cannot make component values exactly, you will not be able to make 2 unlike components have a relationship like this Rz equal to 1 over Gm 2. So, even if you nominally make it like this, it will vary in one or the other direction. But it is still a good thing because it reduces the total phase lag that you would have got ok. So, it is a good technique, but do not try to overdo it that is the message.

So, that summarizes the Two stage opamp. It has a dc gain equal to the dc gain of the 2 stages and when you have resistive loads you can optimize the dc gain of the first stage and let the second stage have a modest gain; this you could not do with the single stage opamp. The single stage had to provide all the gain. With the 2 stages you also get this additional complication of extra poles and zeros, but it is possible to design the values. So, that you have a stable opamp ok.

Now, let us revisit how we got the Two stage opamp. First of all, let me start with the simplest opamp that I had.

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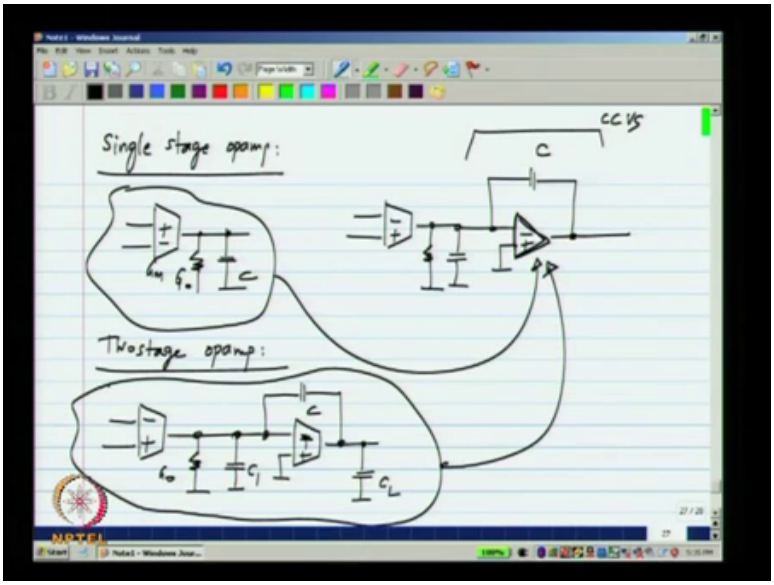

Which is just that one ok; Let me just name them or there be like this. Now, the Two stage, opamp what do I do? I try to make it better by using a current controlled voltage source instead. I wanted this to be an ideal opamp, but clearly that is not possible.

This is the current controlled voltage source and I used my single state opamp in place of that opamp and I ended up with the topology which was the Two stage opamp which of course, is that by substituting a single stage opamp in place of this one which realizes the current controlled voltage source, I got the Two stage opamp. And I also showed that the Two stage opamp is better than the single stage opamp because it offers higher dc gain and so on.

Now, I can play this game further right. I know that if this were an ideal opamp, I would get the ideal integration from there to there. But of course, I do not have an ideal opamp, but instead of using a single stage opamp which is inferior, I could try and use the Two stage opamp over there ok.

So, that may give me better results right because after all Two stage opamp is better than the single stage opamp. Using a Two stage opamp here has to give me better results than

using a single stage opamp. So, that is what I will do here. I will redraw it with this opamp being a Two stage opamp ok.

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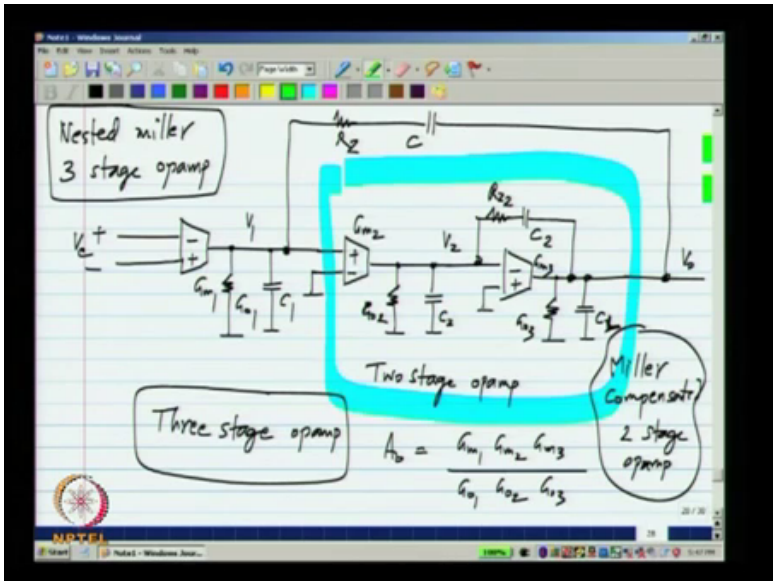

So, first let me draw there Two stage opamp. I will call this Go 2 in C 2 and Go 3 in C 3 ok. I will have let me call this C 2. Now this forms my Two stage opamp and have plus here and minus here because that is the sense I want to implement the current controlled voltage source. Now this is my current controlled voltage source that is this part of the circuit and I drive it with what I had earlier, I will call this Gm 1.

It could have an output conductance Go 1 and there will also be a capacitance C 1 over there ok. Sorry this is not grounded. This is the input to the opamp Ve ok. So, all I did was I know that a trans conductance driving a current controlled voltage source gives me a good opamp and how do I make the current controlled voltage source, I made it with the best opamp I have now which is the Two stage opamp.

Now, this entire thing will give me the Three stage opamp ok. In fact, we can go further, in practice it is not done although you can have a four or five stages right and get better and better results. What is better about it? First of all the reason we went to multiple stages in the opamp is to get higher dc gain, the dc gain that you could get from the first single stage opamp was not good enough.

What is the dc gain of this stage? If I open circuit all capacitors, I open all of these things well simply have Gm 1 Go 1 Gm 2 Go 2 let me label these things Gm 2 Go 2 and this is Gm 3 and Go 3 all of them in cascade. So, the dc gain will be the product of the dc gains of the 3 stages ok. So, this clearly is better than what we could get with a Two stage opamp because there we had only product of Two stages.

So, let us say each stage has potentially has a maximum gain of 50; then, with a single phase opamp you can get a gain of 50; The Two stage opamp, 2500 and with a Three stage opamp, 12500. So, that is what is advantageous about the three stage opamp. Now of course, you can write the node equations for this there are 3 independent state variables in this case ok.

I will call it Vo V 2 and V 1 and you can write it down and analyse it and such an analysis is necessary for the complete design, but the expressions will be so complicated that we will not have any insight from them ok. So, I will only intuitively derive some conditions. First of all the unity gain frequency of the opamp that I am trying to realize is Gm 1 by C ok.

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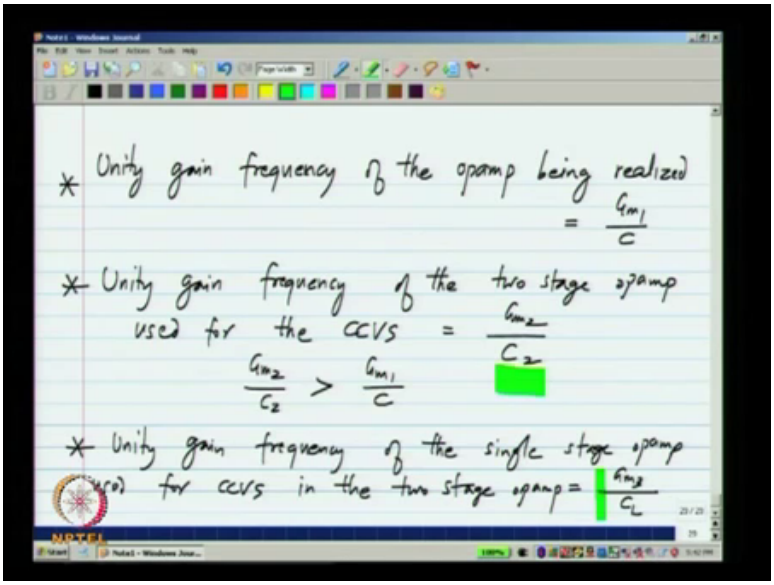

Now, the unit again frequency of the Two stage opamp, used for the Current Controlled Voltage Source is Gm 2 by C 2 sorry I had used uppercase Gm is here this is Gm 1 by C and Gm 2 by C 2. Now clearly the current controlled voltage source has to function as a current controlled voltage source over a frequency range beyond Gm 1 by C ok, only

then we will get this integrating action that is a transfer function of Gm 1 by C from the input to the output.

So, this clearly means that Gm 2 by C 2 has to be greater than Gm 1 by C. And this Two stage opamp itself is made using a current controlled voltage source. So, I think I called this CL earlier, let me go back to the terminology CL consists of any capacitance here plus external load that is applied. So, the unity gain frequency of the single stage opamp used for the current controlled voltage source in the Two stage opamp equals Gm three by CL ok.

And this clearly has to be more than that one. So, that the Two stage opamp itself works properly. In fact, for the Two stage opamp, we did a rigorous analysis found the second pole and this is the approximate value that we got ok. This is the value that we got. Here, I am only going through the intuitive stuff. In fact, if you evaluate the expressions you will see the exact condition.

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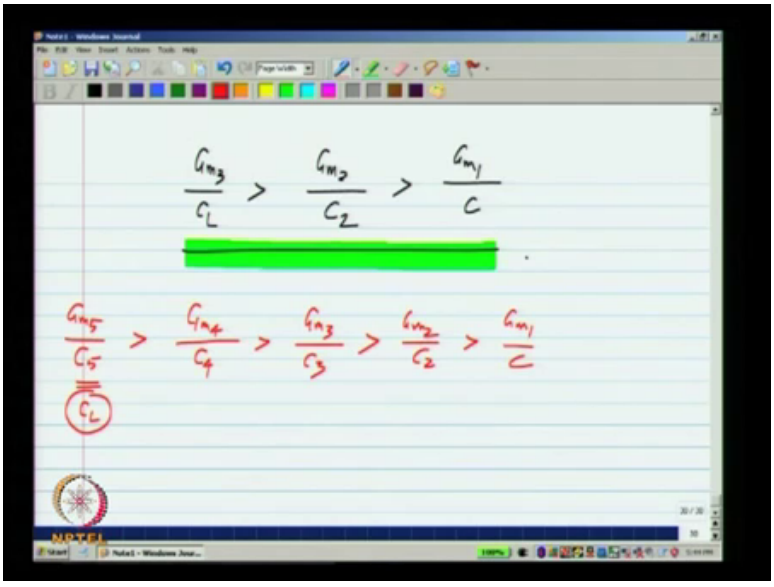

But what this finally, says is the innermost opamp should have a unity gain frequency that is more than the unity gain frequency of the inner opamp which has to be more than the unity gain frequency that you are trying to realize.

So, this also points to some constraints like I said this is only an approximate description because now the transfer function of this can be quite complicated, you will have a third

order denominator and also allowed to zeros because of these parallel paths through the capacitors and so on. It is not very easy to figure out where those zeros are ok. Intuitively, you can do it analytically and then, do it quite easily.

But, intuitively, this condition has to be satisfied. the unity gain frequency of the innermost opamp has to be more than that of the one outside it and which has to be more than that of the one outside it ok. And if you have more stages let us say you go to Five stage opamp; then, you also need to have the inner most which is I will call Gm 5 by C 5 which has to be more than let me write it separately. Gm 5 by C 5 has to be more than Gm 4 by C 4. It has to be more than Gm 3 by C 3 Gm 2 by C 2 and Gm 1 by C and C 5 is nothing but the total load CL ok.

Now this condition also points your to some general constraint that is as you make opamps with more and more stages you can only realize lower and lower unity gain frequencies because typically there is an upper limit to Gm by C ratios that you can realize because what happens is even if you do not have an external load the trans conductor itself will have some capacitances and the ratio of Gm 2 its own inherent capacitance, there is a limit in any given technology as you go to smaller and smaller CMOS processes, this limit goes on increasing, but there is always a limit.

Now, given that the highest one, let us say you place close to the limit that is possible that is the ratio of Gm 2 the inherent capacitances the highest that is implemented. Then, you have to maintain all these things to be successively smaller. So that means, that the highest unity gain frequency you can make a Two stage opamp with is higher than highest unity gain frequency you can obtain for a Five stage opamp ok. So, that is also the reason why you do not go crazy with the number of stages.

Although the higher number of stages will give you a more dc gain, you only use the required number ok. So, 3 is practical maybe 4 and 5 are done, but not so often used and higher than that at least I am no seeing. So, that is how you design multiple stage opamps and because by the by this kind of a Two stage opamp which has the C 2 and we earlier described C 2 as being multi miller multiplied and loading the first stage is known as a Miller compensated opamp. The Two stage opamp that we discussed is a miller compensated Two stage opamp.

Now, you see that first of all the inside the opamp, inside has a miller compensation the outside one also has a miller like compensation. So, this entire thing is called the Nested miller 3 stage opamp. There are many variants of this to enhance stability and so on. We will not discuss any of those things and just like we inserted a resistance in series with this to eliminate the 0, we can also try inserting resistances in series with that and this as well in various combinations.

All of the results of this has to be obtained from more complicated analysis and simulation. I will not discuss those things except to say that that can be done and there are lots of variants of this because now you have more poles and zeros. There are also more ways of trying to get rid of them you can see the papers in the journal solid state circuits or transactions on circuits and systems for details of those things and one thing I want to summarize here is that you can make multiple stage opamps when you need higher and higher dc gains.

Let us say you want a dc gain of close to a 10000 or a million. It is not possible to do with you in 2 stages you may have to go to 3 or 4 or 5 stages ok. It is possible, but stability becomes a bigger concern because of more poles and you are maximum realized unity gain frequency reduces ok. We started with the single stage opamp and we tried to make it better by passing the output current of the transconductor through a current controlled voltage source instead of directly through a capacitor and that gave us the family of opamps that was better and the single stage opamp.

Now, there is an alternative idea which also we can use that is this way traces back to the original discussion or negative feedback circuits that gives a entirely different kind of opamps which also are of interest in many cases ok. First of all let me consider the non-inverting amplifier that we designed long back ok. This is the input to the opamp, that is the output and that is the input to the amplifier.

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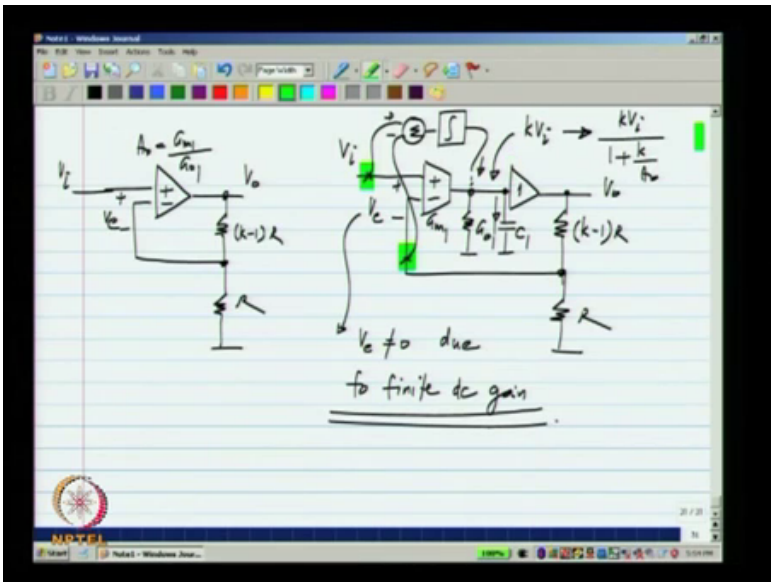

Now, let me place a single stage opamp here and this could have an output resistance Go 1 Gm 1 that is a ok. I will use a buffer to isolate these things just for simplicity, but they will still be a dc gain limitation because of Go 1 itself ok. This is Vo and because of this finite dc gain even if you have a constant voltage V is not 0 ok.

So, what happens is to support a certain output voltage, you need to have a certain voltage across Go 1 which means that there has to be some current flowing through it and to have some current flowing through it, you need to have some voltage across this one, that is the problem. So, in steady state let us assume a constant input there will be a difference between those 2 points when you implement this. So, this is the same as this particular amplifier with a dc gain of Gm 1 by Go 1.

Now, let us go back to the basic idea of negative feedback. What did we say it had to happen? Basically in order to control some value to a desired value we compared the desired and actual values and then, drive the output based on that one ok. That was the basic idea.

Now, we know that this voltage which should have been k V I will settle to a value which is less than that which is k V I by 1 plus k by a naught ok. Now the actual voltage is smaller than this one and we can increase that by pushing more current into Go 1 ok. If we somehow manage to push more current into Go 1, we will make this voltage larger and consequently the error is smaller.

Now, what is the desired outcome in a negative feedback system? The feedback quantity here must be exactly equal to that quantity there. In fact, with an ideal opamp that was happening right; if you had an integrator without a finite dc again this is what was happening ok. There should be a capacitor here C 1 that is what was going to happen.

What we can do is this is the actual value we can compare it to the desired value and based on that control the current that is flowing there using an integrator. So, what we will do is we will take that, we will take that compute the error between the 2 ok. Now, if V I is more than this value; that means, that there has to be more current flowing into Go in from top to bottom. So, what we will do is we will have an integrator and somehow make that push a current into Go that is the idea.

So, in other words just to summarize again this feedback loop settles with a steady state ever between these 2 points ok, when we use this kind of an opamp. So, what we will do is we measure the error between these 2 points after it is settled let us say and then, we integrate that error further and inject the current into this output conductance.

So, once the current through the output conductance increases this voltage goes up; this also goes up and the error will become smaller. It can even become 0, if this integrator is ideal right. It is very clear, if this goes on integrating when the input is non 0 the only way to reach steady state is when these 2 inputs are equal to each other or the input to the integrator is 0 ok.

Now, this gives a different class of opamps known as Feed forward opamps which we will discuss in the next class. Now, one other thing that we can guess right away is that we are assuming that the original circuit reaches steady state and based on that steady state error we are doing the integration.

But the integration itself is a continuous operation. What this really means is that the second integration that we have here is much slower than the first one ok. It almost looks as though the first one reach a steady state and based on the steady state value, we inject some current here ok. In reality what will happen is the original one is though going through it is integration and this is going through in.

It is integration all simultaneously it, I just that this integration has to happen slowly enough. So, that it appears as though the first one, the original loop has reached steady

state and you are measuring the steady state error based on that injecting your current into G naught ok. We will see the details of that in the next class.