

Analog Integrated Circuit Design
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Lecture - 13
Two stage miller compensated opamp- 1

Hello and welcome back this is lecture 13 of Analog Integrated Circuit Design. In the previous class, we looked at simple realization of an opamp at the level of the control sources. We realized reducing voltage control current source loaded by a capacitor. We also saw that the output resistance of the voltage controlled current source limits the dc gain and this consequently results in steady state error. So, even after a long time the output does not reach exactly the desired value, but will be a little bit away depending on the amount of dc loop gain ok.

So, the dc loop gain has to be higher than a certain value and this requires us to have different opamp topologies which can possibly realize higher and higher dc gains. In this lecture we will look at one such opamp which will perform better than the one that we saw in the previous class.

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The slide contains a circuit diagram and mathematical derivations. The circuit shows a first stage with a transconductance g_m and a load capacitor C . The output of this stage is connected to a second stage through a buffer. The input of the first stage is V_e and the output is V_o . The buffer is labeled "Buffer" and has a gain of 1. The output of the buffer is V_o . The input of the buffer is V_o . The output of the first stage is V_o . The input of the first stage is V_e . The output of the first stage is V_o . The input of the first stage is V_e . The output of the first stage is V_o .

Mathematical derivations on the slide:

$$\omega_n = \frac{g_m}{C}$$

$$\frac{V_o}{V_e} = \frac{g_m / sC}{sC + g_m} = \frac{g_m}{sC + g_m}$$

$$= \frac{g_m R_o}{sC R_o + 1} = \frac{1}{sC/g_m + 1/g_m}$$

Annotations on the slide include: "* Buffers can be inconvenient to implement" and "* Limitations on how high $g_m R_o$ can be".

The opamp that we had was a voltage controlled current source or a trans conductor, loaded by a capacitor and to isolate the external load, we can use a buffer, But, it turns out that Buffers are not very easy to implement in CMOS technology. So, they can be

implemented, but they bring with them their own limitations, we would like to avoid them.

So, most of the time; opamps are used without explicit buffers in CMOS processes. This is the input voltage and a current $G_m V_e$ is pushed out of it. So, the voltage here will be G_m by SC times V_e ; where, this is the capacitor C . So, the unity gain frequency of this opamp ω_u equals G_m by C ok.

Now, even if the buffer isolates the external load, the trans conductor as an output resistance R_{out} or an output conductance G_{out} which are reciprocals of each other. Now this is an inherent property of a voltage controlled current source. Just like a current source has an output resistance which is not infinite; a voltage controlled current source also has an output resistance which is not infinite.

So, because of this, the transfer function that we will get will be the output by input of the opamp should have been G_m by SC , but this is not what we will get we will get G_m by SC plus the output conductance.

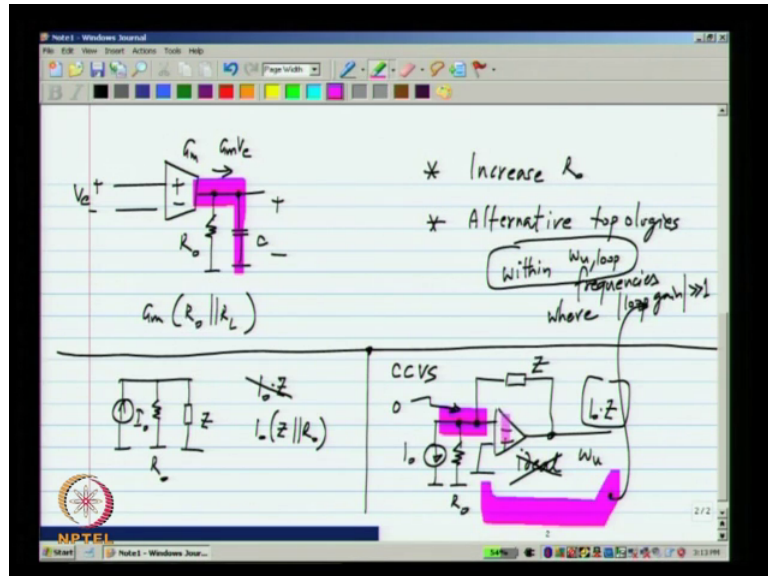
This can be written in various forms; we can write it as $G_m R_{out}$ divided by $SC R_{out} + 1$ which makes the dc gain explicit at dc or low frequencies, we have again equal to $G_m R_{out}$ and the pole which was at the origin, in this transfer function has moved to a frequency minus 1 over $C R_{out}$ ok. It can also be written in alternative form as 1 by SC by G_m plus 1 by $G_m R_{out}$. Let me write it on the side.

Now, in this case, this is the ideal part that we would like to implement. Additionally, we have a small non ideal number here, 1 over $G_m R_{out}$. So, the higher the value of R_{out} , the higher the dc gain $G_m R_{out}$ and the smaller will be this non ideality ok. But in general you will never be able to make this infinite. So, we will have to live with some finite value of $G_m R_{out}$.

And in fact, depending on the topology that we choose, the value of $G_m R_{out}$ may be limited to some modest value like 50 or 100 or so ok; whereas, sometimes we would like to have opamps with the gains of for 10000 or even a million. So, there are limitations on how high $G_m R_{out}$ can be ok.

Now, this depends on the topology. So, depending on the topology we could have either 25 or 250, but there will always be some limitation.

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Additionally, what happens is that sometimes, let us imagine a case, where the opamp is used without a buffer and let us also assume that there is a resistive load R_L . Now, in this case the dc gain of this opamp will be $G_m R_o \parallel R_L$ and regardless of how high you make R_o you will always have R_L . So, the dc gain will be limited to G_m times R_L ok. So, this is another problem that sometimes when you have resistive loads the dc gain will be limited by that and we have to find ways of obtaining higher dc gains even with external loads ok.

So, basically there are 2 possibly, there are different possibilities of trying to increase dc gain. First is increase R_o that is we do something to the transconductor. So, that it is internal resistance is increased. Now, this clearly does not help when we have an external resistive load R_L and we may have to use alternative topologies ok. So, during the initial analysis we will still assume that there is no external load we will derive the topology and then, show that even with external resistive load these things can work well ok.

Now, to investigate alternative topologies first we need to find out exactly why this topology results in limited dc gain. It is quite simple. Ideally we would have wanted all the current from this trans conductor G_m to flow into the capacitor C . Now, what

happens is when you have are not a part of it flows into it. So, that is why we get a finite dc gain, as supposed to when we had only a capacitor we would have infinite dc gain and we had an ideal integrator ok.

Now, essentially what we are doing here is converting the output current $G_m V_e$ of the transconductor into a voltage by passing it through a capacitor ok. Now if we find a different way of converting this current to a voltage G_m by SC without having some of the current going to some other component, we will make a better integrator ok. So, that is the problem.

Now, that is a well-known problem which also has a well-known solution. The problem basically is that let us say you had a current I_{naught} going into an impedance Z and the current source has some eternal output resistance R_{naught} , what happens is a part of this current will go into that ok.

So, the output voltage instead of being I_{naught} times the impedance Z will be I_{naught} times Z parallel R_{naught} and the way to get around it is not to simply try and pass the current through a load resistance by applying the load across the current source, but to make what is known as a current controlled voltage source and we have already seen the topology of a current controlled voltage source using an opamp.

And for now let us assume that the opamp itself is ideal I_{naught} and I connect the same impedance Z in feedback ok. And initially let me assume that the opamp is ideal. What does it mean? This voltage is 0 and the output voltage will be exactly equal to I_{naught} times Z assuming that opamp is operating in negative feedback.

Now, what happens if the current source is non-ideal and we have a resistance R_{naught} ? Because this voltage is 0, no current flows through the resistance and all of the current I_{naught} still flows through this impedance Z ok. So, even in presence of are not the output voltage will be I_{naught} times Z .

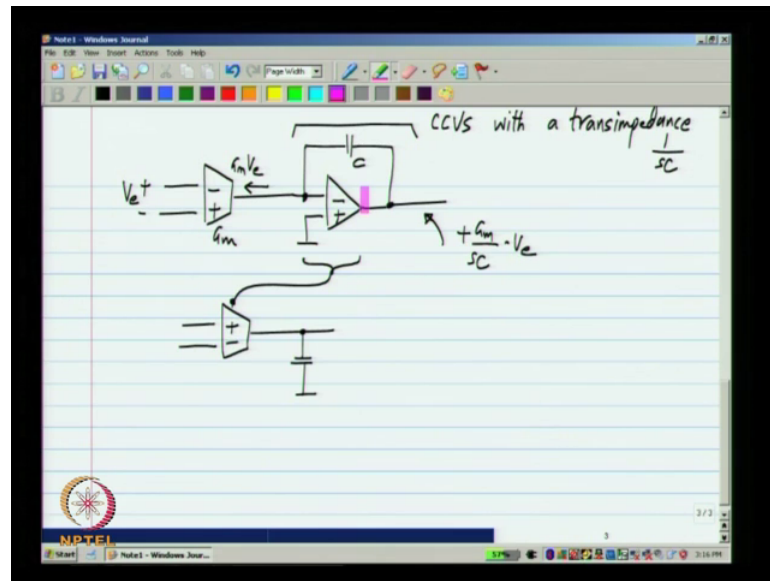
So, that is why when you want to convert a current to a voltage; it is better not to simply apply the impedance across the current source although that is possible. It is better to use a current controlled voltage source of the appropriate transe impedance value ok. You can clearly see that the problem at hand for us is also the same we have a current $G_m V_e$ which has to pass through a capacitive impedance.

Now, we were simply applied the capacitance to the output of the transconductor that is not what we should do we should try to make a current controlled voltage source whose input is the output current of the transconductor and whose output voltage will be the output of the opamp ok. We will see how to do that. Now, before we go there one more thing to keep in mind is that of course, we will not have an ideal opamp we will have a real opamp with some unity gain frequency ω_u ok.

Now, what is the range of frequencies over which this behaves like a current controlled voltage source; behaves like a current controlled voltage source over a range of frequencies where the loop gain magnitude is much more than 1. This we have seen earlier rather basically it is a range of frequencies within the unity loop gain frequency of this particular feedback loop ok. This is a very important point this opamp will be a real opamp and it has to be such that its unity gain frequency is higher than the frequency of interest.

Now, what is the frequency of interest for us? We would like this our opamp to behave like an integrator over a certain range of frequencies and the unity gain frequency with the opamp which is used to make the current controlled voltage source has to be much higher than the unity gain frequency of the opamp we are trying to realize that is G_m by C ok; we will see all of these things in more rigorous analysis later. But it is a good idea to get an intuitive feel for how things should be when we design them. So, how do I make my opamp?

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Simply loading the transconductor with a capacitor C ; I will not do this, I will pass it through a Current Control Voltage Source whose transimpedance is C with the transimpedance of 1 by sC .

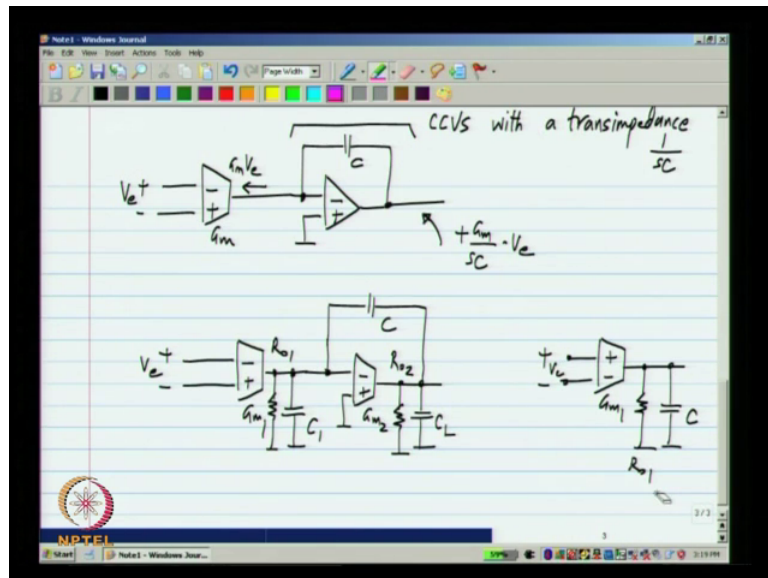
Now, with an ideal opamp, the voltage here will be 0 and the output voltage will be I have a current $G_m V$ here. So, the output voltage here will be minus G_m by sC times V ok. The sine inversion comes because simply because of the inversion through the second stage. So, to get rid of the inversion what I will do is I will invert the signs of the transconductor I will have minus plus.

So, that I have $G_m V$ flowing that way; it will flow in the same way through the capacitor and the output voltage will be plus G_m by sC times V ok. Obviously, this opamp will not be ideal because if we had an ideal opamp, we would try to just use it and not make another opamp with it ok. So, this will be some real opamp and we have to make sure that even with the real opamp all our assumptions hold ok.

Now, what is the opamp that we know? There is only 1 opamp that we know so far. And that is this particular opamp ok. So, this is the opamp that we used in the previous lecture, discussed in the previous lecture and this is the only opamp that we know. So, we will just use it in which place ok. So, please understand what is going on here. So, we want to make an opamp.

So, we will instead of loading the transconductor with a capacitor we will follow the transconductor using a current controlled voltage source. But to make the current controlled voltage source, we need some opamp. So, we will use the simplest opamp that we know which is; basically a transconductor which is loaded by a capacitor ok. So, if we do that what do we get?

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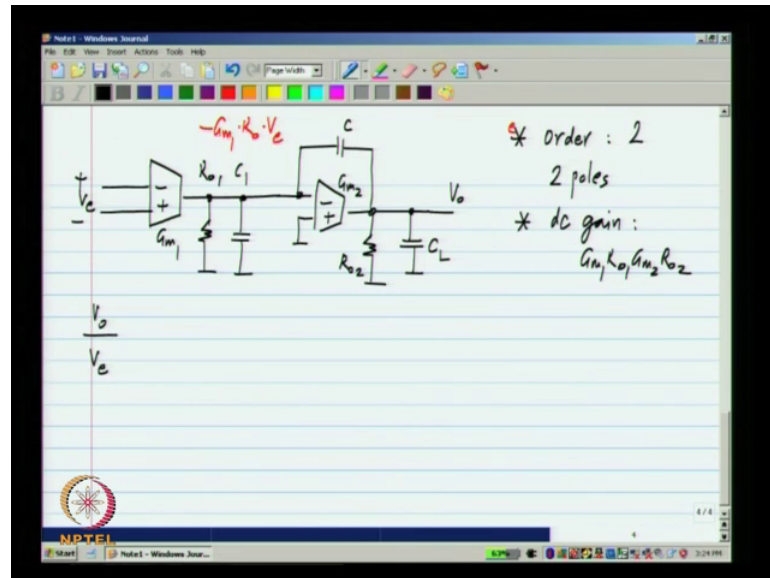
This is the opamp used to make the current controlled voltage source and I will call the CL. CL will be any capacitance that is loading the transconductor plus any external load that may be applied to the opamp ok. So, that will always be present. So, all of that is clubbed into a single capacitor CL.

Now, I have V_e here; I will call this $G_m 1$ and I will call this $G_m 2$ just to distinguish between them and also invariably between any node and ground there will be parasitic capacitance between the output of the first trans conductor and ground there will be some capacitance which I will call $C 1$ in analysis we need to include the effects of all of these things and finally, figure out what exactly happens. So, the reasoning so far has said that this opamp will be better than using just that one, that is $G_m 1$ loaded by a capacitor C ok.

So, that is the reasoning by which we derived all this and also let us put the limitations in place. These transconductance will have some output resistance like I said earlier; you cannot make a current source with an infinite output resistance. It can also not make a

transconductor or a voltage controlled current source with an infinite output resistance ok. So, this is the topology that we have to analyze and see if it is really better than what we started off with which is that one ok.

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I will redraw my opamp here ok. We need to do analysis of this and find out the ratio of output voltage to the input to the opamp V_e and that will be the transfer function of the opamp.

Now, before we go and do the full-fledged analysis, it is a good idea to look at the circuit and see what the transfer function might come out like ok. This will serve later as a sanity check for us. Now, what will be the order of this transfer function? How many poles will it have? The number of poles or the order is nothing but the number of independent state variables in the circuit and state variables are nothing but capacitor voltages and inductor currents.

Here of course, we do not have inductors. So, it is only capacitor voltages and we have 3 capacitors connected like this. So, there can be at most 3 state variables, but we also see that the voltage on C_1 plus the voltage on C equals the voltage on C_L ok. The 3 capacitors are connected in a loop which means that only 2 of them can be independently set. So, there are really only 2 independent variables. So that means, that this will be a second order transfer function; that means, there will be 2 poles.

Now, there can also be any number of zeros; that is a little harder to figure out we will see later how to look at the circuit and try to figure out the frequency of the zeros. But 1 guideline is that whenever you have 2 parallel paths from let say the output of the first stage to the final output, there is a path through $G_m 2$; there is also a path through the capacitor in general you can expect zeros in such a case and so, we will also expect that there will be a 0 here.

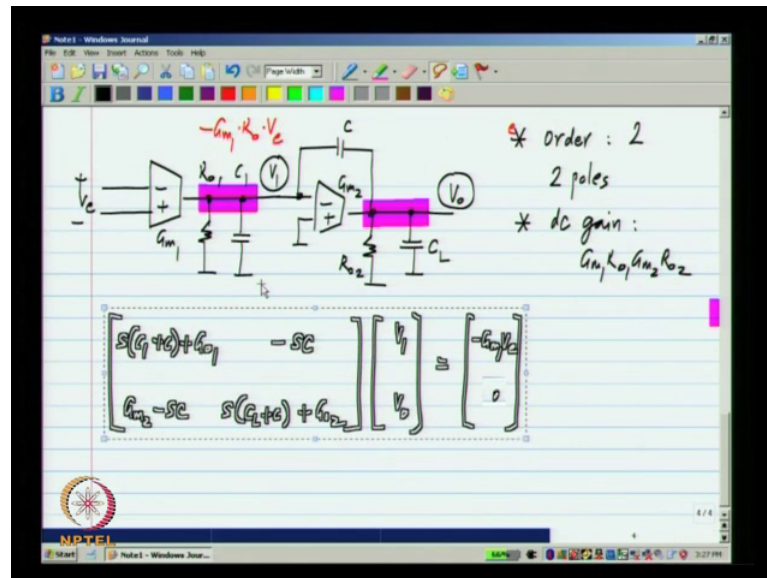
But this is a little more vague and it is also possible that you do not have a 0 or there may be zeros even without 2 parallel paths and so on. But that is some expectation that we have ok. And finally, what would be the dc gain of this? Again, when we find out the transfer function and set the value of S to 0 we should get the dc gain ok.

Now, we can also find the dc gain independently without doing the full blown analysis with Laplace transforms; if we do that then we can, after we do the analysis we can compare it to this value and see if it satisfies sanity check or not. And that is again extremely simple for dc all that happens is that all these capacitors are open circuited $C 1$ $C 2$ and $C L$. We have a current $G_m 1$ times V_e going into $R o 1$.

So, the voltage here will be $G_m 1 R o 1 V_e$ negative of that and that is applied to the second transconductor which provides a current $G_m 2$ times that voltage which flows into the output resistance $R o 2$. So, the output voltage will be plus $G_m 1 R o 1 G_m 2 R o 2$ times V_e . It is basically a product of the dc gain of the first stage and dc gain of the second stage. This is something that you would easily expect when you have a cascade of stages, you will have the product of dc gains to be the total dc gain and that is $G_m 1 R o 1 G_m 2 R o 2$ in this case ok.

So, now let us do the analysis.

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This circuit has 2 nodes and by writing k c l equations at these 2 nodes. They can find out where all the voltages and currents in the circuit first of all k c l at this node let me assign this node voltage to be some V_1 and this is of course, V_{naught} and I will write it in a matrix form; some admittance matrix times the vector of voltages $V_1 V_{naught}$ equals the vector of source currents that is currents flowing into these nodes. First of all the current flowing into this node containing V_1 is minus G_{m1} times V_{ok} .

This is provided by the first transconductor and the matrix entries can be filled up. This entry here is the total admittance which is sC_1 plus C plus G_{o1} ; G_{o1} is the reciprocal of R_{o1} . It is convenient to use the conductances directly instead of writing it as 1 over R_{o1} everywhere ok. And this term is minus sC ; basically the current through this capacitor is sC times V_1 minus V_o that is why we get plus sC here and minus sC ok. They should be familiar to you from basic circuit analysis.

Now, similarly the entry here is the total conductance at the node containing V_o . So, that is sC_1 plus C plus G_{o2} and the entry here is the current being drawn from this node due to the voltage on that node and that happens due to 2 components 1 is C and the other 1 is G_{m2} ok. It turns out that we will get G_{m2} minus sC here ok.

So, this is a system with 2 nodes and there are 2 equations and by solving for this we can find out the value of V_{naught} in terms of V_{ok} . And any number of ways to solve this you can invert the matrix and so on. But since we are only interested in the output

variable we will use crammers rule which says that the output voltage V naught will be equal to the determinant of this matrix. And the second column is replaced by the source vector divided by the dependent the determinant of the admittance matrix ok.

So, let me copy this over. So, as I said I need to copy this over again.

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$$V_p = \frac{\begin{vmatrix} s(c_1+c)+g_{o1} & -g_m V_e \\ g_{m2}-sC & 0 \end{vmatrix}}{\begin{vmatrix} s(c_1+c)+g_{o1} & -sC \\ g_{m2}-sC & s(c_L+c)+g_{o2} \end{vmatrix}}$$

$$= \frac{g_{m1} (g_{m2} - sC) \cdot V_e}{s^2(C_1 C + C C_L + C_L C_1 + g^x - g^x) + s(c(g_{m2} + g_2 + g_1) + C_L g_1 + C_1 g_2)}$$

So, as I said we notice nothing but the determinant with the second column replaced by the source current vector that is the determinant of that divided by the determinant of the admittance matrix ok. And this gives you, it is the determinant of what is on top on the numerator and the determinant of the denominator is nothing but will have a number of terms containing S square due to the product of this and that and also due to product of this sign not ok.

This much is due to the product of this one and that one minus I will have S square times C square ok. And in fact, this cancels with that one and will have a number of terms containing S that is due to product of this with this, product of this with that, the product of this with that one and the terms turn out to be ok. In addition to these there will be a constant and that is only due to this one and that one there. So, that will come out to be G_1, G_2 ok.

So, let me just rewrite it.

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$$V_o = \frac{g_{m1}(g_{m2} - sC)}{s^2(C_1C + CC_L + C_LC_1) + s(C(g_{m2} + h_{o2} + h_{o1}) + C_1h_{o2} + C_Lh_{o1}) + h_{o1}h_{o2}}$$

$$\frac{V_o}{V_e} \Big|_{s=0} = \frac{g_{m1}g_{m2}}{h_{o1}h_{o2}}; \quad 2 \text{ poles}; \quad 1 \text{ zero}$$

$$\text{zero } z_1 = + \frac{g_{m2}}{C}$$

And also I will take V_e to the left hand side. So, that I get the transfer function V_o by V_e . This will be equal to $G_{m1} G_{m2} - sC$ divided by the second order term $C_1 C C_L + C_L C_1$ plus the first order term which has plus the constant term. So, this is the transfer function of the opamp looks somewhat complicated, but it turns out that we can make intuitive sense of this transfer function as well.

But first of all though sanity checks, what did we say? The dc gain. What is the dc gain here? If I substitute s to be 0, this goes away and all these things go away. So, ok so, that is one thing and this is exactly the value that we got we said the dc gain was $G_{m1} R_{o1}$ times $G_{m2} R_{o2}$ and that is exactly what we have here except that it is written in terms of conductances that is all.

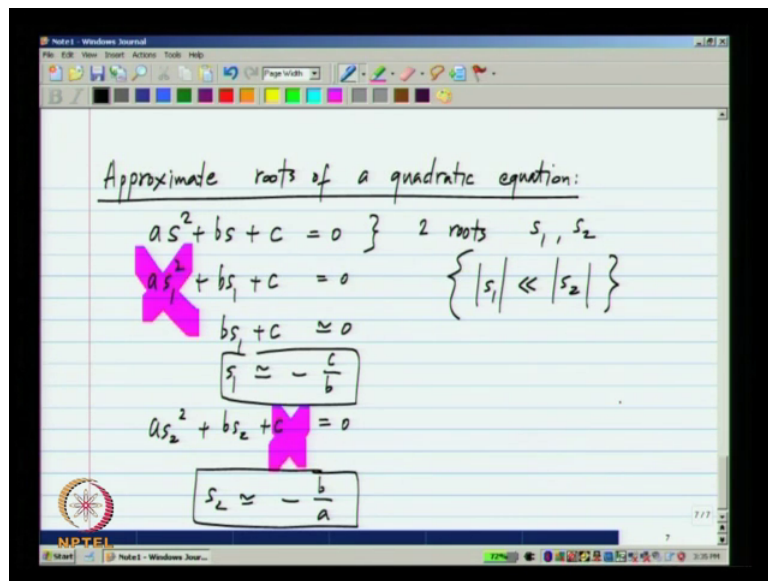
And also we said that it is a second order transfer function because there are only 2 independent state variables and that is the case also there are 2 poles and there is one 0 ok; we can see that in the numerator there is one 0 and this also we guessed because there were 2 different paths to the output; from the output of the first stage the output the second stage. There were 2 parts; one through the trans conductor G_{m2} , one through the capacitor C and generally when you have 2 parallel paths to the output with different phase shifts, different frequency dependences you will end up getting a 0 ok.

So, the next thing is to figure out where the poles and zeros are and then try to make sense out of them. So, first of all the 0 frequency is very easy. Where is the 0 here? It is

when the value of S for which this term becomes 0 and 0, I will denote it by Z 1 equals plus Gm 2 by C ok. I explicitly write the plus because zeros can be in the right half for left half plane and this happens to be in the right half plane ok. Now, the poles of course, can be obtained by solving this quadratic equation.

But the conventional solution to the quadratic equation the familiar one minus b by 2 plus minus square root of b squared minus four (Refer Time: 30:00) by 2 a that simply will not be able to do here because each of the coefficients a b and c are quite complicated. And if I even manage to write down that expression will not be able to make any meaning out of that ok. So, what we will do is we will find some approximate ways of solving the quadratic equation. It turns out that there is an easy approximation which also in this particular case yields intuitive results ok.

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So, it turns out that the quadratic equation of course, has 2 roots, but when the 2 roots are very far from each other that is when the magnitude of one of the roots is very small compare to the magnitude of the other root, the following approximation can be used ok.

Let us say we have a square plus bs plus c equals 0 and there are 2 roots s 1 and s 2 ok. So, this clearly means as 1 square plus bs 1 plus c is 0 and also a s 2 square plus bs 2 plus c equals 0 and let us assume that the magnitude of s 1 is much smaller than the magnitude of s 2; you can verify this for yourself. You can write down the expression for

the solution of the quadratic equation and see that this is indeed the case and in this case it turns out that first of all for s_1 , this term will be negligible compared to s_1 and c .

So, this is approximately equal to 0 and we can easily determine s_1 to be approximately $-\frac{c}{b}$ ok. What we have done is to reduce the quadratic equation to a first order or a linear equation. Similarly for s_2 , it turns out that this is much smaller than s_2 and s_2 can be approximated by $-\frac{b}{a}$ ok. Again, we had to solve only a linear equation.

Now, you have to keep in mind of course, that this is true only when one of the magnitudes is much smaller than the other. Now, in fact, you can try solving every quadratic equation that you see approximately like this and see if it is indeed true that one of the roots has a much smaller magnitude than the other. If it is then, it is consistent otherwise it is not ok.

Once you follow this procedure and find the roots s_1 must come out to be much smaller of magnitude than s_2 . Now, clearly this will not hold when the quadratic equation has complex conjugate roots because when you have 2 roots which are complex conjugates of each other. The magnitudes of the 2 roots; is exactly the same. So, this will hold only for real roots which are very far from each other ok. So, this at least looks manageable given the complexity of the coefficient a , b and c ok.

So, now let us find out the values of these.

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The image shows handwritten mathematical derivations for two poles, p_1 and p_2 , in a circuit analysis context. The derivations are as follows:

$$p_1 = -\frac{c}{b} = -\frac{G_1 G_2}{C(G_{m_2} + h_{12} + h_{o_1}) + C_1 G_2 + C_L G_1}$$

$$= -\frac{G_1}{C\left(\frac{G_{m_2}}{G_2} + 1 + \frac{h_{o_1}}{h_{12}}\right) + C_1 + C_L \frac{G_1}{G_2}}$$

$$p_2 = -\frac{b}{a} = -\frac{C(G_{m_2} + h_{12} + h_{o_1}) + C_1 G_2 + C_L G_1}{C C_1 + C_1 C_L + C_L C_1} \quad (C+C_1)$$

$$= -\frac{\frac{C}{C+C_1} \cdot h_{m_2} + h_{o_2} + h_{o_1} \cdot \frac{C+C_L}{C+C_1}}{C_L + C_1 C / (C+C_1)}$$

I will call this Pole P 1 to be the smaller one and that is nothing, but minus c by b and this if I substitute the coefficients from a quadratic equation what do I get? So, this is the expression, we have this is still somewhat complicated. But as you will soon see you can make intuitive sense out of this one, I will just divide both numerator and denominator by G_2 to put it in a more meaningful form.

The reason I did this is to get the answer in the form of some conductance divided by some capacitance as you can see the numerator has some conductance G_1 and the denominator has terms which represent capacitances well later make sense of what these capacitances are ok.

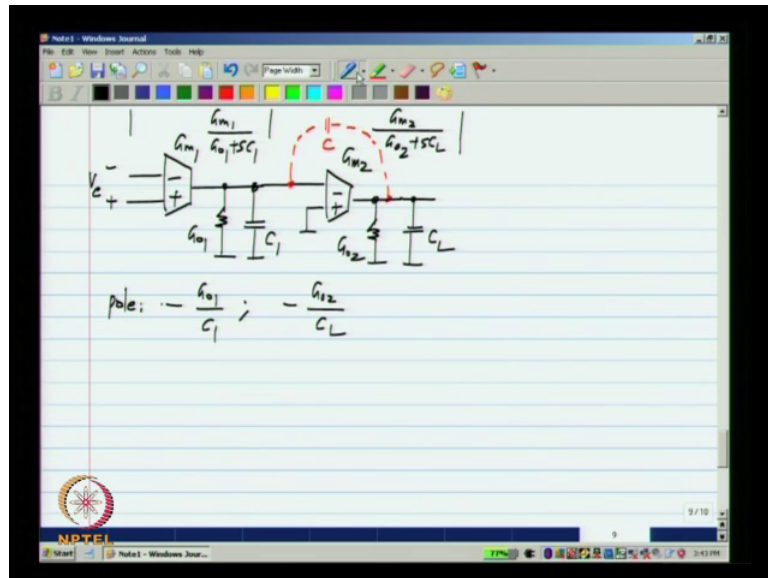
Similarly, the higher of the 2 routes; the higher frequency route p_2 will be minus b by a which is minus and here, we will have and in this particular case I will divide both the numerator and denominator by $C + C_1$ ok.

Again, you will later see why this makes sense. So, first of all I will have C by $C + C_1$ times G_2 in the numerator you see that G_2 is multiplying both C and C_1 . So, we will have plus G_2 and plus we will also have $G_1 C + C_1 G_1$ by $C + C_1$ and in the denominator I will have $C L + C_1 C$ divided by $C + C_1$ ok.

So, again I have made some manipulation of the expression. So, that in the numerator I have a; conductance and in the denominator we have a capacitance ok. So, that makes it

easier to make sense out of the poles. Now before we try to do that let us first quickly review how one might be able to tell the values of the poles in a circuit intuitively without doing circuit analysis ok.

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So, let us take the simple opamp we had earlier. Let me just call the capacitance C_1 and this conductance G_{o1} that is simply the output resistance of this conductance G_{m1} ok. Now you can work this out and see right and you will find that the pole is at minus G_{o1} by C_1 . I will not do the analysis here and similarly. You can let us say add another stage here; let us say this is a trans conductance G_{m2} and this is a conductance G_{o2} with a capacitance C_L ok.

Now, you can work this out it turns out that you will have some transfer function from here to there and another one from here to there and the 2 are independent that is the first 1 has a transfer function G_{m1} by G_{o1} plus sC_1 the second 1 has a transfer function G_{m2} by G_{o2} plus sC_L and the final transfer function is the product of the 2 and there will be 2 poles ok. And the second pole is due to the second stage due to this combination the first pole is due to that G_{o1} by C_1 and there will be another pole at minus G_{o2} by C_L ok.

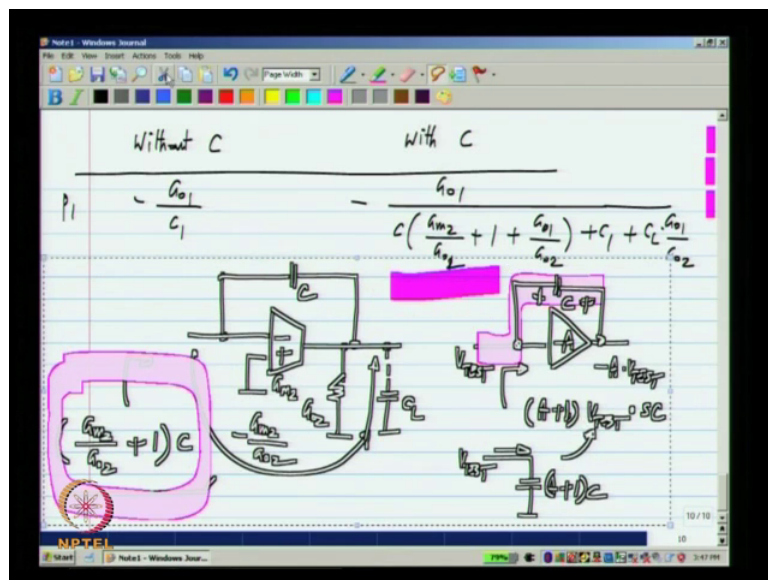
So, in circuits we are you have these R C parallel combinations which are isolated from each other you can identify the poles to be simply minus the conductance divided by the capacitance across it ok. So, you identify capacitance, you find what conductance

appears across them and the ratio of conductance to capacitance gives you the poles and you must have done this in basic circuit analysis also with simple R C circuits and exactly the same thing holds in this case ok.

Now, when you have capacitance and resistance connected in arbitrary fashion; this is not easy to do or maybe even impossible to do, but when you have isolated pieces of our senses you can do this ok. Now you also notice that the example circuit I took is exactly the same as this opamp except that I did not have this C ok. In my refined opamp, what I think is the refined opamp I also have this capacitor C ok. Now without that C, we can identify the poles very easily.

Now with C, we have identified the poles to be this one and that one ok. Now we will try to relate the case without C and with C and see how it makes sense. So, also notice that this pole has a conductance G_{o1} and some capacitance and here, it has a conductance G_{o1} and a capacitance C_1 which is across it. Similarly, this has G_{o2} plus some conductance divided by some capacitance; whereas, here we have G_{o2} divided by C_L ok.

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So, without C, I have minus G_{o1} by C_1 . And with C, I have minus G_{o1} by $C G_{m2}$ by G_{o2} plus 1 plus G_{o1} by G_{o2} plus C_1 plus C_L times G_{o1} by G_{o2} .

Now, we can already see some relationship between the two, we have G_{o1} by C_1 plus some capacitance and what is that capacitance? That is C times G_{m2} by G_{o2} plus 1 ok. Now why do I get a term like this; if you observe the second stage looks like this one; it also has this capacitor C_1 . For the moment, let us ignore this capacitor. So, basically from here to here from here to the output there is a gain of minus G_{m2} by G_{o2} and this capacitor C is connected across an amplifier whose gain is minus G_{m2} by G_{o2} ok.

So, let us say I have an amplifier of a negative gain minus A and I connect a capacitor across it; what happens? And let us say I apply some test voltage to the input. The output will be minus A times we test and the voltage across the capacitor in this polarity will be A plus 1 times sorry, in this polarity will be A plus 1 times V test.

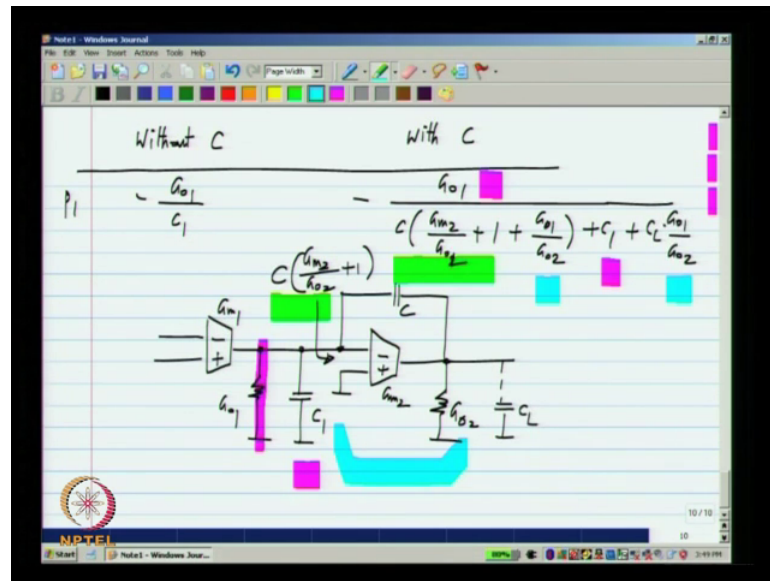
So that means, that from this source V test it will draw a current which is equal to a plus 1 times V test times SC ok. So, simply looking into this block, it appears like I have a capacitance of A plus 1 times C because if I apply V test to this, the current flowing here would be exactly same as that one ok.

This phenomenon is known as Miller Effect. If you connect a capacitor from the input to output of a negative gain amplifier, from the input it looks like a much larger capacitor and how much is it? It is equal to 1 plus gain times the capacitance value and this capacitor is also sometimes called the Miller Multiplied Capacitor ok.

Now, the second stage over opamp, I has a negative dc gain of c_{m2} by G_{o2} ; we have a capacitor C connected across it. So, looking in here it approximately looks like a capacitance. So, G_{m2} by G_{o2} plus 1 times C ok. It is only approximately. So, because the amplifier we have here is not an ideal ok; it is not an ideal voltage controlled voltage source of this game unlike this one.

This is a ideal voltage controlled voltage source of gain minus A ; whereas, here it is a trans conductor loaded by a resistor there is also a capacitor here and so on. So, only approximately it looks like a capacitor. So, you do see that in addition to C_1 which appeared across G_{o1} you also have this particular term ok.

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So, in other words, if I redraw the complete opamp this is the first stage C_1 ampere will directly across G_{o1} and we have this capacitor across an amplifier whose dc gain is G_{m2} divided by G_{o2} . And there is also some capacitance C_L here.

So, approximately looking into this, we see a miller multiplied capacitance C times G_{m2} by G_{o2} plus 1 ok. So, what do we have? We have a conductance G_{o1} that is there we have a capacitance C_1 that is there and we have a miller multiplied capacitance which is there.

Now, there are also these other terms this one and that one; they appear because first of all this pole itself was obtained approximately and secondly, that is as an approximate route to the quadratic equation and secondly, this amplifier is not ideal ok. It is it has a finite output resistance; I mean non zero output resistance and so on.

So, you also have these extra terms, but it turns out that the significant terms are what is highlighted here C_1 and the miller multiplied C ok. So, although the expression was complicated we were able to make intuitive sense out of it which is good.

So, what happens is that we will have across the conductance output conductance of the first stage, we effectively have these 2 capacitors capacitance C_1 and the miller multiplied capacitance C because C is connected across the input to say is connected from the input to output of the second stage ok.

Now, it is also of interest to see what has happened to this pole frequency. As it increased or decreased, what do you think? So, you can see that first of all it is obviously, reduced in frequency because the numerator is the same the denominator C 1 remains as it is.

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The image shows a whiteboard with handwritten mathematical expressions for pole frequencies p_1 and p_2 in two columns: "Without C" and "With C".

For p_1 :

- Without C:** $p_1 = -\frac{g_{o1}}{c_1}$
- With C:** $p_1 = -\frac{g_{o1}}{c \left(\frac{g_{m2}}{g_{o2}} + 1 + \frac{g_{o1}}{g_{o2}} \right) + c_1 + c_L \frac{g_{o1}}{g_{o2}}}$

An arrow points from the "Without C" expression for p_1 to the "With C" expression, with the text "low frequency" written below it.

For p_2 :

- Without C:** $p_2 = -\frac{g_{o2}}{c_L}$
- With C:** $p_2 = -\frac{g_{o2} + g_{m2} \frac{c}{c+c_1} + g_{o1} \frac{c+c_L}{c+c_1}}{c_L + \frac{c \cdot c_1}{c+c_1}}$

And we also have this and if C is comparable to c_1 G_{m2} by G_{o2} is a number mod that is much more than one. So, the denominator has increased a lot. So, when you have no capacitor and when you have a capacitor, it moves to low frequency ok.

Similarly, P_2 which was minus G_{o2} by C_L became minus G_{o2} plus there are other terms like $G_{m2} \frac{C}{C+C_1}$ plus $G_{o1} \frac{C+C_L}{C+C_1}$ and divided by C_L plus $\frac{C \cdot C_1}{C+C_1}$ and the next lecture, we will go and see interpret this and then make sure that it makes intuitive sense as well ok.

In the next lecture, what we will do is we will make sense out of this expression as well and see how it makes intuitive sense.

Thank you and see you again.