Analog Integrated Circuit Design
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Lecture -12
Single stage opamp realization

Hello and welcome again. So, far we have looked extensively at negative feedback systems and how to design them? How to design negative feedback amplifiers without significant ringing in the step response? So, now, will switch gears a little bit and actually try to implement the integrator first at the control source level and then finally, at the transistor level ok.

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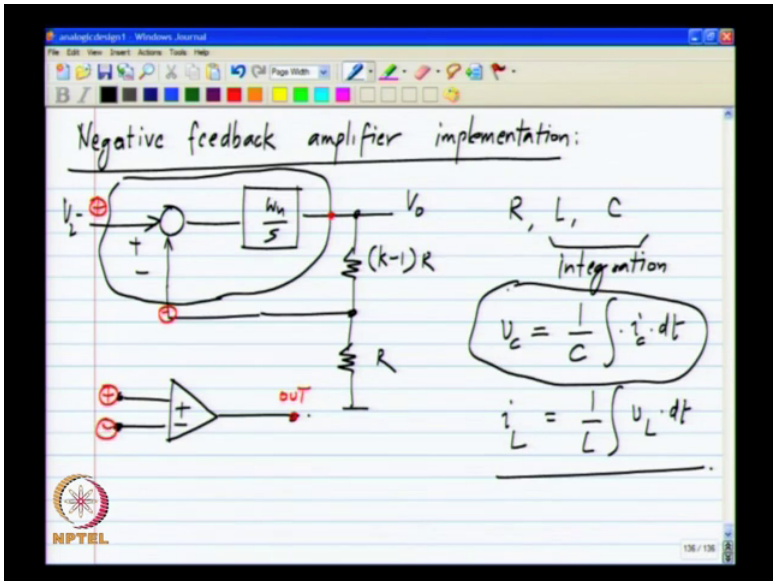

So, as you know this is an amplifier of gain k and we have investigated its behaviour extensively able to implement. This we need to have way to take the difference between the input and the feedback quantities and a way to integrate it ok. And this combination of taking the difference and integrating it, we know is the op amp or the operational amplifier. So, this corresponds to these terminals; we can think of this as a plus terminal minus and this is the output.

Now, how do we actually go about implementing this one? First of all we need to be able to make an integrator and we know of only 2 elements of the basic elements R L and C. 2 elements which can implement integration ok. So, the capacitor integrates the current

into a voltage; the voltage across the capacitor will be integral of the current flowing through the capacitor and similarly, the current in an inductor is proportional to the integral of the voltage across the inductor.

So, in principle we can use either of these to implement the function of integrating with respect to time. But in practice inductors are harder to come by and more restricted in the range of values. So, it is easier to make good quality capacitors and good quality inductors and inductors also tend to be bulky. And as you know this course is entitled analog integrated circuit design and on an integrated circuit everything is very small. So, you cannot use a inductor as an integrator very effectively. We have to use a capacitor ok. So, that is what we will do and our implementation of the integrator will consist of a capacitor.

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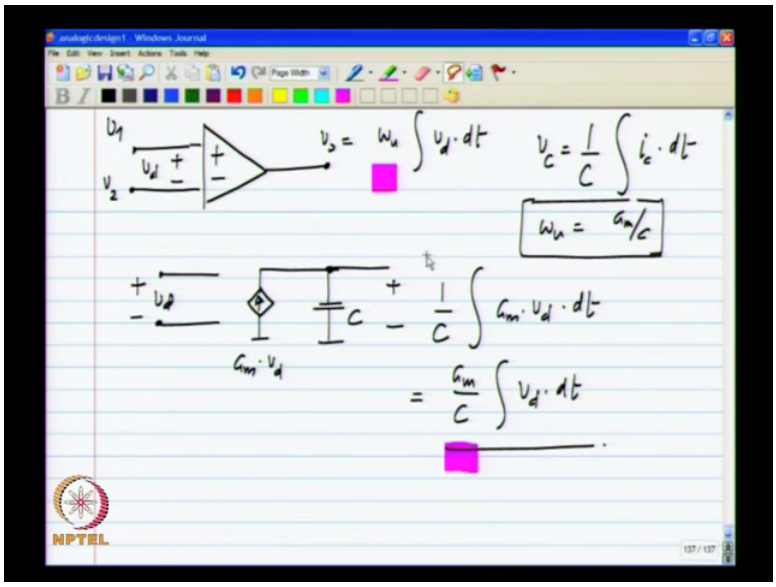

Now, a capacitor integrates the current flowing through it ok. Whereas, we want to integrate let me call this V 1 and V 2 and the difference is Vd. These are the inputs of the op amp as we have defined it and we want to integrate Vd to get V owe would like Vo to be some omega u integral of Vd with respect to time ok.

So, first we need to convert the difference Vd into a current and make that current flow through the capacitor ok. The way to do that is by using a voltage controlled current source and the voltage controlled current source will have a proportionality constant Gm and the current will be Gm times Vd.

So, this means that if difference Vd is applied to the inputs of the voltage controlled current source, the voltage controlled current source drives a current Gm times Vd and that is made to flow into a capacitor C and the voltage across this is 1 by C integral Gm Vd d t which is Gm by C taking the constant outside integral of Vd d t ok. So, comparing these we see that the unity gain frequency of the integrator or the op amp by itself is omega u which is Gm by c.

So that is all that is there to it; we now have a block that takes the difference Vd and integrates it to give you Vo ok. So, let us see if we can build our amplifier using this.

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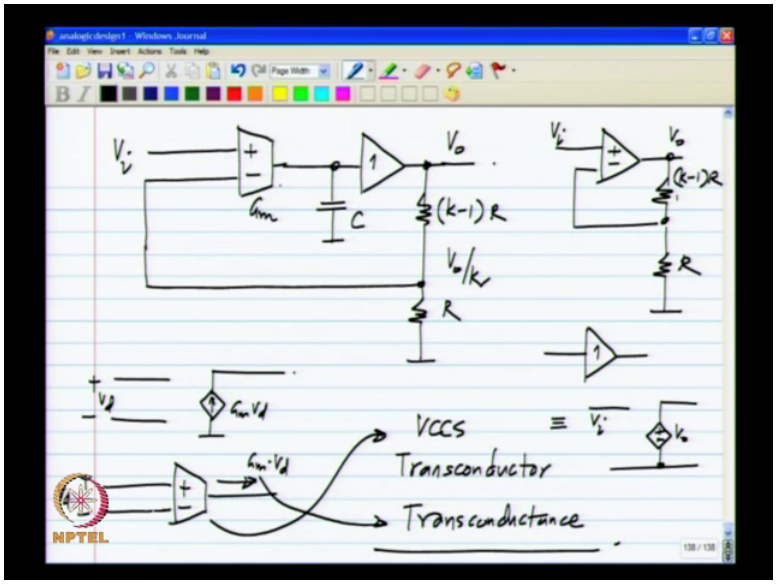

And, we know that our amplifier has to look like this 1 there are many kinds of amplifiers you can build, but will still take our prototype amplifier that we started with; the amplifier of gain k ok. Here, we have to have our resistive divider and this is Vd and I will use the simpler notation of simply writing Gm, but it is understood that the current here will be Gm times Vd ok.

So, think about this for a moment think about the circuit and see if it will work. If you look at this our idea was to convert Vd to current and then, make the current go through the capacitor, but now we have connected the resistive network. So, a part of the current will go through that. So, the voltage V naught is simply not the integral of Vd, but it also has some other complicated terms.

And if there R happens to be very small hardly any current goes through the capacitor and most of it will go through the resistors ok. So, this circuit by itself will not do we cannot use this ok. Because what we connect to the output disturbs the action of integration. So, we need to insert a buffer here, which I will denote like this.

This means that the voltage here is exactly the same as the voltage there and this can drive a load this can supply any current that is needed by the load ok. This is equivalent to you have Vi here. It is a voltage controlled voltage source of gain 1 ok. So, once we do this, our job is complete because now any current from the control source flows into the capacitor and the buffer isolates the capacitor from what is happening outside.

And now, you can see that. If you have a constant Vi and you are divided by k which is being compared is different from Vi. Then a current will flow either into the capacitor or out of the capacitor and the capacitor voltage will go on changing. The capacitor voltage will stop changing; it will remain static only if we are Vo by k happens to be exactly equal to Vi or Vo happens to be k Vi ok. So, this is the amplifier which we learned earlier. So, this is the simplest implementation of the op amp, you need a voltage controlled current source and a capacitor ok.

So, I will make 1 more change to this diagram which is more of a notation change. So, in IC design, it is common to denote a voltage controlled current source of this sort with this particular symbol which looks like the symbol of the op amp with its nose chopped off. So, you have the difference Vd and this means that if it is applied in this polarity indicated here, plus minus a current Gm times Vd is forced out of the voltage controlled current source. This is a voltage controlled current source also known as a Transconductor and this Gm is the Transconductance.

So with that change the picture of my op amp implementation will look like this ok. And I will write Gm here to indicate the Transconductance that is all that is there to it. So, we have the op amp. Now, what can be the possible problem with this? Because we know how to make voltage controlled current sources, we know that every MOS transistor or even bipolar transistor is a voltage control current source we can use it here in some form or the other, will see exactly how to implement it.

But before that let us say what possible non idealities we can have when we come to the implementation. What do you think please think about it for a moment. What possible

non idealities you can have? Now, the obvious thing is that you cannot make an ideal current source. An ideal current source has an infinite output resistance and any current source that you make whether it is controlled or fixed will have a finite output resistance which means that.

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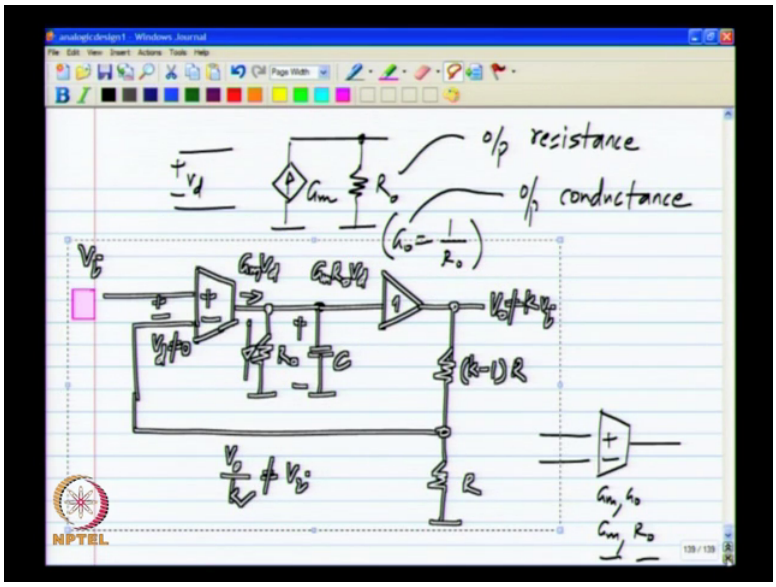

I cannot make this by itself. It will always be accompanied by some R out or sometimes I will indicate it by Go which is the reciprocal of Ro the output conductance.

So, what does this mean for our op amp? By the way this while using the new symbol can be shown outside or sometimes just to make the schematic simpler; we may write Gm and Go which means that this has a transconductance of Gm and an output conductance of Go or alternatively we could even write Gm and Ro which means that it has a transconductance of Gm and an output resistance of Ro ok.

So, let us do that to our amplifier and see exactly what happens? In this case I will show it explicitly outside. First, let us reason out what happens and then, analyse and see exactly what happens ok. So, again let us assume that Vi is a constant and let us say what is the value of Vo that we get. Earlier if we a was a constant eventually we would go to a value which is k times V i.

So that is how we got the amplifier. Now, let us say if V not is k times Vi this will be V not by k which will be equal to Vi ok. And the difference voltage of the transconductance

is 0 which means that the current flowing out is 0 and because the current is 0 the current through the resistor will be 0 and the voltage across this is also 0, but we have a contradiction here if this is 0 volts the unity gain buffer will make the output also 0 ok. So, there is a problem; I mean this is the output cannot be at k times Vi ok. So, what should happen is that V naught will be at some voltage which is not k times Vi and we not by k will not be equal to Vi.

So, there will be some difference voltage here which is not 0 and that difference voltage should be such that Gm times Vd and flowing through the resistor produces a voltage which is equal to V naught that is Gm time Ro times Vd equals V naught. Note that I am ignoring the current flowing through the capacitor because I am considering the steady state with a dc input. In dc steady state, there is no current flowing through the capacitor. So, the difference should be such that the output Gm Ro Vd equals V naught.

So, we can do the analysis exactly and see what happens? Let us say V naught is some value and this is at V naught by k and Vd equals.

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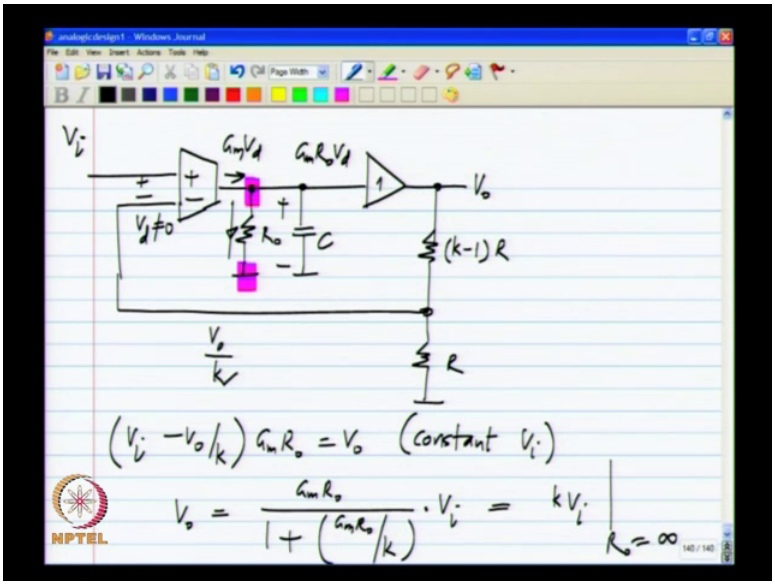

Vi minus V naught by k and that times Gm Ro is the voltage developed across the resistor and that is the same voltage that is given out as V out. So, this is equal to V naught ok.

So, this says that V naught is Gm Ro divided by 1 plus Gm Ro by k ok. We know this Gm Ro divided by 1 plus Gm Ro sorry times Vi and this is for constant Vi that is Vi is dc and we can see that in the limiting case where Ro goes to infinity; this is k times Vi when Ro is infinity, it passes the sanity check whatever case we had originally with ideal voltage controlled current source, this satisfies that 1 that corresponds to R equals infinity ok. So, when Ro is not equal to infinity; Ro is less than infinity, this number will be smaller than k.

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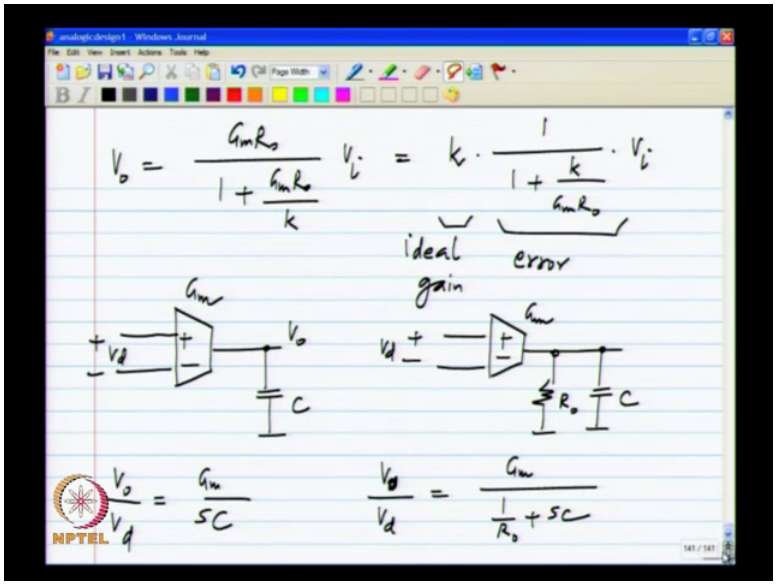

So, that is very obvious if we write it in an alternative form which is k 1 plus k by Gm Ro times Vi.

So, we have the ideal gain here and we have an error here due to the fact that Ro is not infinite ok. So, we can analyse this a little more and interpreted what interpret what it means? So, first way let us look at what is the transfer function of the op amp in this case.

So, ideally we wanted the op amp to be like this that is without any output resistance in the transconductor and the transfer function of the op amp was Gm by S C and Gm by C is the unity gain frequency omega u. But in reality, we have Vd we have Gm and we also have Ro ok.

So, in this case V naught by Vd will be Gm divided by the total admittance at the output which is 1 by Ro plus S C ok. So, we have an extra term and the pole which was at the origin has moved to a different frequency. In this case the pole is at the origin and in this case the pole is at a different frequency ok. So, let me make these of a different color just for distinction.

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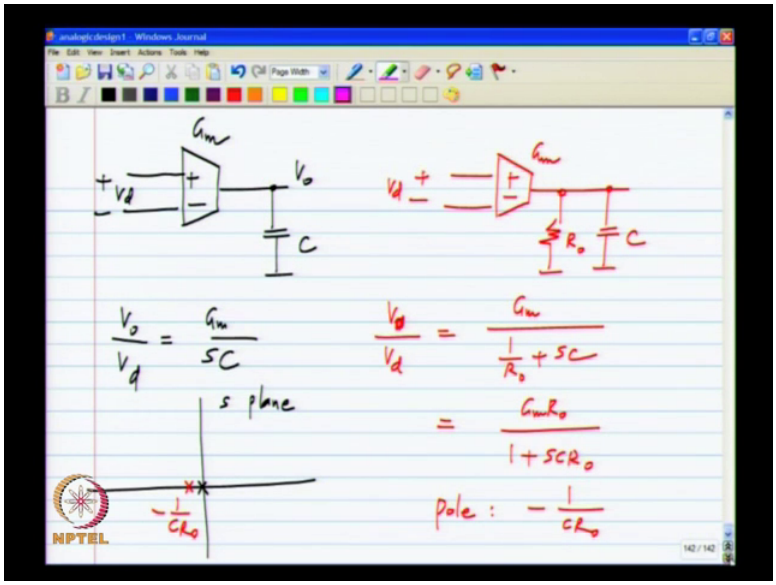

So, if you look at the s plane originally the pole was here and now, this can be written as for instance Gm Ro 1 plus S C Ro and the pole is at minus 1 by C R naught ok. So, the pole moves into the left half plane and exactly how much it moves depends on the value of R naught; the higher the value of R naught the lesser the movement into the left half plane ok.

So, that is what it looks like and we can also look at the magnitude and phase of the 2 op amps that is the ideal case when there is no R naught or R naught is infinity and the actual case when there will be a finite R naught.

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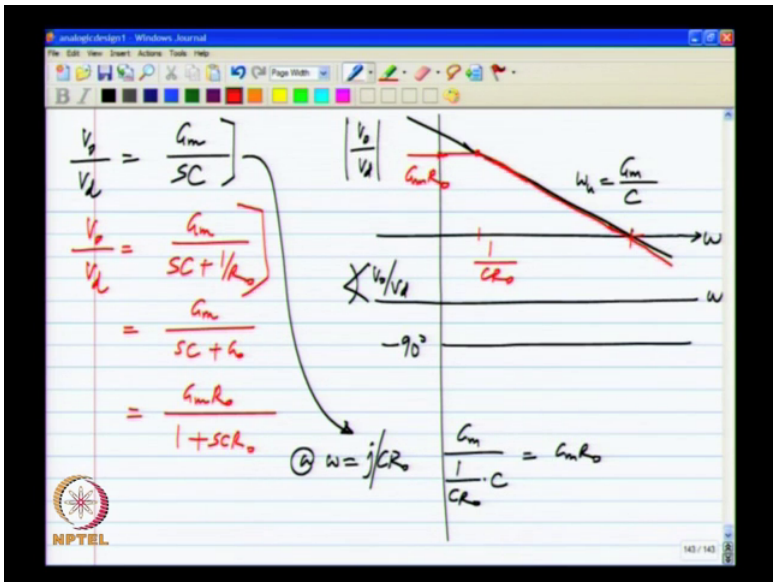

Hostile droid for the ideal case; Again, magnitude will be like that and this is Gm by C which is the omega u of the op amp. This is the magnitude plot of the gain of the op-amp and the phase plot of course, simply that minus 90 degrees or minus pi by 2. Now what happens in practice? We will get, this could also be written as Gm by S C plus G naught or in a number of other ways or Gm R naught by 1 plus S C R naught ok. So, first of all at very low frequencies this does not go to infinity.

So, it goes to Gm R naught and at frequency 1 by C R naught, it has a pole and after the pole, it drops down at 20 degree per decade ok. Notice that I have drawn the black line and the red line to be coincident after 1 by C R naught. This is because if you look at the gain of this particular function when omega equals j by C R naught, what do you get?

At omega equals j by C R naught, the magnitude of this is Gm by 1 by C R naught times C which is equal to Gm R naught ok. So, at this particular frequency even the integrator has the same gain. So, in the bode plot sense the red line meets the black line and then, follows the black line because after that the slope is 20 degree per decade for both of these curves ok. So, this also means that even this 1 intersects the unity at a frequency approximately Gm by c.

So, we will confirm that with calculation later, but that is what happens. So, the magnitude response of the non-ideal op amp follows I mean is a constant Gm are not up

to a frequency 1 by C R naught, after that it follows the same frequency response as that of the ideal op amp ok.

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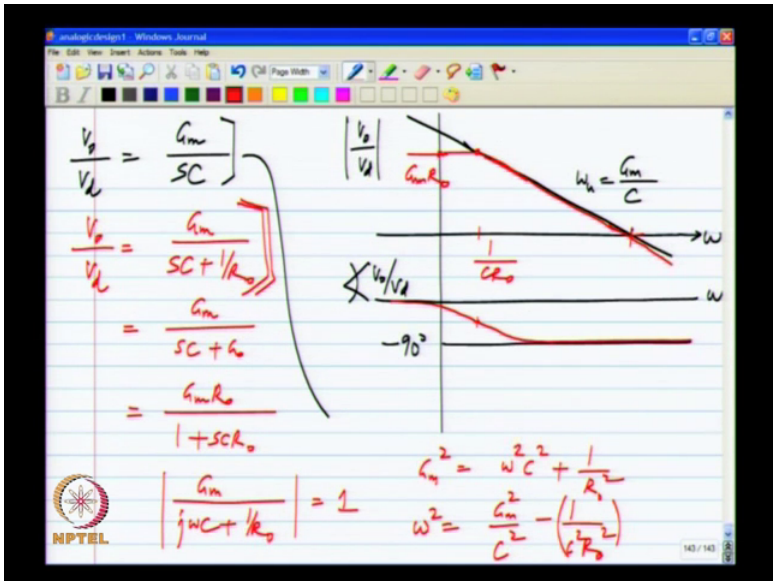

So, similarly the phase plot, it does not start from minus 90, it starts from 0, but at 1 by C R naught it goes to minus 45 degrees. And soon after that it goes to minus 90 degrees ok. So, the difference occurs only in the low frequency range in the frequency 1 by C or not and surrounding it. At very high frequencies the 2 transfer functions identical ok.

So, in circuit terms, what this means is that if you think about it, at low frequencies the all of the current from Gm goes into R naught; whereas, in the ideal case the current from Gm always goes into the capacitor. So, that is a substantial difference, but at high frequencies what happens is the impedance of the capacitor is much less than the impedance of this output resistance R naught.

So, most all of the current or most of the current from Gm goes into the capacitor which is the same as in the ideal case. So, this means that at high frequencies these 2 are more or less the same. At low frequencies they are not the same because the current from Gm goes through R naught here. Whereas, here even at low frequencies it has to go to C and from the analysis also it is clear at low frequencies there is a difference in characteristics at high frequencies there is no difference.

And just for completeness will calculate when the magnitude response here goes to unity to be unity ok. So, this means that Gm square is omega square C square plus 1 by R naught square. So, omega square is given by Gm square by C square minus 1 by C square R naught square.

So, as long as this is very small ok, as long as 1 over C R is much smaller than Gm by C, the unity gain frequency is still approximately Gm by C and we see that this is invariably the case for any reasonable op amp because if this condition is violated the op amp will be almost useless ok. Now let us take a look at this whole thing in terms of the loop gain of the system.

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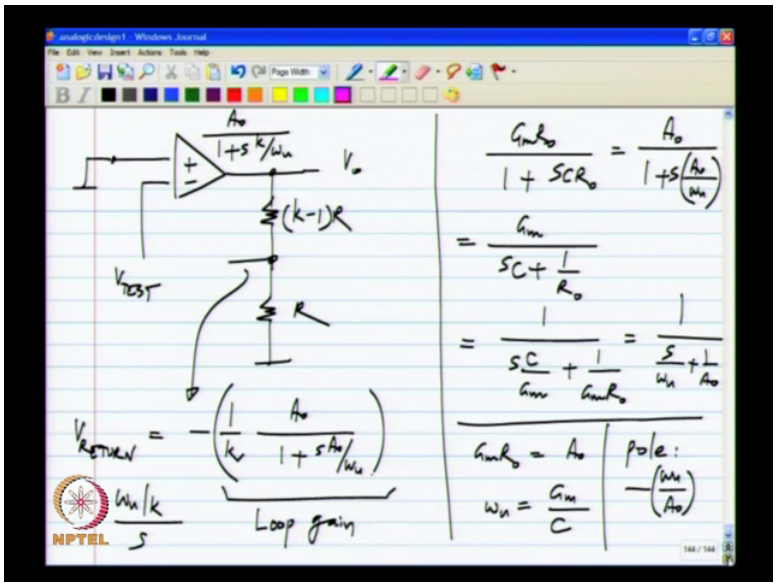

So, we now have an op amp, whose transfer function is not of the form omega u by s. So, let us write it in general terms the actual transfer function is Gm R naught by 1 plus S C R naught this is 1 way to write it or we can write it as Gm by S C plus 1 by R naught or equivalently also as 1 over S C by Gm plus 1 by Gm R naught.

So I will denote Gm R naught by a quantity A naught and this A naught is the dc gain of the op amp ok. As you can see if I apply a dc increment Vd, the output dc will be equal to Gm times R naught times Vd ok. So, the dc gain is Gm R naught and we know that the unity gain frequency omega u we had defined it as Gm by C, I will keep it as it is ok. So, this form if I choose I can write this as 1 by s by omega u plus 1 by A naught and this

kind of makes the non ideality very clear, if a not tends to infinity you will get omega u by s as the transfer function ok.

But it can also be written in a number of other ways if I write it in the first form I will get A naught by 1 plus S omega u by u naught sorry A naught by omega u ok. So, note that I have not made a notation for P 1. So, we have three related parameters here the dc gain Gm R naught the pole 1 by C R naught and the unity gain frequency of the original op amp, Gm by C. I will always use the gain frequency omega u and the dc gain A naught as the primary parameters and the third 1 can be derived from it. So, the pole is at naught u divided by a naught.

The pole of the system is that minus omega u by n ok. So, ideally A naught is infinity in practice it is a large number which means that the pole of the op amp will be at a much smaller frequency compared to the unity gain frequency ok. The pole should have been at the origin, but it is at a small frequency which is not at the origin ok. So, instead of this we will have u naught by 1 plus S k by omega u Vi and V naught.

Now we have evaluated systems of this type and we quantified the amount of negative feedback by loop gain and we said that whenever the loop gain is very large, the system will behave ideally and whenever the loop gain is small, the system will not behave ideally ok. And our original system when the op amp was an ideal integrator had an infinite dc loop gain eternal infinite dc gain and as a consequence it also had an infinite dc loop gain.

Now, let us evaluate the loop gain by setting the input to 0, applying a test voltage here by breaking the loop and seeing what comes back. So, it is clear what comes back? If I apply V test I get minus this whole thing times V test here and then that divided by k appears at the output of the resistive divider ok. So, the return voltage V return will be minus 1 by k A naught by 1 plus S k by omega u ok.

And the loop gain is nothing but what is enclosed in this parentheses excluding the minus sign ok. This is the loop gain and again just a quick recap, the loop gain without this non ideality without the finite output resistance was omega u by k divided by S and you can easily see that if V naught goes to infinity this reduces to that value sorry this is not S k by omega u it is S A naught by omega u; if A naught goes to infinity you will simply get 1 by k times omega u by S.

So, the key point to note is that.

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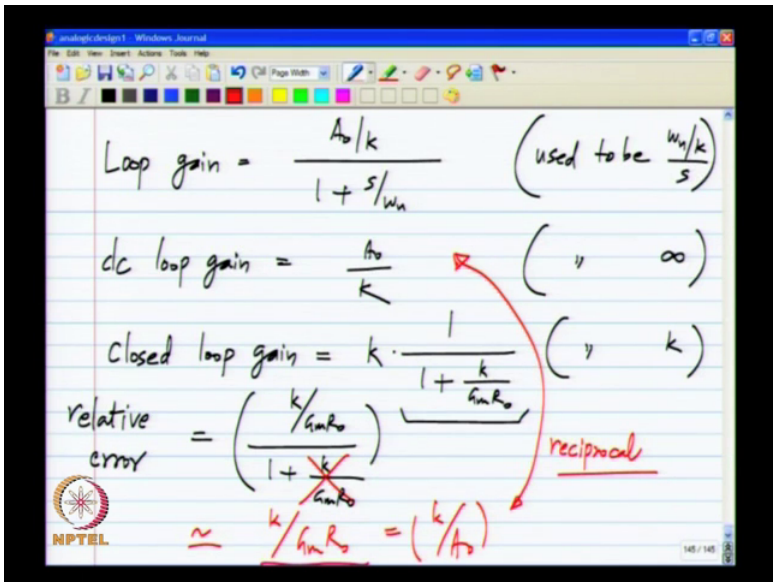

And it used to be that one, if I look at the dc loop gain, it is A naught by k and this used to be infinite ok. So, and if you look at the closed loop gain, it is equal to k 1 plus k by Gm R naught. So, let us just quickly go back and see that is what we had ok. So, if you see this is the expression, we rearranged to get that 1 ok. So, there is an error term. So, this is what we have and this used to be k ok. So, if you look at the relative error in the gain relative error means the ideal gain minus the actual gain, the difference in the gain, this will be simply that and if I further simplify it I will get that.

So, that is my error and again that is the difference between the ideal and the actual gains and that I normalized to the gain that I want k. So, that is the relative error. That is how much the relative error is and we would naturally want the relative error to be very small like a percent or 0.1 percent or sometimes even less than that ok.

So, this means that this number k by Gm Ro has to be very small and this is also kind of expected because ideally Gm Ro was infinity and now we would like it to be as large as possible ok. So, what we can do is simply neglect this k by Gm Ro in favour of 1 and approximate the relative error to be k by Gm R naught ok. So, that is the relative error. And as you see this is k by A naught k by the dc gain of the op amp and this is nothing, but the reciprocal of dc loop gain.

And again, this is not a coincidence; please think about how this happened originally the dc loop gain was infinity. So, the relative error was 0. Now the dc loop gain is A naught by k the relative error is k by A naught ok. And this is not a coincidence; this is how it should be because loop gain quantifies the amount of negative feedback, we used to have infinitely strong negative feedback at dc. Now it is only finitely strong.

So, we have a finite relative error and is also not surprising; we have seen this earlier, while evaluating the closed loop frequency response of the negative feedback amplifier we saw that the a d the loop gain was omega u by k divided by s or in general some omega u loop divided by s. So, the loop gain magnitude is very large for frequencies below omega u loop and the loop gain magnitude is small for frequencies beyond that and we have seen that the closed loop gain is close to 1 for frequencies below omega u loop where the loop gain magnitude is large; it does not follow the negative feedback amplifiers gain for frequencies beyond omega u loop.

So, the loop gain being large means that there is less error, but in this case the loop gain is not infinitely large. So, there is a relative error and the relative error is exactly the reciprocal of the loop gain ok. So, this is one of the problems with the implementation of negative feedback amplifiers that you will always have a current source with a finite output resistance which means that you will get a finite dc gain. So, what was an ideal amplifier at dc before is no longer ideal even at dc ok. So, that is the bottom line.

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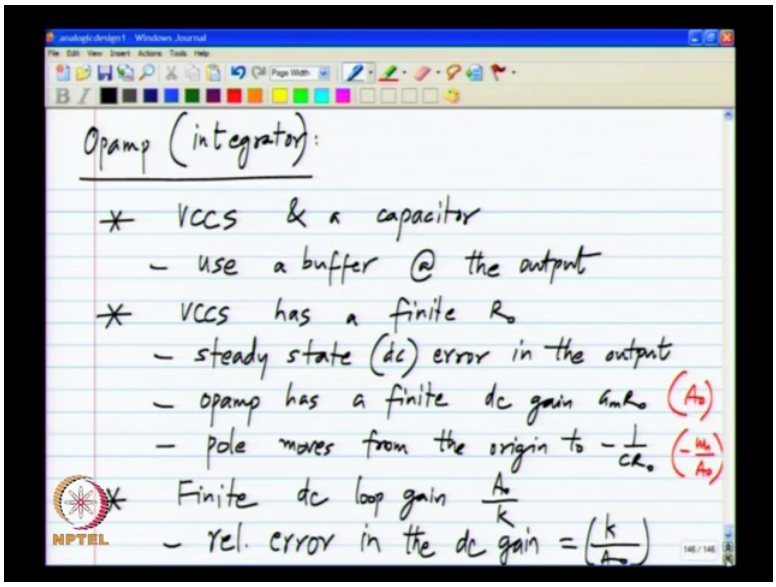

So, to summarize, to implement an op amp which is an integrator, we need to have some integrating function and which we do using a Voltage Control Current Source and the capacitor and we also use a buffer at the output. So, as not to disturb the currents flowing through the capacitor due to the load.

Now, the problem is that VCCS has a finite output resistance. So, this means that there is a steady state error that is even for a dc input for an input that is constant the output will not settle to k times the input. It will settle to something like some something slightly smaller than k times the input. So, this is known as a steady state error or a dc error ok. Equivalently, we can think of this as the op amp as a finite dc gain, Gm Ro and because of this the pole moves from the origin to minus 1 by C R naught ok.

So, in more general terms the op amp will always have a finite dc gain A naught which is not infinity and the pole moves to minus omega u divided by A naught ok; where, omega u is the intended unity gain frequency of the op amp. And finally, the result of this is that you have a finite dc loop gain which is A naught by k which gives a relative error, you can think of it as a relative error in the dc output or relative error in the closed loop dc gain of k by A naught that is the reciprocal of the loop gain.

So this is one of the implementation problems that we have to deal with, right. Because we cannot make ideal current sources we have to live with finite dc gain and this causes an error even in the dc gain of the amplifier ok.

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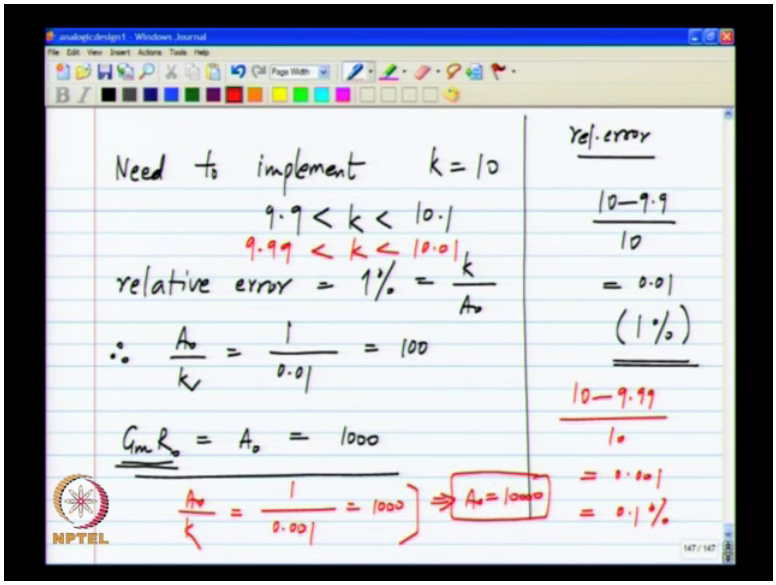

So, just to get a feel for numbers let us say I want to implement amplifier of gain 10 ok. I know that I am going to get an error and I would like the relative error to be less than something and I will say that my k has to be between 10.1 and 9.9 ok. So, now, we know that the finite dc gain of the op amp will make the gain smaller. So, it is going to be about 9.9 ok. So, what is the relative error here 10 minus 9.9 divided by 10 which is equal to 0.01 or 1 percent. The relative error is 1 percent. So, we need a sufficiently high dc loop gain.

This we know is k by A naught the reciprocal of the dc loop gain. Therefore, the dc loop gain has to be 100 and therefore, the dc gain of the op amp Gm times R naught which is A naught should be a 1000 ok. So, this now put some more constraints on the op amp.

Before we were only concerned with implementing a certain unity gain frequency which lets us choose a certain capacitor C and a certain trans conductance Gm and we also have to make sure that whatever circuit you use to design the Gm should have a sufficiently high R naught and how high is it? It should be such that Gm R naught is 1000 for this particular example.

Now this is not some fixed number. So, it could be that in some cases I want the gain to be controlled even better I want it to be between 9.99 and 10.01. So, in this case the relative error is 0.001 which corresponds to 0.1 percent. So, obviously, for this particular example A naught by k should be 1 by 0.001 or 1000 ok. The dc loop gain itself has to be 1000. So, that you get a 0.1 percent relative wherever in the gain or 0.1 percent relative error in the dc output steady state output.

And this implies that A naught has to be ten thousand ok. So, the more the accuracy you want the higher the value of A naught you want. So, which means that you have to take more care in the design of your op amp so, that it gives you a high dc gain ok. Finally, the dc loop gain is the dc gain of the op amp times whatever is the gain of the feedback network; if you want to make an our non-inverting amplifier in 10. The gain of the feedback network is 0.1. So, the gain of the op amp has to be 10000.

So, this puts some additional constraints on the op amp and also this is the reason why we have to go for more and more complicated topologies. In some cases you may end up with having to need an op amp gain of a hundred, thousand or a million in which case the

structure of the op amp can be very complicated ok. So, before going to a new topic, let us just see what happens because of this at high frequencies ok.

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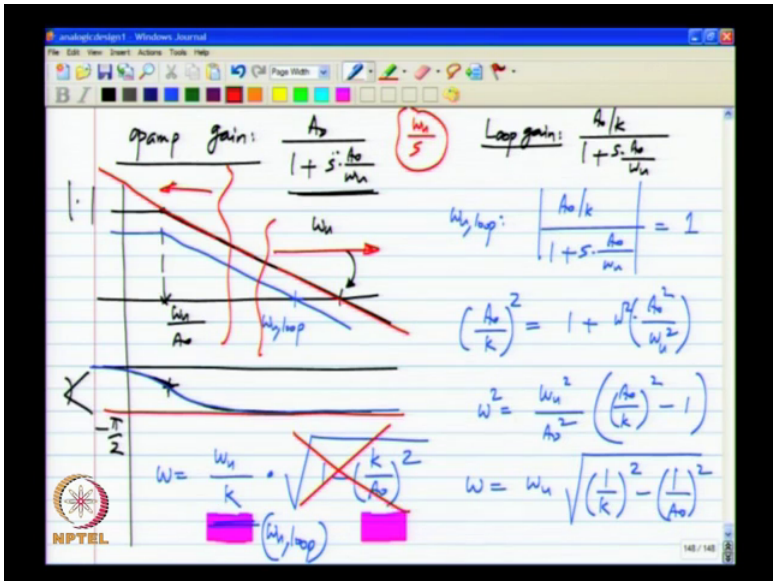

The op amp gain is A naught by 1 plus S A naught by omega you ok. So, I will draw the magnitude and the angle of this one. So, that is how it looks like and ideally, they should have been simply omega u by S which means that the magnitude R, I mean like that. Similarly ideally the phase would have been that way and in reality the phase would be something like that.

Where, this frequency is omega u; we said that even for the op amp with the finite dc gain it is approximately omega u. This frequency is omega u by A naught and this angle is minus pi by 2 ok. Now, we have done a lot of study of to make the loop gain. So, that the closed loop system is stable and so on. Now we would also like to see, if this problem of finite dc gain has an effect on that because we did a lot of hard work lot of analysis.

Now, if we have to go and change it all again because of this finite dc gain problem, it will be a waste ok. Now, let me specify the loop gain; the loop gain is what matters not the gain of the op amp. All I have done this I have taken this expression and divided by k this is the case for our prototype amplifier. So, what does it mean as far as the magnitude is concerned it simply shifts down.

All I have to do is to shift down that curve ok. Let me; In fact, it is better to put it on the same plot, I will do that. And what happens to the face? As you can see nothing happens to the face because I have only divided the loop gain by a real number. So, nothing happens to the face. So, the face follows the same curve and this is my unity loop gain frequency ok.

So, omega u loop is where the magnitude of a not by k divided by 1 plus S A naught by omega u becomes 1 ok. Now the reason I am worried about it as I said this we did a lot of hard work lot of analysis and we do not want to have to redo everything if we can help it ok. So, we have to see what happens to all our conditions etcetera because of the dc gain. Now, one of the things you remember is that from the Nyquist plot for stability, the area of interest is around minus 1 comma 0 that is we are looking at when the magnitude of the loop gain becomes close to 1.

We are not interested in what the magnitude of the loop gain is when it is very large at low frequencies ok. The stability dependent depended on like for instance, if you recall the condition P 2 had to be greater than 4 times the unity loop gain frequency ok. And the P 2 had to be much beyond the unity loop gain frequency and so on. So, what we are interested in this one in the region around where the loop gain becomes unity ok.

So, let us solve for this, we will get A naught by k square to be 1 plus omega square A naught square by omega u square ok. So, if I simplify this I will get omega square to be omega u square by naught square times A naught by k whole square minus 1 or I will take A naught inside omega to be omega u times square root of 1 by k square minus 1 by A naught square. I will further rewrite this as omega equals omega by k times square root of 1 minus k by A naught whole square.

I wrote it in this form because omega u by k is the unity loop gain frequency, if we did not have a finite output resistance; if we did not have a finite dc gain. If we had an infinite dc gain. Now we see that it is that frequency times something square root of 1 minus k by A naught square and remember this k by A naught is a very small number that is the relative error in the dc gain and by design we would make it very small ok.

So, it is safe to neglect that one because by design we would make k by A naught very small. So, the unity loop gain frequency even when you have a finite dc gain is approximately omega u by k and that part has not changed. And this is good news for us

because all our stability criteria which has specified something about the unity loop gain frequency are the same as before and we can judge stability by looking at this type of function.

Omega u by k is assuming that it is an ideal integrator even without worrying about the finite dc gain because the finite dc gain affects only this part of it. And the stability is determined by what is happening in this part; where, the loop gain is coming close to unity ok.

So, this means that it is a very useful approximation for the stability calculations to still assume an ideal integrator, even if we have a finite dc gain as long as the dc loop gain is large and the dc loop gain will be large in any decent negative feedback system that you design; otherwise even at dc you will have a large steady state error ok. So, that ends this lecture we have looked at how to try and make the op amp and it brings one particular non ideality which is the finite dc gain. We saw what the effect is. Its effect is mainly at dc and we have to make the dc loop gain large enough to get a sufficiently small steady state error.

Now, it can also affect the stability in general what we examined it and seen that if we make the dc loop gain large enough, the stability criteria are not affected and we can evaluate the stability assuming that it is still an idle integrator and it is very good for analysis. All the analysis that we did earlier we do not have to modify them at all ok.

Thank you, see you in the next class.