Analog Integrated Circuits
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Lecture - 04
Cascode Amplifiers

In today's lecture, we are going to look at a certain type of amplifier called the Cascode Amplifier. So, we will start off by looking at the common source amplifier.

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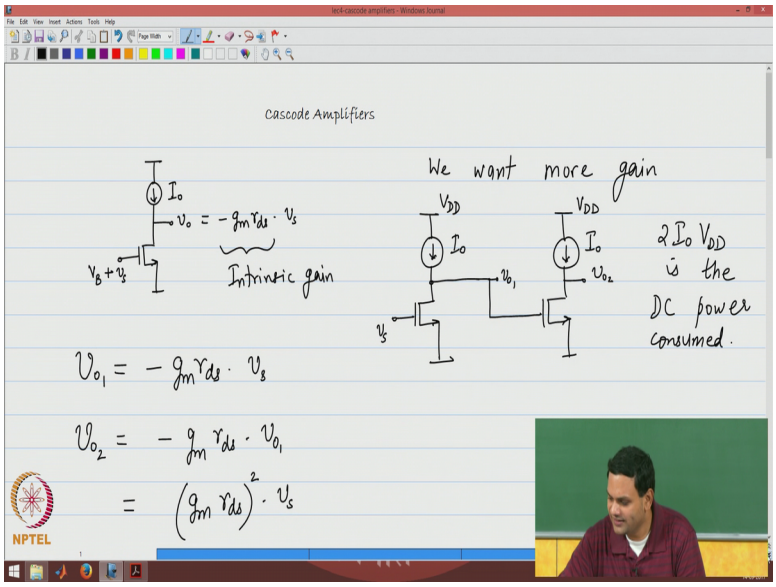

That we have seen before. So, let us assume that the common source amplifier is biased with a drain current of I naught; it has an appropriate gate bias voltage, I will call that V B and along with this I will also apply a small signal voltage V S.

We know that the output voltage that is taken at the drain for the amplifier is equal to minus g m r ds times V S. So, the gain of the common source amplifier is negative and it has a gain in for this particular circuit of minus g m r ds because I am using an ideal current source as the load for the transistor in other words there is no load resistance for this particular circuit.

This minus g m r ds is called the intrinsic gain of the common source amplifier of the MOSFET. So, this is this intrinsic gain of the MOSFET is the largest gain you can get from a MOSFET circuit with one single MOSFET with one single device. Now, let us

say we want; even more gain from the amplifier there are of course, several different ways of doing this; one way to do this is to is to cascade 2 common source amplifiers.

So, the output of the first common source amplifier is fed to the input of the second common source amplifier I am not showing the biasing details in this particular figure. So, let the output of the first stage be V o 1 and the output of the second stage be V o 2 we know that V o 1 is minus g m r ds times V s this is the gain of the first stage and V o 2 is minus g m r ds times V o 1 or g m r ds squared times V S.

So, the gain of this cascaded circuit is approximately the squared of the intrinsic gain of a single transistor now you can see that this particular circuit consumes the power of let us say these 2 transistors were biased data current I naught and the supply voltage was V DD that DC power consumed by the circuit is 2 I naught V DD; so 2 I naught V DD is the dc power consumed.

Because the original circuit consumed the power of I naught times V DD now suppose I want to get a gain of g m r ds the whole squared, but I do not want to use twice the dc power we need to come up with a different circuit that is capable of doing this. So, to see this we will look at how the signal flows through the circuit.

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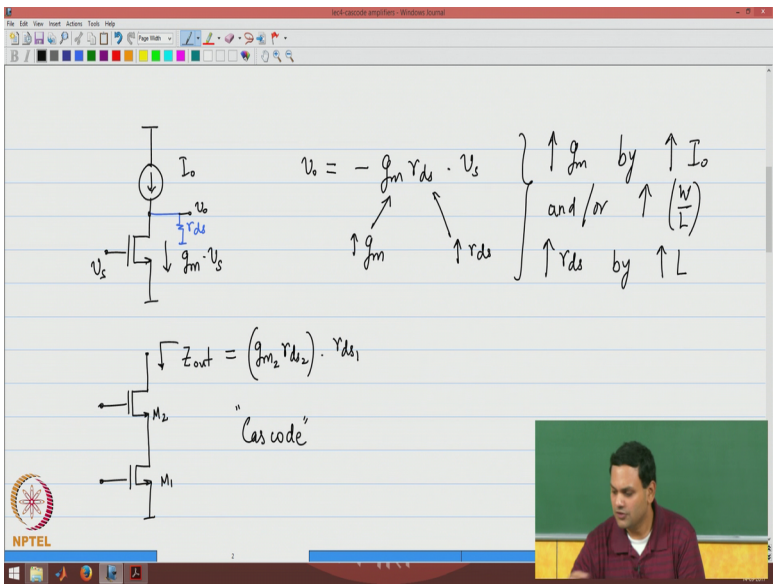

As you can see in the original common source amplifier when the source voltage is applied to the gate of the transistor this causes a current of g m times V S to flow

downwards from the drain to the source inside the transistor and what happens to the signal current; if you had a load resistance the signal current would probably flow through the load resistance.

But in our case we do not have a load resistance because this is an ideal current source of value I naught the only path for the current to flow through is the intrinsic drain source resistance of the MOSFET. So, these current flows through the r ds of the transistor I will show that here. So, the in total impedance at the output node is simply r ds and therefore, this generates a negative minus g m r ds voltage minus g m r ds times V s voltage at the output node.

Now, as you can see there are since the voltage gain is minus g m r ds times V s there are only 2 ways to change the gain of the circuit one way is to change the g m. So, we want to increase g m or you want to increase r ds how do you increase g m you increase g m by increasing I naught that is the bias current and or increasing the size of the transistor the width to length ratio of the transistor. These are the only 2 ways by which you can increase the g m of the device.

Now, if you want to there is a certain limit if you want to use the same power you can keep increasing the width over length, but there is only so much beyond which the device will not respond to increase in width these are due to certain second order effects which we are not interested in right now, but the thing I want to point out is that the increasing g m with I naught and width is limited. So eventually, I need to start increasing r ds how do you increase r ds I increase r ds by choosing a longer length for the device.

If I choose a longer length then the r ds will get larger, but again just like g m if I keep increasing the length of the device eventually r ds will reach a; you will reach a point where r ds will not respond to any increase in length anymore. So, let us say that will be the maximum intrinsic gain of this device we will assume you have already reach that maximum intrinsic gain. So, next you will now that you have reach certain device limits we will have to look at circuit techniques to increase this increase the gain.

Now, we will look at a circuit technique to increase r ds. So, we have seen in the k in the context of current mirrors that the cascode current mirror tries to increase the output resistance of the circuit of the current mirror by stacking 2 devices on top of each other.

In other words, if you look at the output resistance of this circuit, this is called a cascode connection as we have seen before the output resistance of this circuit is let me call these devices m 1 and m 2 the output resistance of this circuit is g m 2 r ds 2 times r ds 1.

It can be shown that this is the output resistance in other words the output resistance of m 1 gets amplified by the intrinsic gain of m 2. So, now, this is one way to increase the output resistance of the circuit.

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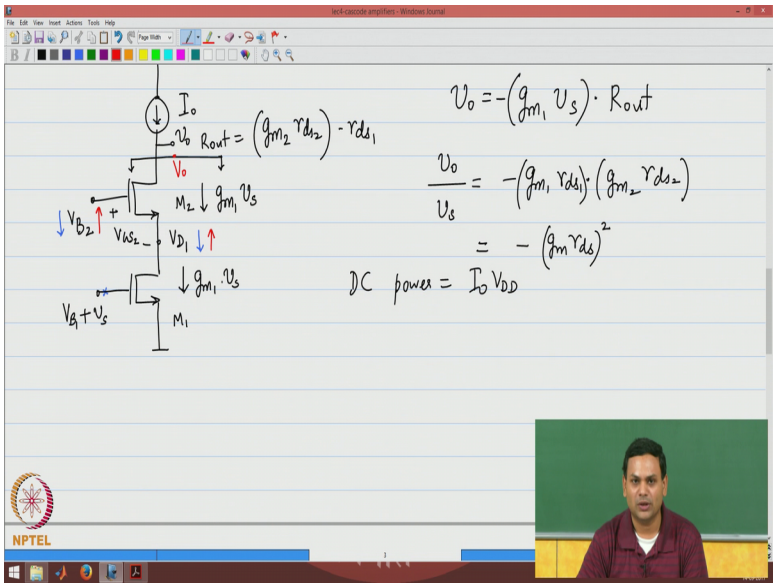

So, let us see what a cascode amplifier will look like if I were to build a cascode amplifier, I have a single current source I naught I will again call these devices m 1 and m 2 and I am going to apply a bias voltage V B 1 an appropriate bias voltage V B 1 plus the signal at the gate of m 1.

Now, in the cascode connection the gate of m 2 is not connected to a signal, but is connected to an appropriate bias voltage V B 2; we will in a few minutes, we will see what is the appropriate value of V B 2 we will want to use here, but let us look at the output resistance of this circuit as we have seen the output resistance of this circuit is nothing, but g m 2 r ds 2 times r ds 1; this is the output resistance of this circuit. Now what happens to the signal current the signal current generated inside m 1 is g m 1 times V s and as it turns out this current also flows through m 2. And eventually, since you are in this case we are loading it with an ideal current source this signal current has no other path to flow through, but the output resistance of this cascode circuit itself.

Therefore the output voltage at the drain of m 2; so V o is g m 1 V s times r out with a negative sign. So, therefore, V o by V s is minus g m 1 times r out which is as you can see I will rearrange this as you can see this is the same as the intrinsic product of the 2 intrinsic gains that we wanted to achieve.

So, now we have managed to create a gain that is the square of the intrinsic gain of a single device. So, in other words if g m 1 if the 2 transistors were identical then g m 1 and g m 2 would be equal and r ds one and r ds 2 would be equal. So, we have managed to create again that is the square of the intrinsic gain the difference in this case is that we have used only one single device one single current I naught. So, the total dc power consumption is I naught times V DD.

We do not need a cascade of 2 amplifiers we have managed to do that get this such a large gain with only one single amplifier now it turns out that there are a couple of other variance of the circuit . So, as you can see; maybe I will go back to the previous circuit you can see that the second device is a common what is called a common gate device m 2 looks like this.

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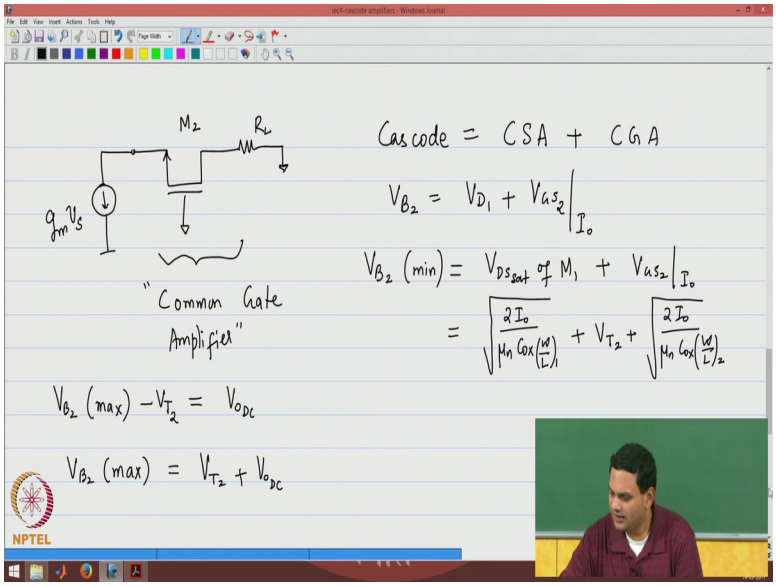

If I were to redraw it slightly differently this is device m 2 the input for device m 2 is basically the signal current of value g m times V g g m times V s and that is the this current source represents device m 1 that creates g m; g m times the s current.

For small signals the gate of m 2 is grounded and if you have a load resistance for example, at the output the small signal current would flow through that load resistance if not it would flow through the output resistance of the circuit itself. So, therefore, as you can see m 2 is simply a common gate amplifier. So, in other words the cascode connection is simply a common source amplifier stacked with a common gate amplifier. So, m 2 acts as a common gate amplifier.

Now, you can see that we have used m 2 as an NMOS transistor in reality m 2 need not have the same size. So, it could have a different g m and a different r ds and that would be a design parameter of interest, but first let us look at the constraint on V B 2 because it is a common gate amplifier the gate voltage V B 2 has certain constraints. So, if you look at V B 2, I want to find out what is the maximum value and the minimum value of V B 2 that can be applied to the circuit. So, to do that I am going to denote the voltage at the intermediate point as VD 1 which is the drain voltage of m 1 I am going to I am looking now only at bias quantities. So, V B 2 is nothing, but VD 1 plus V g s 2.

In other words, I am applying k V l around that loop. So, what does that mean if I change V B 2 the value of V B 2 since m 2 has a constant current I naught set by the current source on top what will happen is that V g s 2 will remain constant as long as m 2 is in saturation if that happens VD 1 will follow V B 2 with a difference of V g s 2 which is set by I naught. So, V g s 2 is calculated at a bias current of I naught.

So, if I keep decreasing V B 2 what will happen is that if V B 2 decreases VD 1 will continue to decrease note that for transistor m 1, this node is at a constant voltage and the drain the gate voltage this is constant the drain voltages dropping therefore, the transistor will eventually move towards the will start moving towards the triode region eventually it will hit the edge of the triode region beyond which we do not want to move; therefore, the absolute minimum voltage possible is clearly will clearly happen when VD 1 is equal to V d sat of m 1 plus V g s 2.

If I were to calculate this this is nothing but root of 2 I naught mu over mu n c ox w over l of m 1 plus V g s 2 which is nothing, but V t 2 plus V d s sat of 2 which is 2 I naught over mu n C ox w over l of 2 this is the minimum value that V B 2 can occupy what about V B 2 maximum. Low let us assume that I am increasing the voltage V B 2 I will

show that in red if I start increasing V B 2 you can see that again VD 1 will start increasing.

So, therefore, m 1 is moving further away from triode. So, there is no problem with a m one, but note that at the output if the output were biased at some voltage V o eventually that was said maybe through feedback eventually the transistor m 2 will go into the triode region that will happen when you hit the triode condition for m 2 and that is simply given by this V B 2 max minus V t equals V o d c. So, in other words V o d c is the drain voltage and that becomes exactly equal to the gate voltage which is V B 2 minus V t. And therefore, V B 2 max is nothing, but V t 2 plus the output dc voltage.

So, this as long as you choose the bias voltage V B 2 such that it lies between these 2 values you will ensure that for dc both transistors are in saturation.

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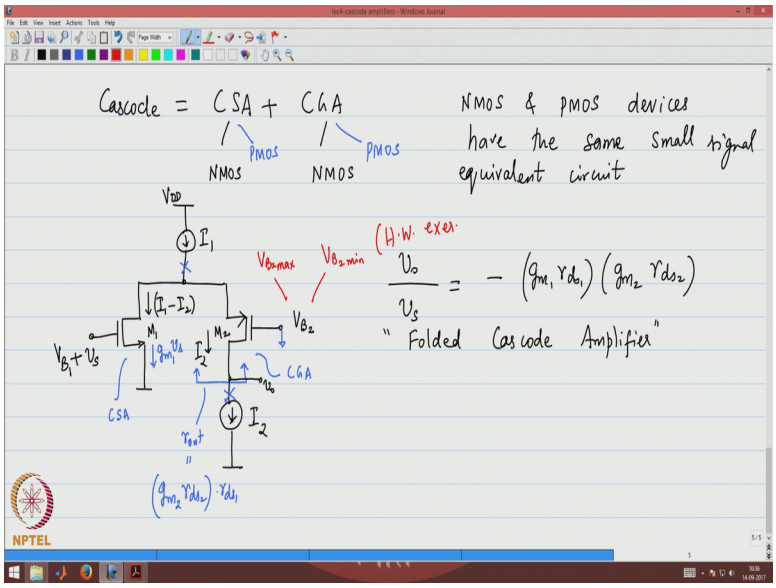

Now, if you remember we had said that the cascode is a common source amplifier cascaded with a common gate amplifier the common source amplifier is an NMOS common source amplifier and in the first case. We had seen that the common gate amplifier is also an NMOS device, but remember that the NMOS and PMOS both NMOS and PMOS transistors have the same small signal equivalent circuit.

Therefore in reality either of these 2 devices could be NMOS or PMOS because only the biasing details will differ. Let us look at one variant where the common source amplifier

is composed of an NMOS device, but the common gate amplifier is composed of a PMOS device. So, the common source amplifier has a bias voltage V B plus the small signal voltage V s applied at its gate and now you are going to have a common gate amplifier, but instead of an NMOS transistors you are going to have a PMOS transistor.

Now, because of the because the biasing details will change I am going to show it in a slight draw the circuit in a slightly different fashion I am going to draw it like this in a minute you will see why I am going to connect the gate of PMOS transistor m 2 to some bias voltage V B 2. Now why am a drawing the PMOS transistor like this because in general convention current flows from bias current or total current flows from top to bottom and inside the PMOS transistor current will flow only from the source to the drain which is the opposite of the NMOS device.

Now, to bias the NMOS and PMOS device remember that at the output we connected a current source in this case we will have a current source to ground I will call that I two, but clearly you need a current flowing into the drain of NMOS transistor. And I will show that as a; current source I 1 what is the bias current drain current of m 2 that is simply I 2 the bias current of m 1 is clearly I 1 minus I 2.

So, the NMOS transistor is biased at a current I 1 minus I 2 and therefore, V B one the bias voltage for the NMOS device should be chosen appropriately in such a case if you look at the small signal equivalent circuit I will show that in blue the gate of the PMOS transistor will be grounded. So, this acts as a common gate amplifier this clearly acts still acts as a common source amplifier and this is an open circuit and this is an open circuit. And therefore, the circuit still looks like a common source amplifier stacked with a common gate amplifier and the overall output resistance is still g m 2 r ds 2 times r ds 1.

The overall trans conductance in other words the signal current flowing is g m 1 times V s the overall gain seen from the output which is taken at the drain of m 2. So, the overall gain of the circuit is still minus g m 1 r ds 1 times g m 2 r ds 2. So, it still looks like the product of to intrinsic gains the only difference being that one of the devices is an NMOS is a PMOS transistor this particular circuit is called a folded cascode amplifier.

Because the circuit looks like, because the way the circuit is drawn the current is folded into the PMOS device and you can see; I will leave this as a homework exercise I will leave the calculation of V B 2 max and V B 2 min as an exercise for the viewer. Now we

will complete with a small discussion on how to increase the gain further; suppose, I want to increase the gain even further without increasing the number of stages.

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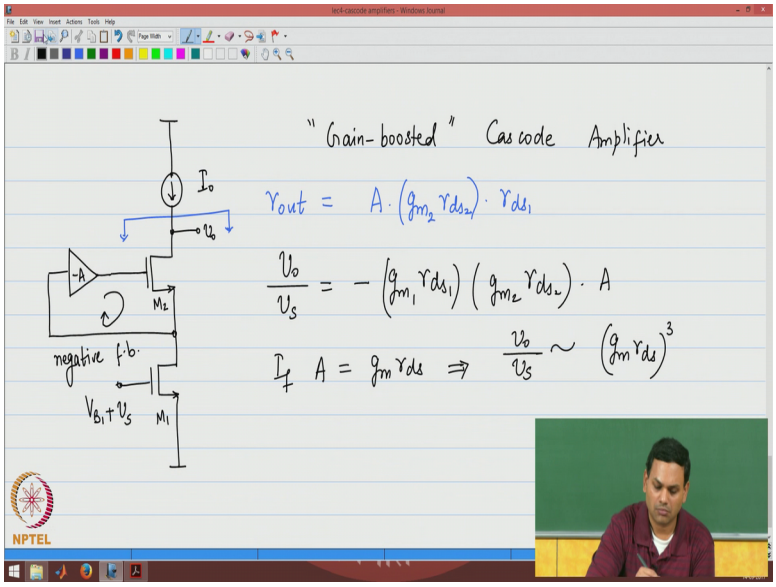

There is one more option to do this I will show that with an illustration on the NMOS cascade. Now in the original cascode amplifier the gate of m 2 was connected to signal ground it was connected to a appropriate dc voltage.

In our case, what we will do is we will try feeding back the signal from the drain of m 1 to the gate of m 2 through an amplifier of gain minus a as you can see you need an amplifier of minus a to ensure that you have negative feedback as a turns out this particular circuit has an r out which is equal to a times g m 2 r ds 2 times r ds 1; in other words, the negative feedback push is the output gain a output resistance even further by and value equal to a.

What does this mean for the gain of the circuit this means that V o over V s which is the gain of the circuit is now minus g m 1 r ds 1 into g m 2 r ds 2 into a. So, in other words if you have an amplifier of gain a which may also be a third intrinsic gain you can get gains of the order of the cube of g m r ds if a over of the order of an intrinsic gain V o by V s is of the order of g m r ds the whole cubed this particular circuit is called the Gain-boosted Cascode.